Data sheet acquired from Cypress Semiconductor Corporation.
Data sheet modified to remove devices not offered.

TEXAS INSTRUMENTS

SCCS058 - March 1997 - Revised March 2000

CY74FCT163646

16-Bit Registered Transceiver

Features

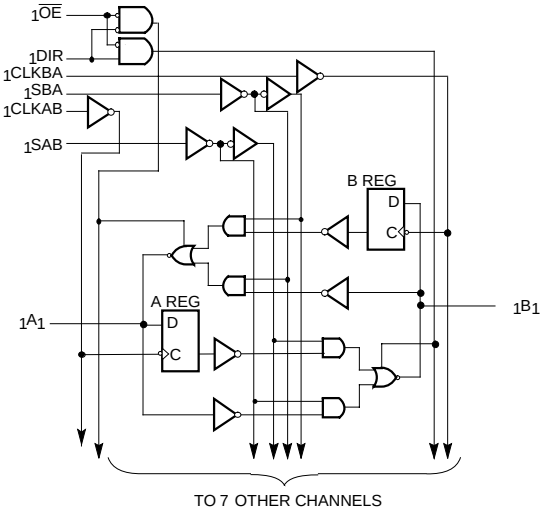
- **Low power, pin-compatible replacement for LCX and LPT families**
- **5V tolerant inputs and outputs**
- **24 mA balanced drive outputs**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for reduced noise**
- **FCT-C speed at 5.4 ns**
- **Latch-up performance exceeds JEDEC standard no. 17**
- **ESD > 2000V per MIL-STD-883D, Method 3015**
- **Typical output skew < 250 ps**
- **Industrial temperature range of –40˚C to +85˚C**
- **TSSOP (19.6-mil pitch) or SSOP (25-mil pitch)**
- **Typical V_{olp} (ground bounce) performance exceeds Mil Std 883D**
- **V_{CC} = 2.7V to 3.6V**

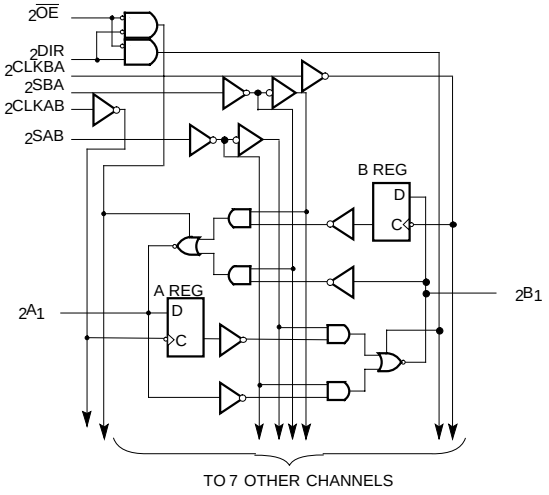
Functional Description

The CY74FCT163646 16-bit transceiver is a three-state, D-type register, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH logic level. Output Enable ($\overline{OE}$) and direction pins (DIR) are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register, or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the Output Enable ($\overline{OE}$) is Active LOW. In the isolation mode (Output Enable ($\overline{OE}$) HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

The CY74FCT163646 has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The inputs and outputs were designed to be capable of being driven by 5.0V buses, allowing them to be used in mixed voltage systems as translators. The outputs are also designed with a power-off disable feature enabling them to be used in applications requiring live insertion.

Logic Block Diagrams

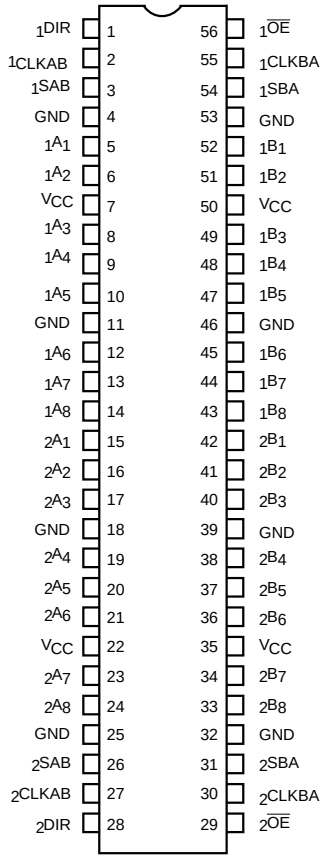




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Pin Configuration

SSOP/TSSOP
Top View



Pin Description

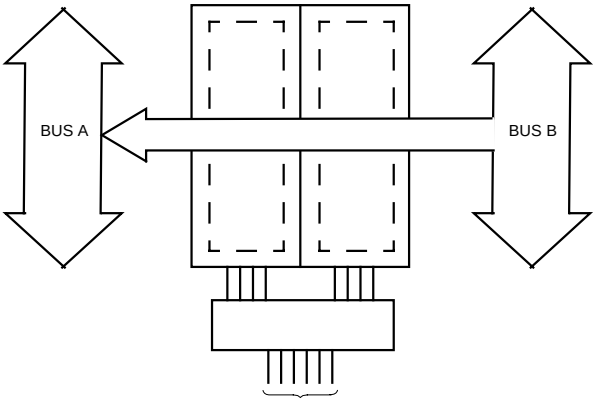
Pin Names	Description
A	Data Register A Inputs Data Register B Outputs
B	Data Register B Inputs Data Register A Outputs
CLKAB, CLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR	Direction
$\overline{OE}$	Output Enable (Active LOW)

Function Table[1]

Inputs						Data I/O[2]		Function
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A	B	
H H	X X	H or L ⌐¬	H or L ⌐¬	X X	X X	Input	Input	Isolation Store A and B Data
L L	L L	X X	X H or L	X X	L H	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real Time A Data to Bus Stored A Data to B Bus

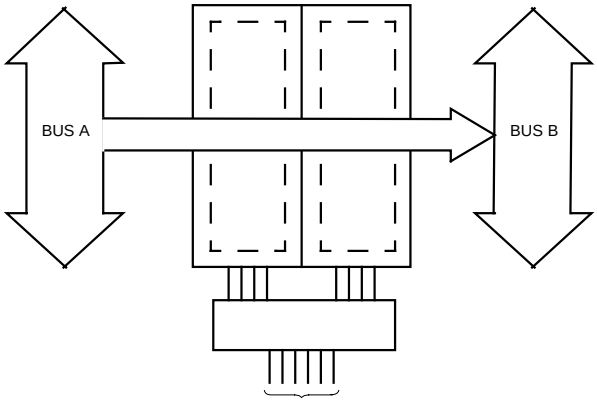
Notes:

1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, ⌐¬ = LOW-to-HIGH Transition
2. The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.



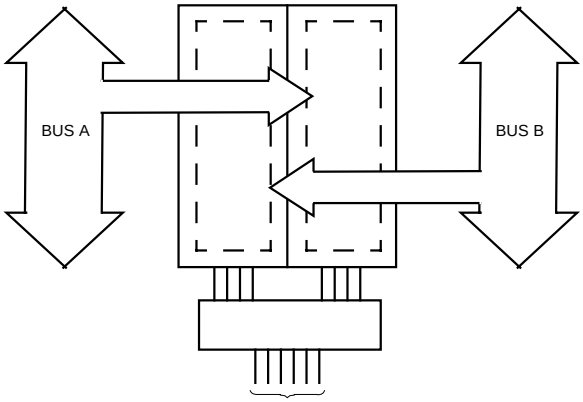
DIR	$\overline{OE}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

Real-Time Transfer
Bus B to Bus A



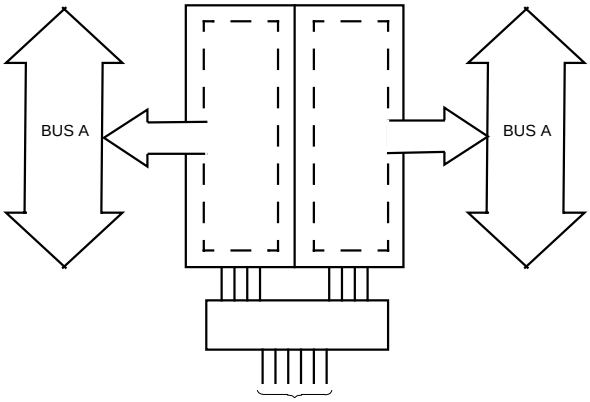
DIR	$\overline{OE}$	CLKAB	CLKBA	SAB	SBA
H	L	X	X	L	X

Real-Time Transfer
Bus A to Bus B



DIR	$\overline{OE}$	CLKAB	CLKBA	SAB	SBA
H	L	⌐	X	X	X
L	L	X	⌐	X	X
X	H	⌐	⌐	X	X

Storage from
A and/or B



DIR [3]	$\overline{OE}$	CLKAB	CLKBA	SAB	SBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

Transfer Stored Data
to A and/or B

Maximum Ratings[4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature with
Power Applied ..... –55°C to +125°C

Supply Voltage Range ..... 0.5V to +4.6V

DC Input Voltage .....–0.5V to +7.0V

DC Output Voltage .....–0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin) .....–60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage.....>2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	2.7V to 3.6V

Notes:

3. Cannot transfer data to A-bus and B-bus simultaneously.
4. Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics Over the Operating Range V_{CC}=2.7V to 3.6V

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
V_{IH}	Input HIGH Voltage	All Inputs	2.0		5.5	V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[6]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA		–0.7	–1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=5.5V			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=5.5V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=GND			±1	µA
I_{ODL}	Output LOW Dynamic Current[7]	V_{CC}=3.3V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	45		180	mA
I_{ODH}	Output HIGH Dynamic Current[7]	V_{CC}=3.3V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	–45		–180	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}= –0.1 mA	V_{CC}–0.2			V
		V_{CC}=3.0V, I_{OH}= –8 mA	2.4[8]	3.0		
		V_{CC}=3.0V, I_{OH}= –24 mA	2.0	3.0		
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}= 0.1mA			0.2	V
		V_{CC}=Min., I_{OL}= 24 mA		0.3	0.5	
I_{OS}	Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=GND	–60	–135	–240	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V			±100	µA

Capacitance[5] (T_A = +25˚C, f = 1.0 MHz)

Symbol	Description[9]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} =0V	5.5	8.0	pF

Notes:

5. Typical values are at V_{CC}=3.3V, T_A=+25˚C ambient.
6. This parameter is specified but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametrics tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
8. V_{OH}=V_{CC}–0.6 V at rated current.
9. This parameter is measured at characterization but not tested.

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \le 0.2V$ $V_{IN} \ge V_{CC}-0.2V$	0.1	10	µA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC}=Max.	$V_{IN}=V_{CC}-0.6V$[10]	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[11]	V_{CC}=Max., Outputs Open DIR=OE=GND One-Bit Toggling 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	50	75	µA/MHz
I_C	Total Power Supply Current[12]	V_{CC}=Max.,Outputs Open f_0=10 MHz (CLKBA) 50% Duty Cycle DIR=$\overline{OE}$=GND One-Bit Toggling, f_1=5 MHz, 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	0.5	0.8	mA
			$V_{IN}=V_{CC}-0.6V$ or V_{IN}=GND	0.5	0.8	
		V_{CC}=Max., Outputs Open f_0=10 MHz (CLKBA) 50% Duty Cycle DIR=$\overline{OE}$=GND Sixteen-Bits Toggling f_1=2.5 MHz 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	2.5	3.8[13]	
			$V_{IN}=V_{CC}-0.6V$ or V_{IN}=GND	2.6	4.1[13]	

Notes:

10. Per TTL driven input); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0N_C/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    N_C = Number of clock inputs changing at f_1
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range V_{CC}=3.0V to 3.6V[14,15]

Parameter	Description	CY74FCT163646C		Unit	Fig. No.[16]
		Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5	5.4	ns	1, 2
t_{PZH} t_{PZL}	Output Enable Time DIR or $\overline{OE}$ to Bus	1.5	7.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time DIR or $\overline{OE}$ to Bus	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.5	5.7	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus	1.5	6.2	ns	1,5
t_{SU}	Set-Up Time HIGH or LOW Bus to Clock	2.0	—	ns	4
t_H	Hold Time HIGH or LOW Bus to Clock	1.5	—	ns	4
t_W	Clock Pulse Width HIGH or LOW	5.0	—	ns	6
$t_{SK(O)}$	Output Skew[17]	—	0.5	ns	—

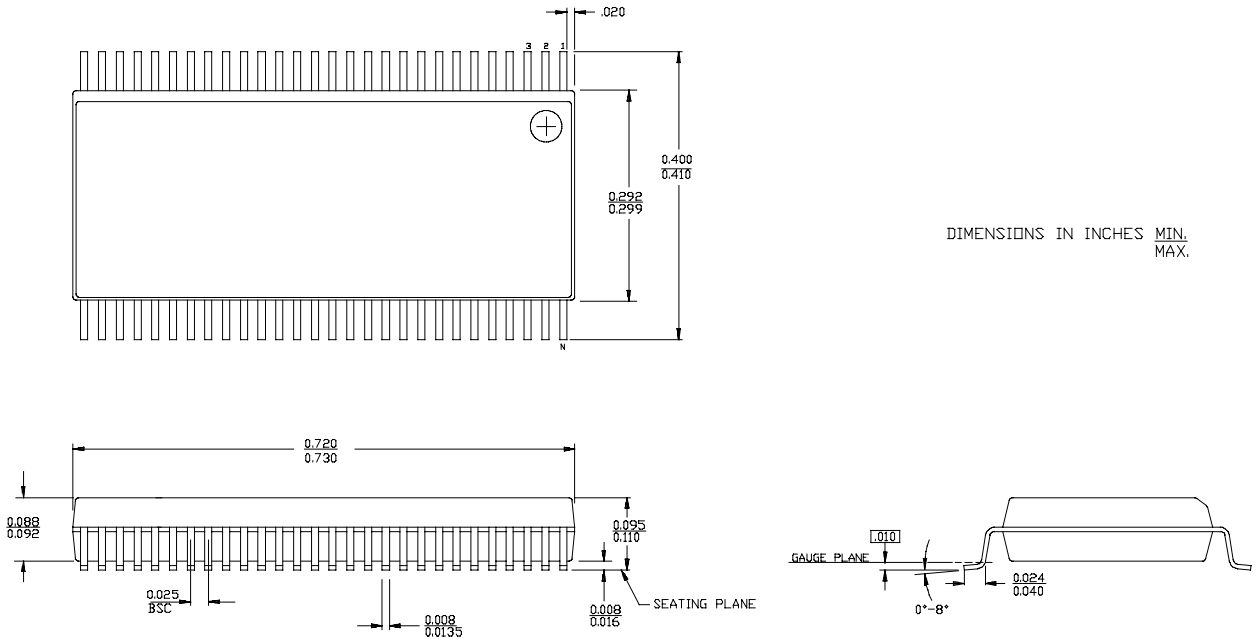
Ordering Information CY74FCT163646

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT163646CPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163646CPVC/PVCT	O56	56-Lead (300-Mil) SSOP	

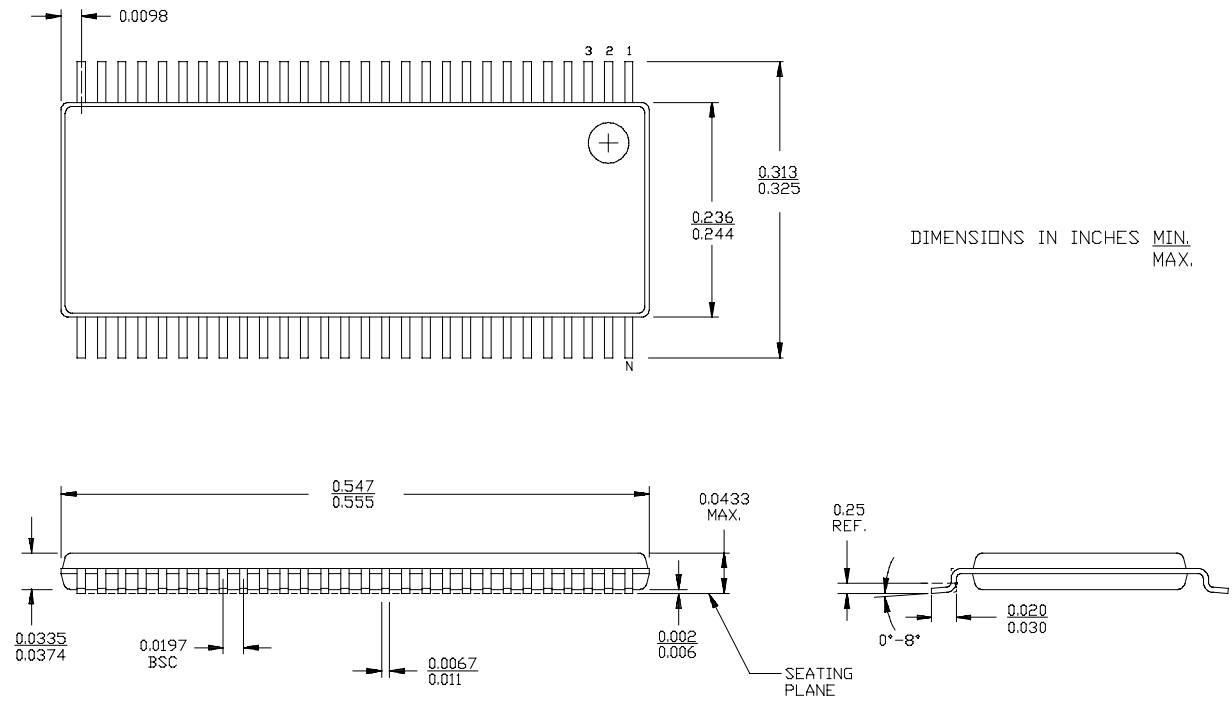
Notes:
14. Minimum limits are specified but not tested on Propagation Delays.
15. For V_{CC} =2.7, propagation delay, output enable and output disable times should be degraded by 20%.
16. See “Parameter Measurement Information” in the General Information section.
17. Skew any two outputs of the same package switching in the same direction. This parameter is ensured by design.

Package Diagrams

56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package Z56



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CY74FCT163646CPAC	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
CY74FCT163646CPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
CY74FCT163646CPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
CY74FCT163646CPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

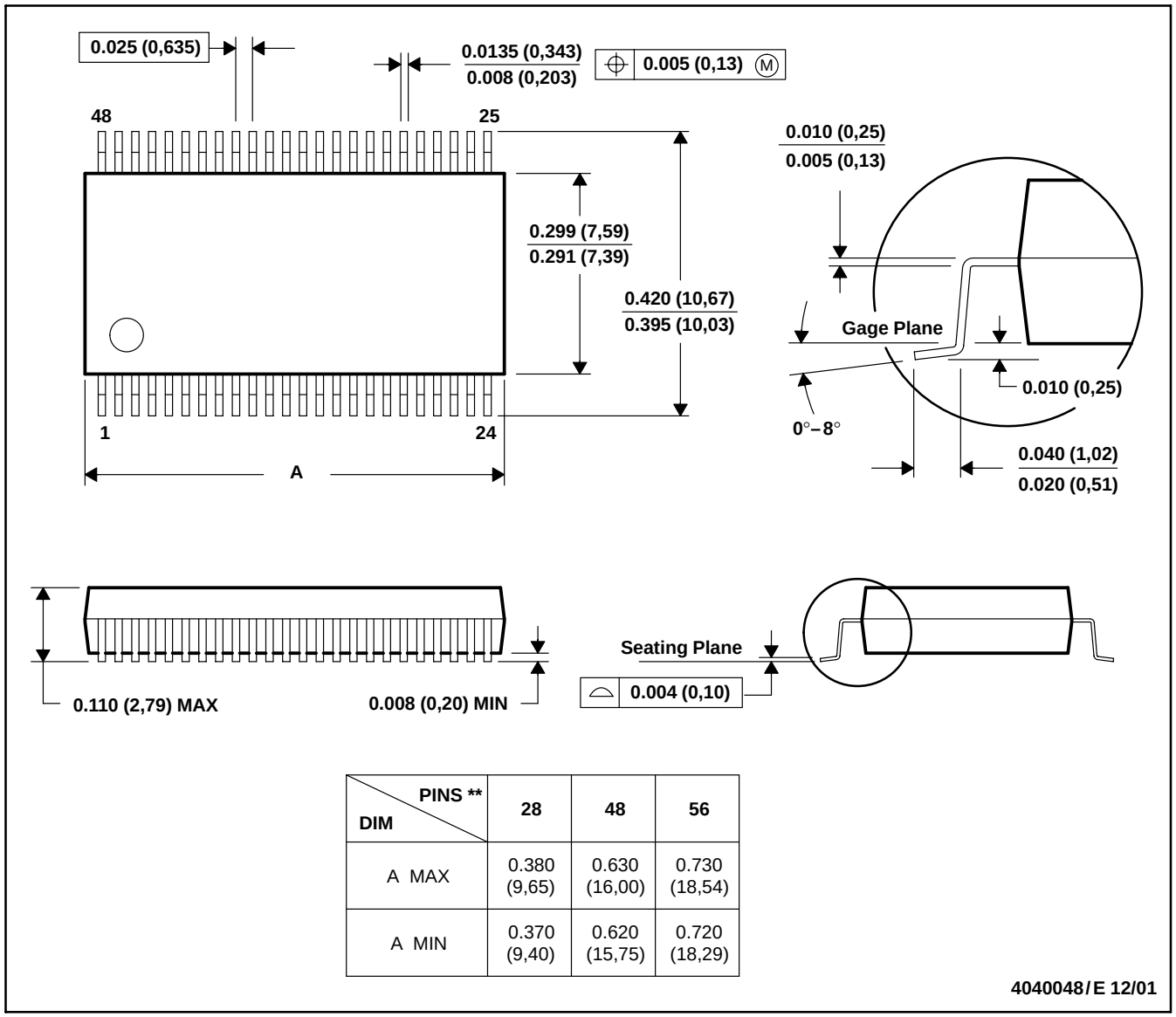
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



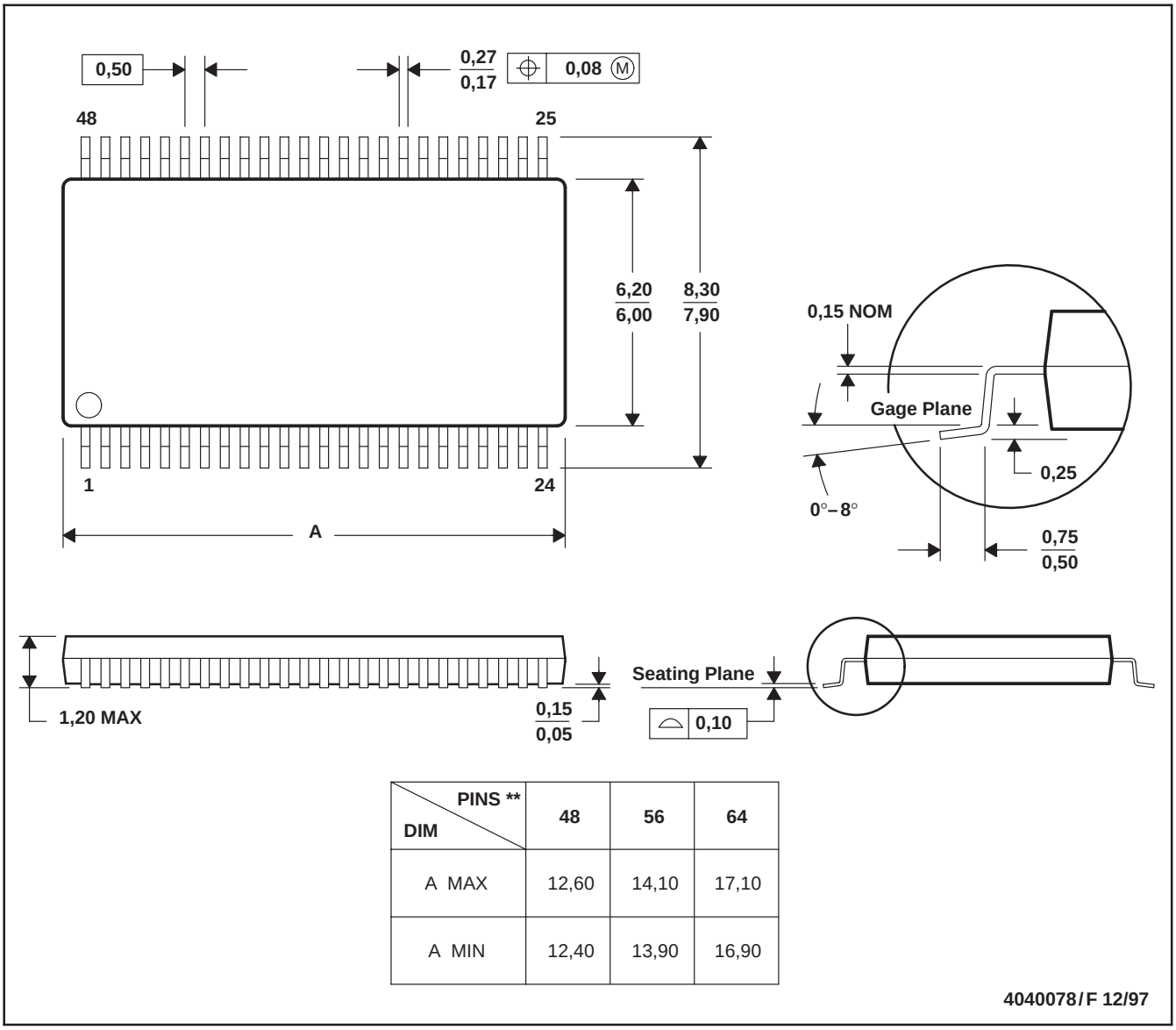
DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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MSP430G2403IPW28 OPA643P TLV990-28PFB TPA6203A1DRBR BQ24314DSGR TPS7A8018DRBR
TPS92200D2DDCR MSP430F2001TRSAT TLC085CDR TPS71710DCKR MSP430F47127IPZ
UA9637ACPS ISO124U/1K MSP430F2112TRHBT PCM56U SN74GTL2006PWR SN74LVCZ240APW
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