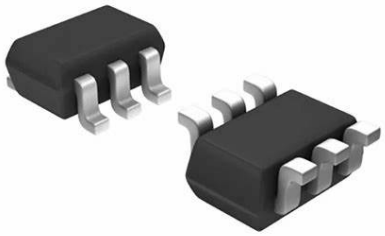
HJKE
WWW.HJKEIC.COM

PESD3V3L5UY

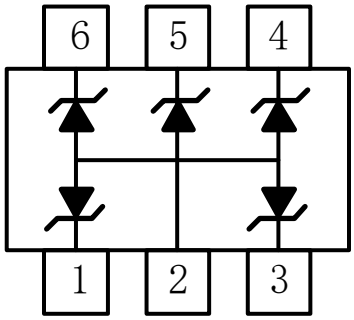
5-Line Ultra TVS Array

Features

- Low leakage current
- Operating voltage: 3.3V
- Low clamping voltage
- JEDEC SOT-363 package
- Complies with following standards:
  - – IEC 61000-4-2 (ESD) immunity test
    - Air discharge: ±30kV
    - Contact discharge: ±30kV
  - – IEC61000-4-5 (Lightning) 3A (8/20μs)
- RoHS Compliant



SOT-363



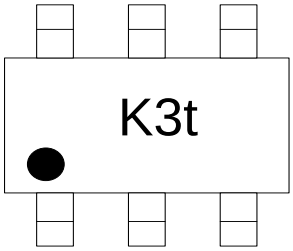
Circuit diagram

Mechanical Characteristics

- Package: SOT-363
- Lead Finish: Matte Tin
- Case Material: “Green” Molding Compound.
- Terminal Connections: See Diagram Below

Applications

- Peripherals
- Industrial Equipment
- Notebook Computers
- Portable Instrumentation
- Microprocessor Based Equipment
- Cell Phone Handsets and Accessories
- Personal Digital Assistants (PDAs) and Pagers



K3t = Device Marking Code

Dot denotes Pin1

Marking (Top View)

Ordering Information

Part Number	Packaging	Reel Size
PESD3V3L5UY	3000/Tape & Reel	7 inch

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

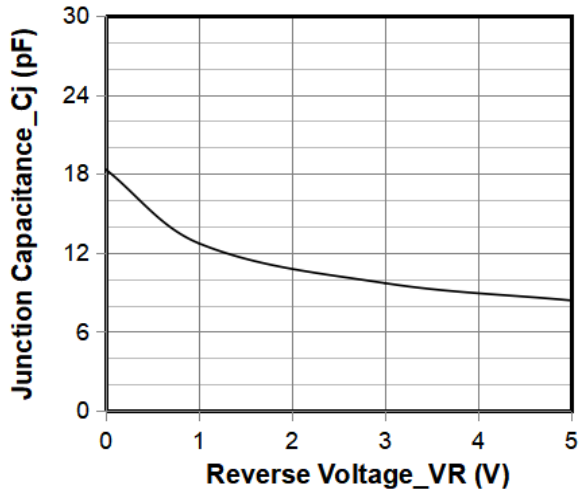
Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20μs)	Ppk	35	W
Peak Pulse Current (8/20μs)	I_{PP}	3	A
ESD per IEC 61000−4−2 (Air) ESD per IEC 61000−4−2 (Contact)	V_{ESD}	±30 ±30	kV
Operating Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	Tstg	−55 to +150	°C

Electrical Characteristics (T_A=25°C unless otherwise specified)

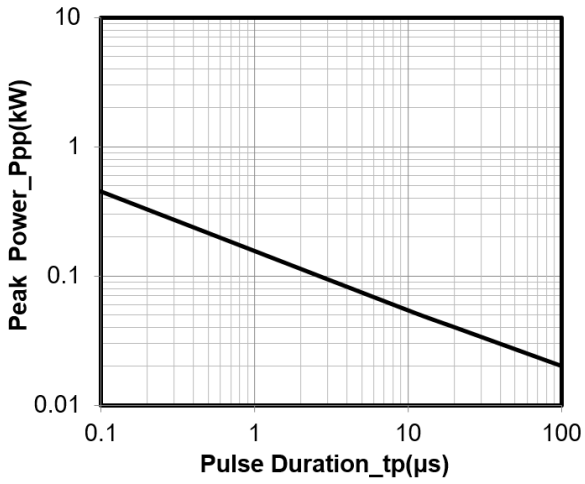
Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V_{RWM}			3.3	V	
Reverse Breakdown Voltage	V_{BR}	5.3		8.5	V	I_T = 1mA
Reverse Leakage Current	I_R			0.2	μA	V_{RWM} = 5V, any I/O pin to ground
Clamping Voltage	V_C			9	V	I_{PP} = 1A (8 x 20μs pulse), any I/O pin to ground
Clamping Voltage	V_C			12	V	I_{PP} = 3A (8 x 20μs pulse), any I/O pin to ground
Junction Capacitance	C_J		20		pF	VR = 0V, f = 1MHz, any I/O pin to ground

Note 1: I/O pins are Pin 1, 3, 4, 5, 6

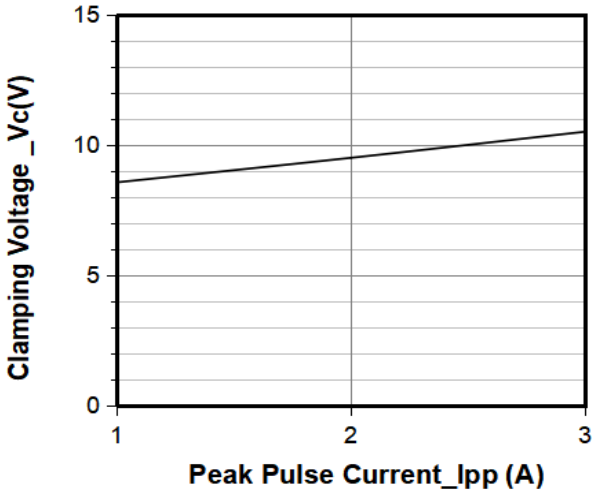
Typical Performance Characteristics (TA=25°C unless otherwise Specified)



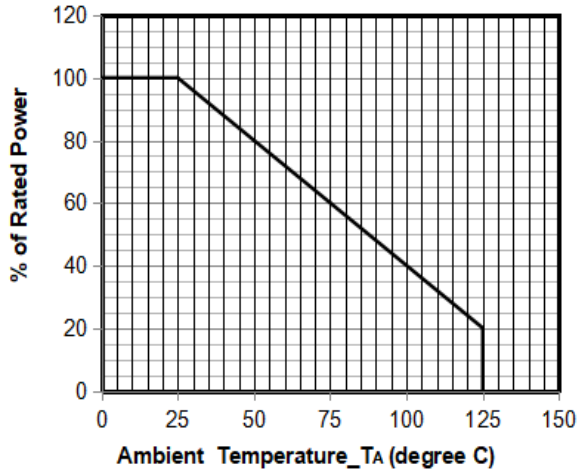
Junction Capacitance vs. Reverse Voltage



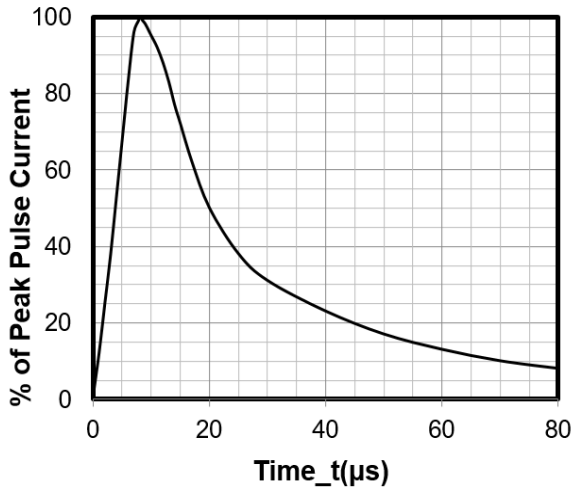
Peak Pulse Power vs. Pulse Time



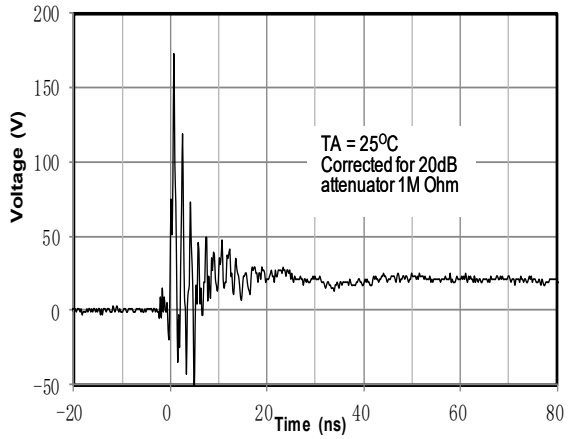
Clamping Voltage vs. Peak Pulse Current



Power Derating Curve



8 X 20μs Pulse Waveform

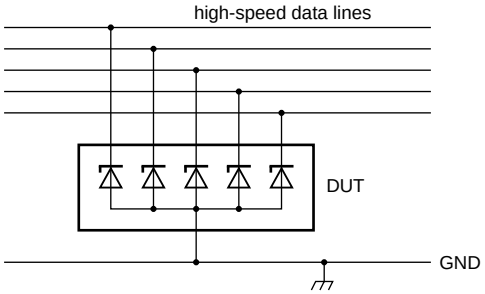


ESD Clamping Voltage

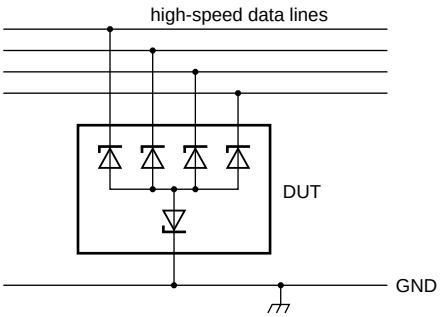
8 kV Contact per IEC61000−4−2

Application information

The devices are designed for the protection of up to five unidirectional data or signal lines from the damage caused by ESD and surge pulses. The devices may be used on lines where the signal polarities are both, positive and negative with respect to ground. The devices provide a surge capability of 35 W per line for an 8/20 µs waveform each.



Typical application for unidirectional application of five lines



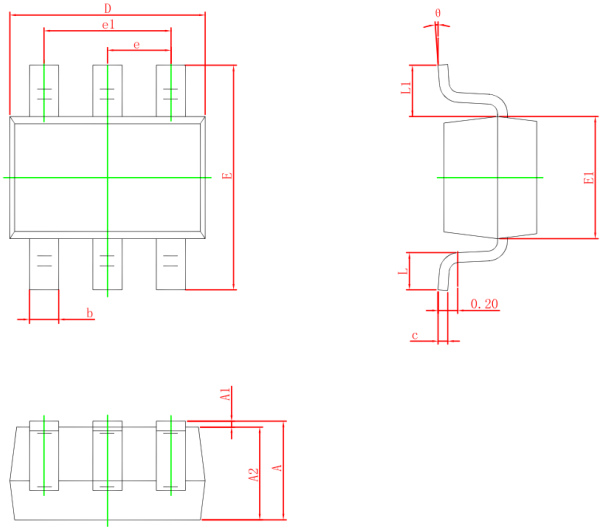
Typical application for bidirectional application of four lines

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

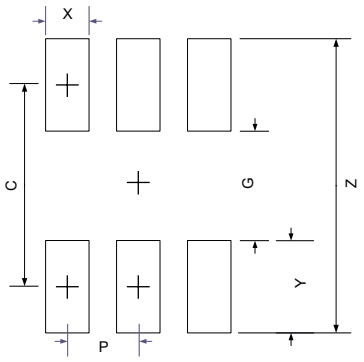
1. Place the device as close to the input terminal or connector as possible.
2. The path length between the device and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

SOT-363 Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0. 900	-	1.100	0.035	-	0.043
A1	0.000	-	0.100	0.000	-	0.004
A2	0.900	-	1.000	0.035	-	0.039
b	0.150	-	0.350	0.006	-	0.014
c	0.080	-	0.150	0.003	-	0.006
D	2.000	-	2.200	0.079		0.087
E	2.150	-	2.450	0.085	-	0.096
E1	1.150	-	1.350	0.045	-	0.053
e	0.650 TYP.			0.026 TYP.		
e1	1.200	-	1.400	0.047	-	0.055
L	0.260	-	0.460	0.010	-	0.018
L1	0.525 REF.			0.021 REF.		
θ	0°	-	8°	0°	-	8°

Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	1.85	0.073
G	1.00	0.039
P	0.65	0.026
X	0.40	0.016
Y	0.85	0.033
Z	2.70	0.106