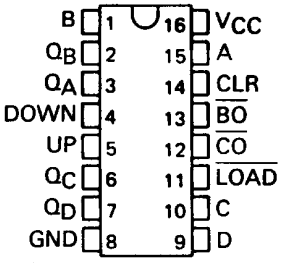
SN54192, SN54193, SN54LS192, SN54LS193, SN74192, SN74193, SN74LS192, SN74LS193
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

SDLS074 – DECEMBER 1972 – REVISED MARCH 1988

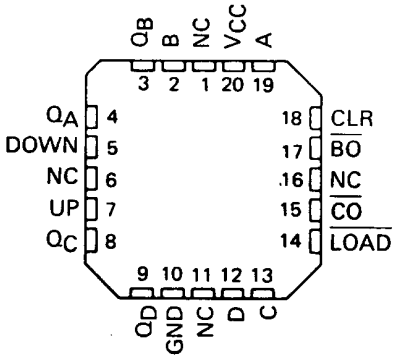
- **Cascading Circuitry Provided Internally**
- **Synchronous Operation**
- **Individual Preset to Each Flip-Flop**
- **Fully Independent Clear Input**

TYPES	TYPICAL MAXIMUM COUNT FREQUENCY	TYPICAL POWER DISSIPATION
'192,'193	32 MHz	325 mW
'LS192,'LS193	32 MHz	95 mW

SN54192, SN54193, SN54LS192, SN54LS193 . . . J OR W PACKAGE
SN74192, SN74193 . . . N PACKAGE
SN74LS192, SN74LS193 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS192, SN54LS193 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

description

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The '192 and 'LS192 circuits are BCD counters and the '193 and 'LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

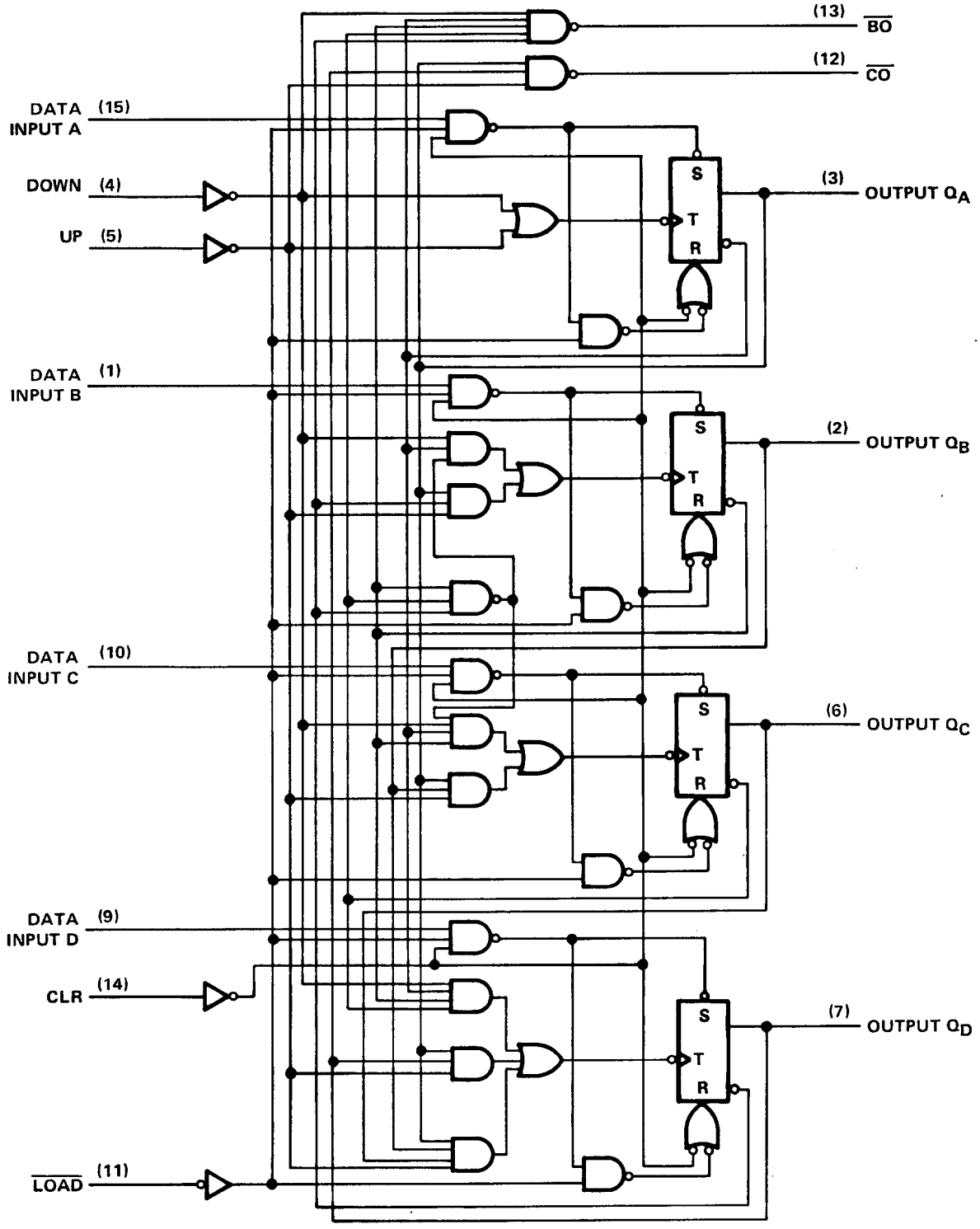
	SN54'	SN54LS'	SN74'	SN74LS'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	7	7	V
Input voltage	5.5	7	5.5	7	V
Operating free-air temperature range	−55 to 125		0 to 70		°C
Storage temperature range	−65 to 150		−65 to 150		°C

NOTE 1: Voltage values are with respect to network ground terminal.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

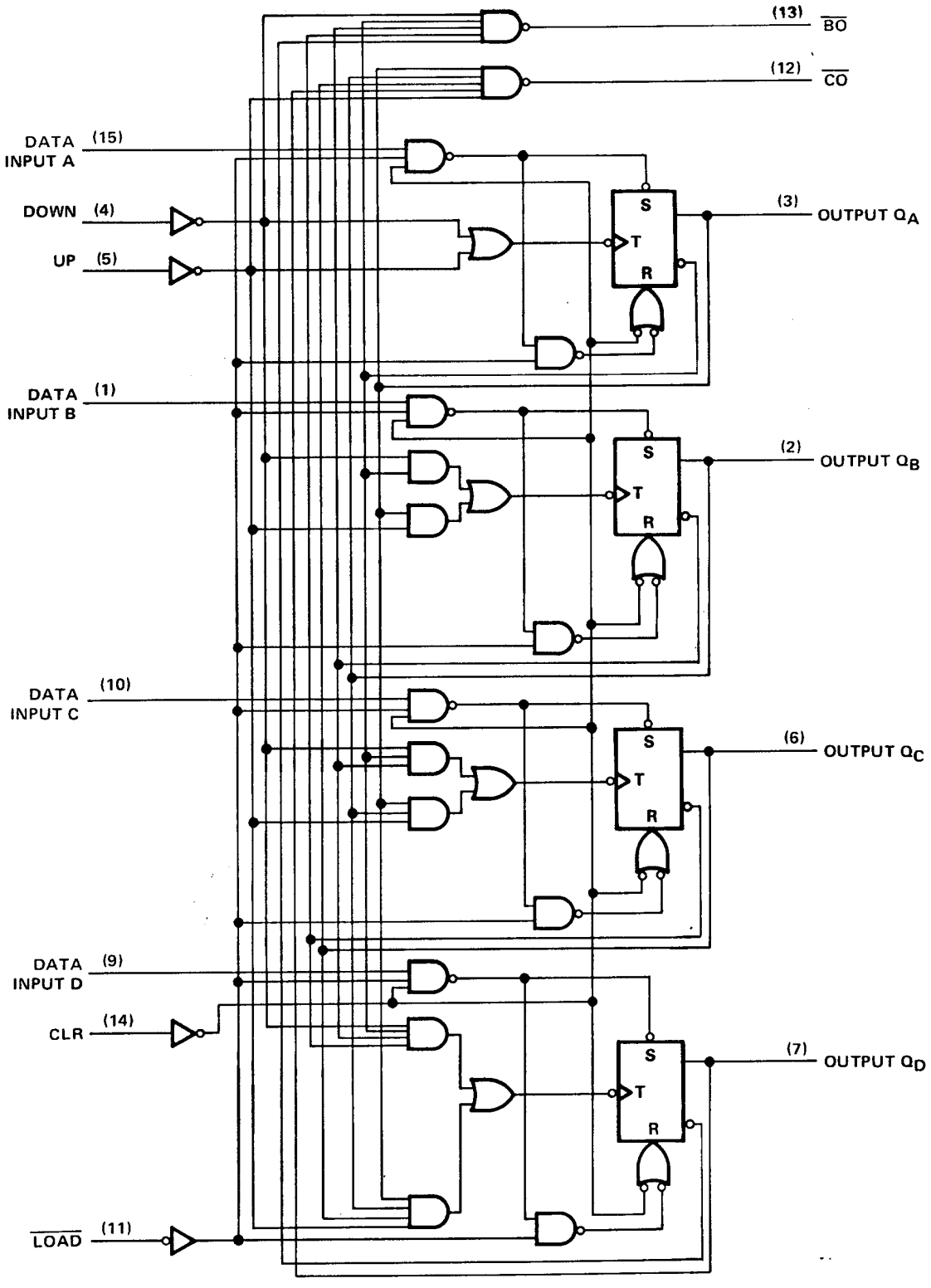
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logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

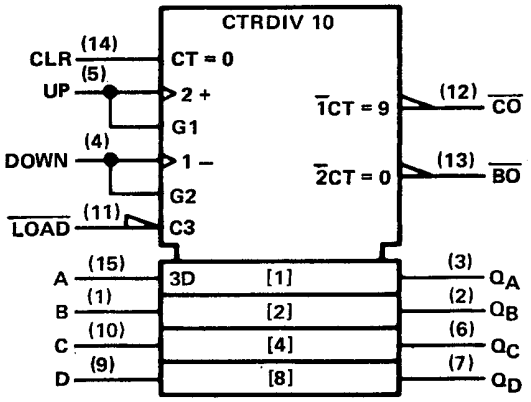
logic diagram (positive logic)



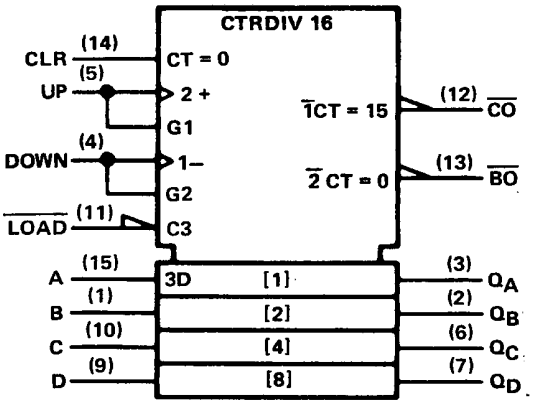
Pin numbers shown are for D, J, N, and W packages.

logic symbols†

'192



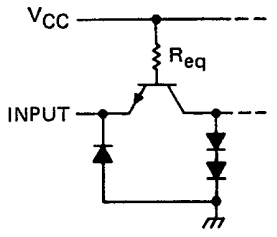
'193



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

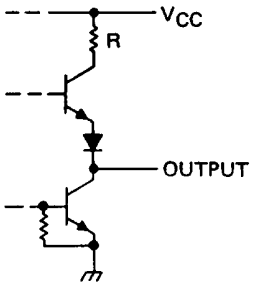
schematics of inputs and outputs

EQUIVALENT OF INPUTS
OF '192, '193



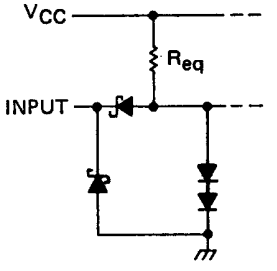
'192, '193: R_{eq} = 4 kΩ NOM

TYPICAL OF OUTPUTS
OF '192, '193



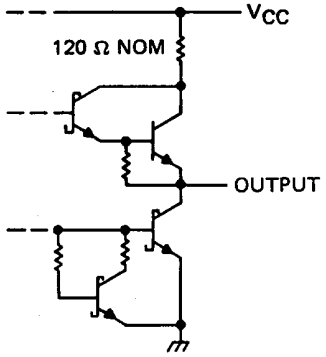
'192, '193: R = 130 Ω NOM

EQUIVALENT OF INPUTS
OF 'LS192, 'LS193



Load input: R_{eq} = 25 kΩ NOM
All other inputs: R_{eq} = 17 kΩ NOM

TYPICAL OF OUTPUTS
OF 'LS192, 'LS193

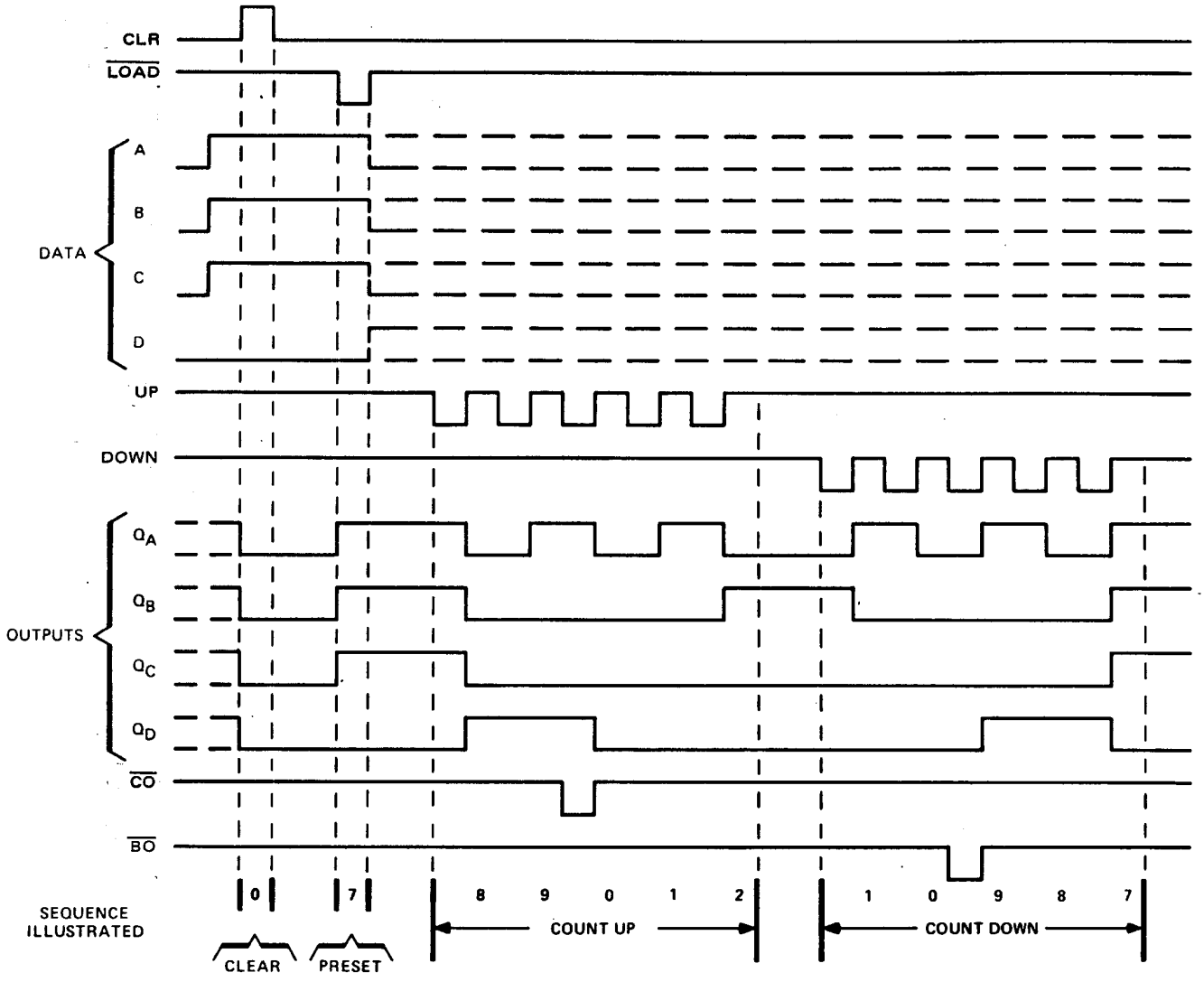


'192, 'LS192 DECADE COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



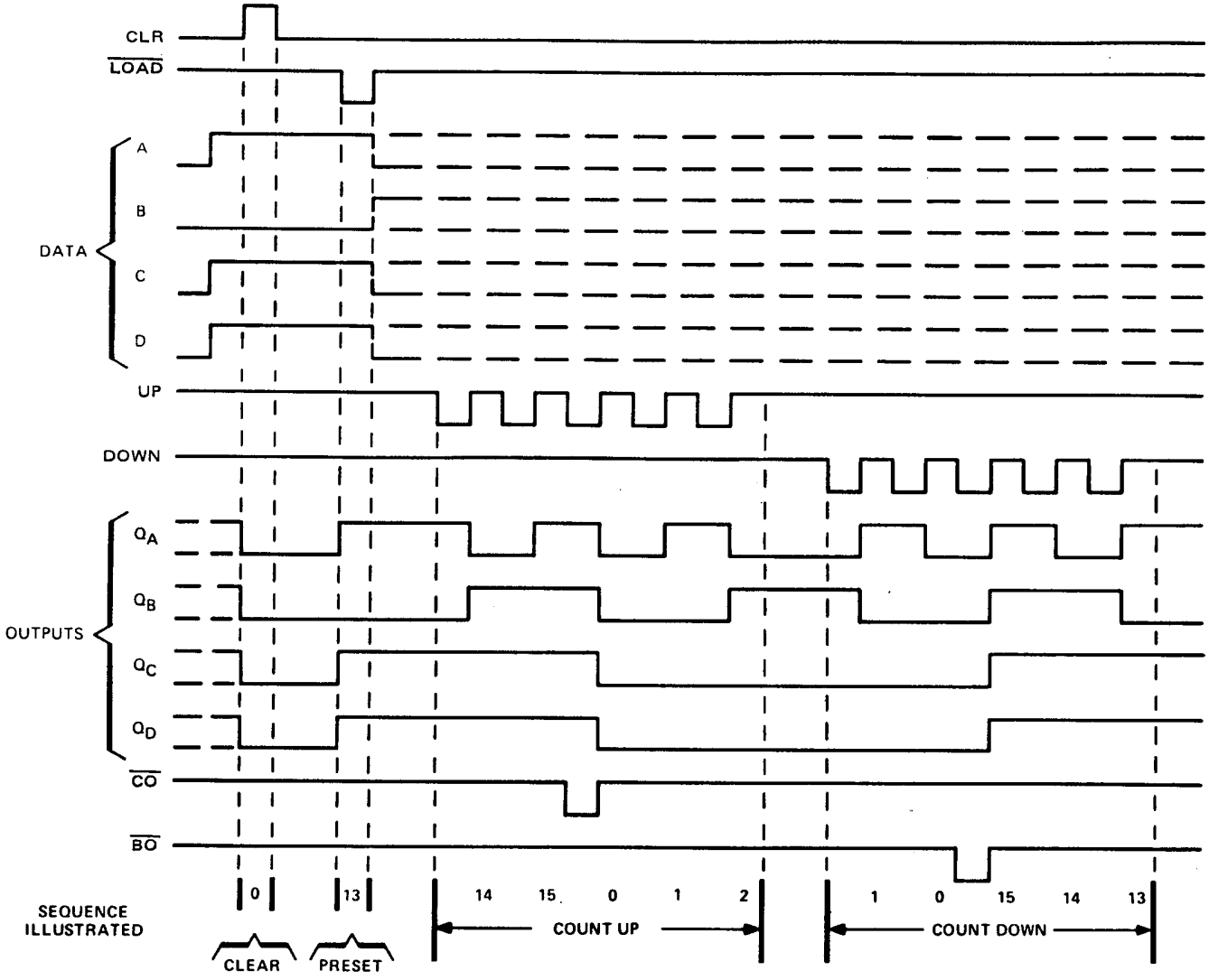
NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

'193, 'LS193 BINARY COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

recommended operating conditions

			SN54192 SN54193			SN74192 SN74193			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				16			16	mA
f_{clock}	Clock frequency		0		25	0		25	MHz
t_w	Width of any input pulse		20			20			ns
t_{su}	Data setup time, (see Figure 1)		20			20			ns
t_h	Hold time	Data, high or low	0			0			ns
		$\overline{LOAD}$	3			3			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54192 SN54193			SN74192 SN74193			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−65	−18		−65	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		65	89		65	102	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figures 1 and 2	25	32		MHz
t_{PLH}	UP	$\overline{CO}$			17	26	ns
t_{PHL}					16	24	
t_{PLH}	DOWN	$\overline{BO}$			16	24	ns
t_{PHL}					16	24	
t_{PLH}	UP OR DOWN	Q			25	38	ns
t_{PHL}					31	47	
t_{PLH}	$\overline{LOAD}$	Q			27	40	ns
t_{PHL}					29	40	
t_{PHL}	CLR	Q			22	35	ns

¶f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

recommended operating conditions

		SN54LS192 SN54LS193			SN74LS192 SN74LS193			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			−400			−400	μA
I_{OL}	Low-level output current			4			8	mA
f_{clock}	Clock frequency	0		25	0		25	MHz
t_w	Width of any input pulse	20			20			ns
t_{su}	Clear inactive-state setup time	15			15			ns
	Load inactive-state setup time	15			15			ns
	Data setup time (see Figure 1)	20			20			ns
t_h	Data hold time	5			5			ns
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

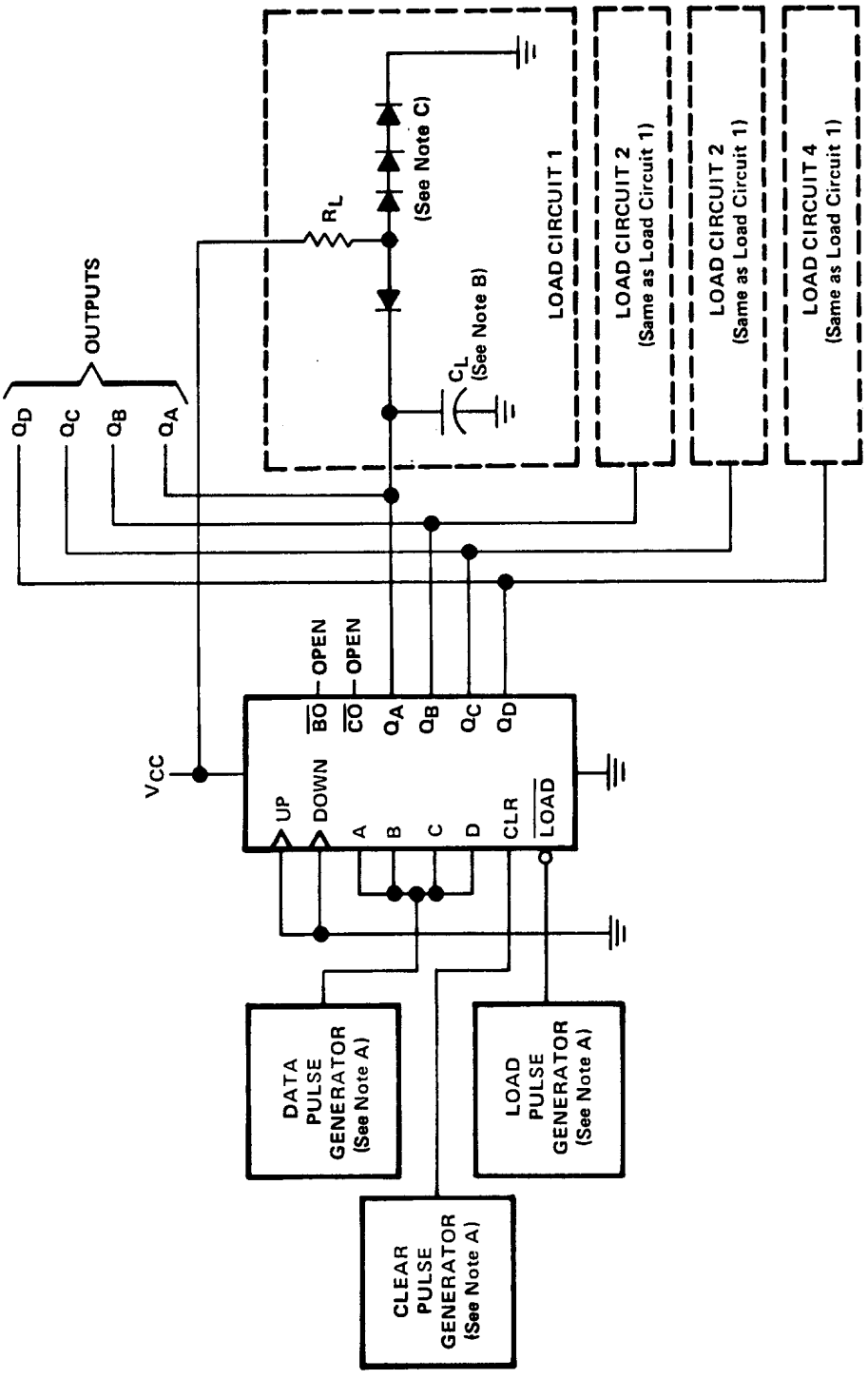
PARAMETER		TEST CONDITIONS†		SN54LS192 SN54LS193			SN74LS192 SN74LS193			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.15	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			19	34		19	34	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 2 kΩ, See Figures 1 and 2	25	32		MHz
t_{PLH}	UP	$\overline{CO}$			17	26	ns
t_{PHL}					18	24	
t_{PLH}	DOWN	$\overline{BO}$			16	24	ns
t_{PHL}					15	24	
t_{PLH}	UP OR DOWN	Q			27	38	ns
t_{PHL}					30	47	
t_{PLH}	$\overline{LOAD}$	Q			24	40	ns
t_{PHL}					25	40	
t_{PHL}	CLR	Q			23	35	ns

PARAMETER MEASUREMENT INFORMATION

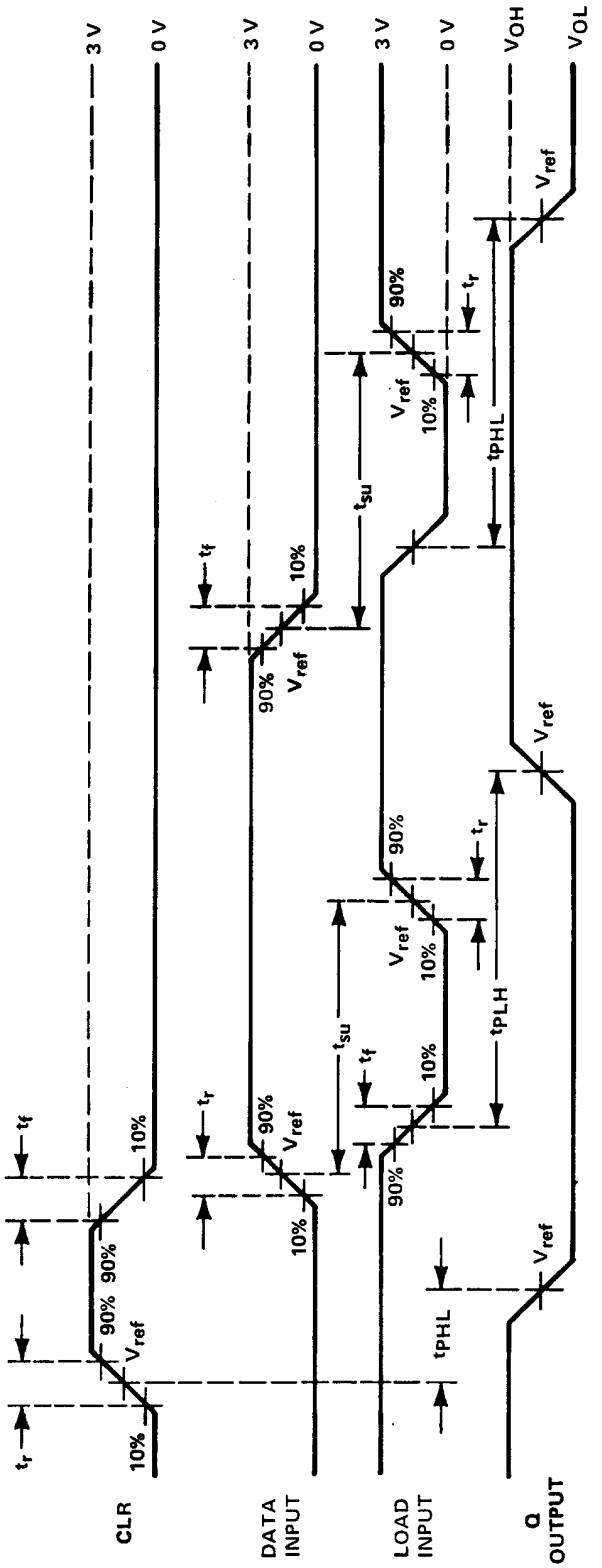


TEST CIRCUIT

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$ and for the data pulse generator PRR $\leq$ 500 kHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064 or equivalent.
D. t_r and $t_f \leq 7$ ns.
E. V_{ref} is 1.5 V for '192 and '193, 1.3 V for 'LS192 and 'LS193.

FIGURE 1A – CLEAR, SETUP AND LOAD TIMES

PARAMETER MEASUREMENT INFORMATION

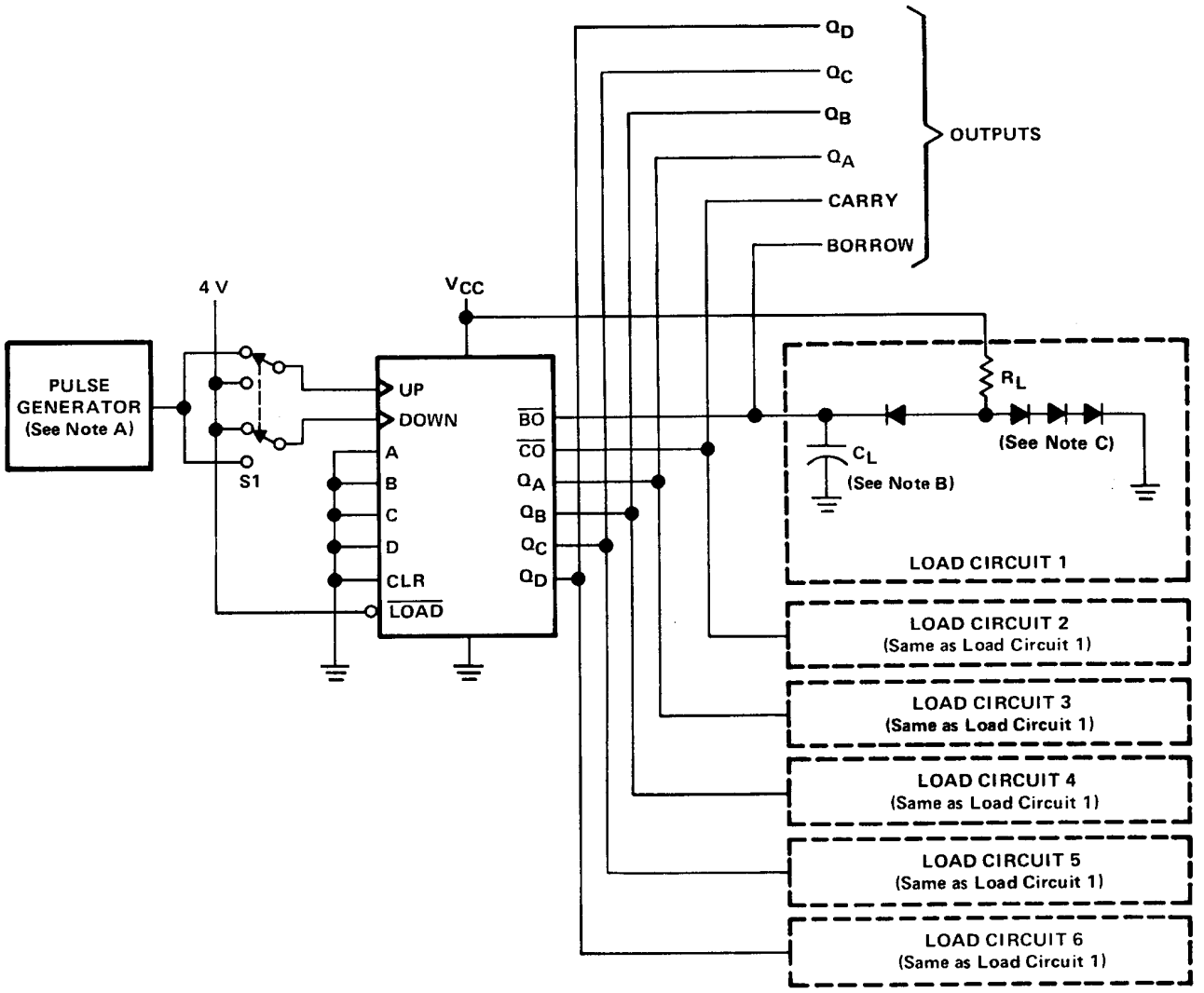


VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$ and for the data pulse generator PRR ≤ 500 kHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064 or equivalent.
D. t_r and $t_f \leq 7$ ns.
E. V_{ref} is 1.5 V for '192 and '193, 1.3 V for 'LS192 and 'LS193.

FIGURE 1B – CLEAR, SETUP, AND LOAD TIMES

PARAMETER MEASUREMENT INFORMATION

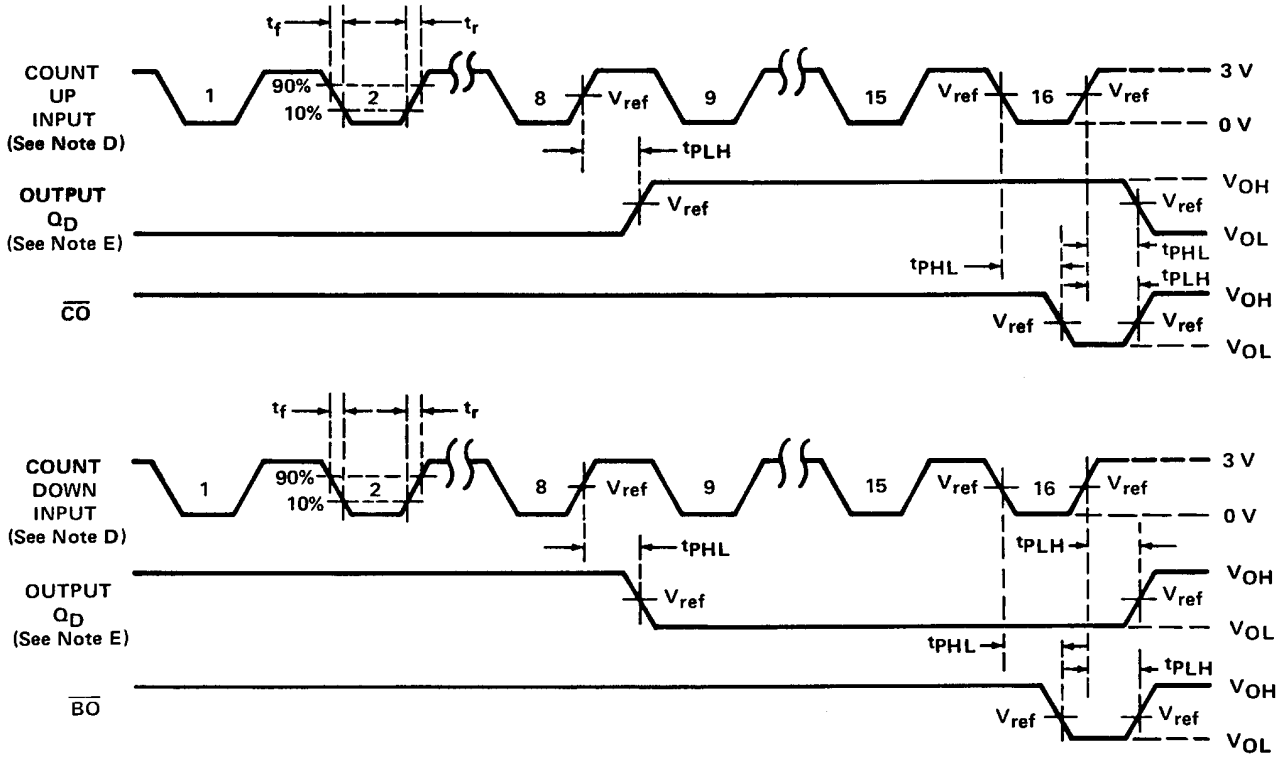


TEST CIRCUIT

NOTES: A. The pulse generators have the following characteristics: PRR ≈ 1 MHz, Z_{out} ≈ 50 Ω, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064 or equivalent.
D. Cout-up and dount-down pulse shown are for the '193 and 'LS193 binary counters. Count cycle for '192 and 'LS192 decade counters is 1 through 10.
E. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.
F. t_r and t_f ≤ 7 ns.
G. V_{ref} is 1.5 V for '192 and '193, 1.3 V for 'LS192 and 'LS193.

FIGURE 2A – PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: PRR ≈ 1 MHz, Z_{out} ≈ 50 Ω, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064 or equivalent.
D. Cout-up and dount-down pulse shown are for the '193 and 'LS193 binary counters. Count cycle for '192 and 'LS192 decade counters is 1 through 10.
E. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.
F. t_r and t_f ≤ 7 ns.
G. V_{ref} is 1.5 V for '192 and '193, 1.3 V for 'LS192 and 'LS193.

FIGURE 2B – PROPAGATION DELAY TIMES

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9558401QEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9558401QE A SNJ54192J	Samples
5962-9558401QFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9558401QF A SNJ54192W	Samples
5962-9558401QFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9558401QF A SNJ54192W	Samples
76006012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	76006012A SNJ54LS 193FK	Samples
76006012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	76006012A SNJ54LS 193FK	Samples
7600601EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7600601EA SNJ54LS193J	Samples
7600601EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7600601EA SNJ54LS193J	Samples
7600601FA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7600601FA SNJ54LS193W	Samples
7600601FA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7600601FA SNJ54LS193W	Samples
JM38510/31508B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31508B2A	Samples
JM38510/31508B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31508B2A	Samples
JM38510/31508BEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31508BEA	Samples
JM38510/31508BEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31508BEA	Samples
JM38510/31508BFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31508BFA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/31508BFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31508BFA	Samples
JM38510/31508SFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31508SFA	Samples
JM38510/31508SFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31508SFA	Samples
M38510/31508B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31508B2A	Samples
M38510/31508B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31508B2A	Samples
M38510/31508BEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31508BEA	Samples
M38510/31508BEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31508BEA	Samples
M38510/31508BFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31508BFA	Samples
M38510/31508BFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31508BFA	Samples
M38510/31508SFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31508SFA	Samples
M38510/31508SFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31508SFA	Samples
SN54192J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54192J	Samples
SN54192J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54192J	Samples
SN54LS193J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS193J	Samples
SN54LS193J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS193J	Samples
SN74LS193DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS193	Samples
SN74LS193DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS193	Samples
SN74LS193N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS193N	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS193N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS193N	Samples
SN74LS193NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS193N	Samples
SN74LS193NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS193N	Samples
SN74LS193NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS193	Samples
SN74LS193NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS193	Samples
SNJ54192J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9558401QE A SNJ54192J	Samples
SNJ54192J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9558401QE A SNJ54192J	Samples
SNJ54192W	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9558401QF A SNJ54192W	Samples
SNJ54192W	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9558401QF A SNJ54192W	Samples
SNJ54LS193FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	76006012A SNJ54LS 193FK	Samples
SNJ54LS193FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	76006012A SNJ54LS 193FK	Samples
SNJ54LS193J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7600601EA SNJ54LS193J	Samples
SNJ54LS193J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7600601EA SNJ54LS193J	Samples
SNJ54LS193W	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7600601FA SNJ54LS193W	Samples
SNJ54LS193W	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7600601FA SNJ54LS193W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS193, SN54LS193-SP, SN74LS193 :

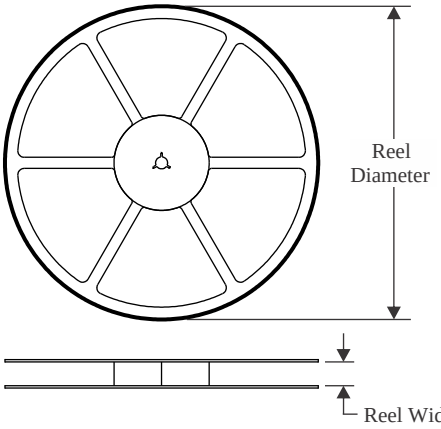
- Catalog : SN74LS193, SN54LS193
- Military : SN54LS193
- Space : SN54LS193-SP

NOTE: Qualified Version Definitions:

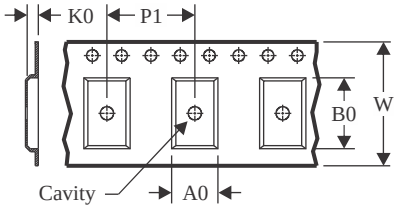
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

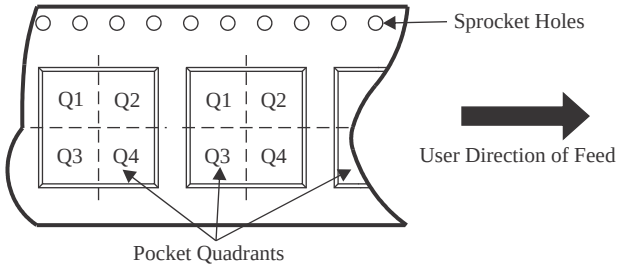


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

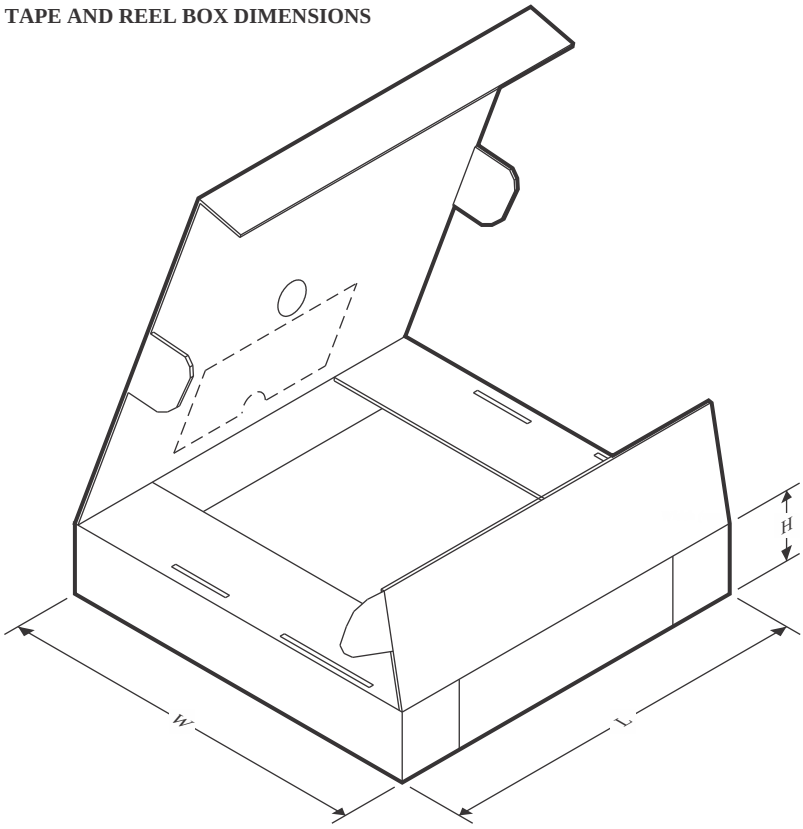
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS193DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS193NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS193NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

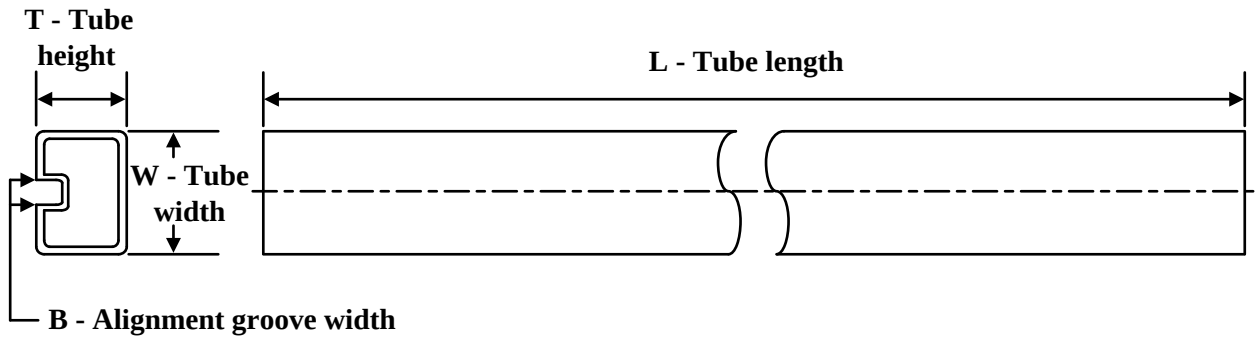
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS193DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LS193NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74LS193NSR	SO	NS	16	2000	356.0	356.0	35.0

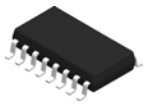
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9558401QFA	W	CFP	16	25	506.98	26.16	6220	NA
76006012A	FK	LCCC	20	55	506.98	12.06	2030	NA
76006012A	FK	LCCC	20	55	506.98	12.06	2030	NA
7600601FA	W	CFP	16	25	506.98	26.16	6220	NA
7600601FA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/31508B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/31508B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/31508BFA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/31508BFA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/31508SFA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/31508SFA	W	CFP	16	25	506.98	26.16	6220	NA
M38510/31508B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/31508B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/31508BFA	W	CFP	16	25	506.98	26.16	6220	NA
M38510/31508BFA	W	CFP	16	25	506.98	26.16	6220	NA
M38510/31508SFA	W	CFP	16	25	506.98	26.16	6220	NA
M38510/31508SFA	W	CFP	16	25	506.98	26.16	6220	NA
SN74LS193N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS193N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS193N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS193N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS193NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS193NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS193NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS193NE4	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54192W	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54192W	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54LS193FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS193FK	FK	LCCC	20	55	506.98	12.06	2030	NA

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SNJ54LS193W	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54LS193W	W	CFP	16	25	506.98	26.16	6220	NA

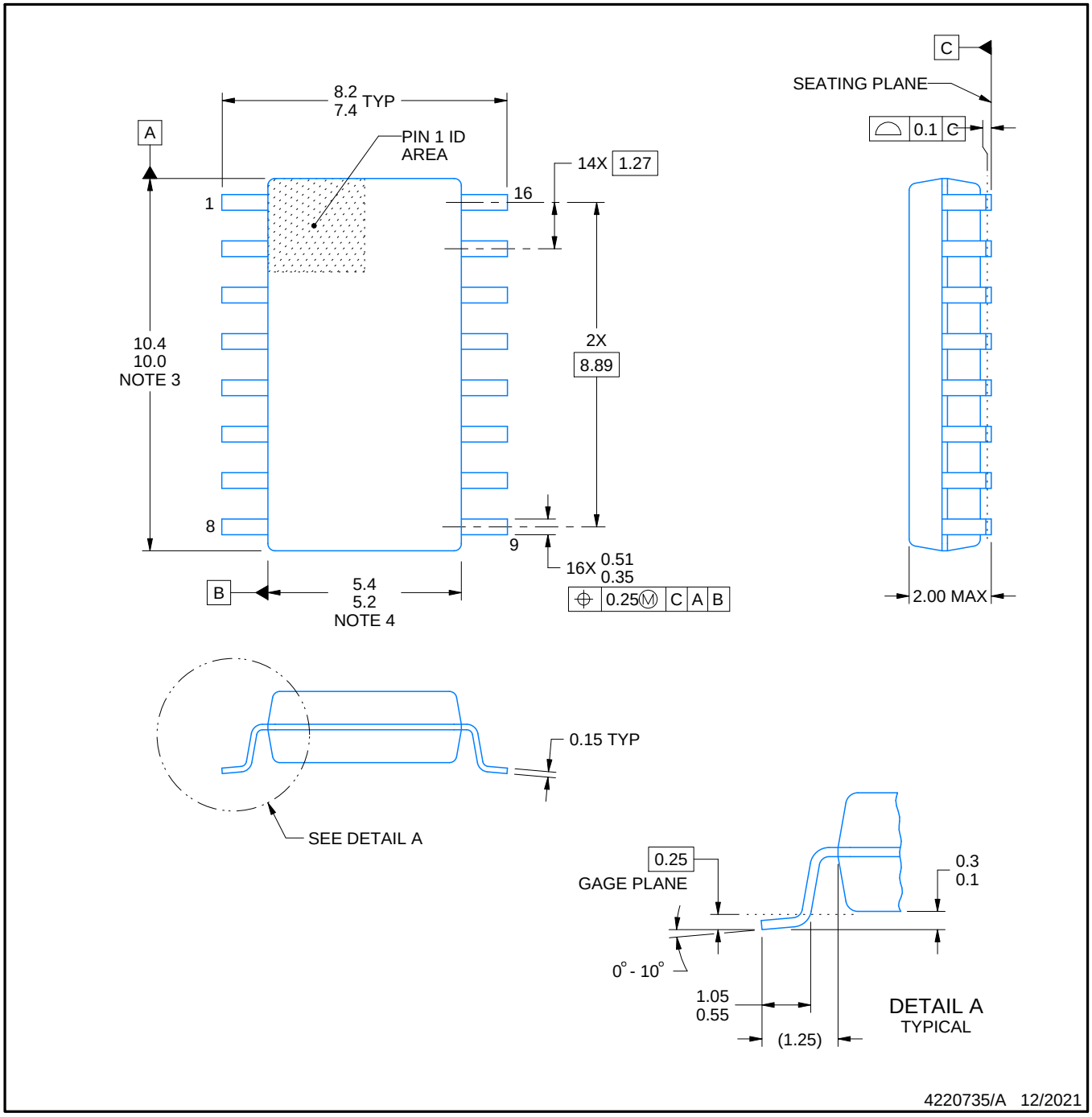


PACKAGE OUTLINE

NS0016A

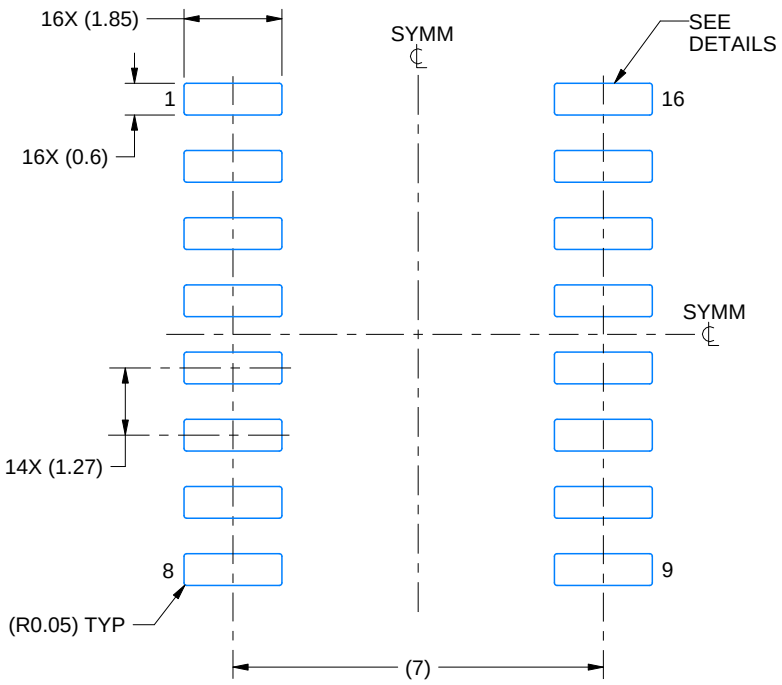
SOP - 2.00 mm max height

SOP

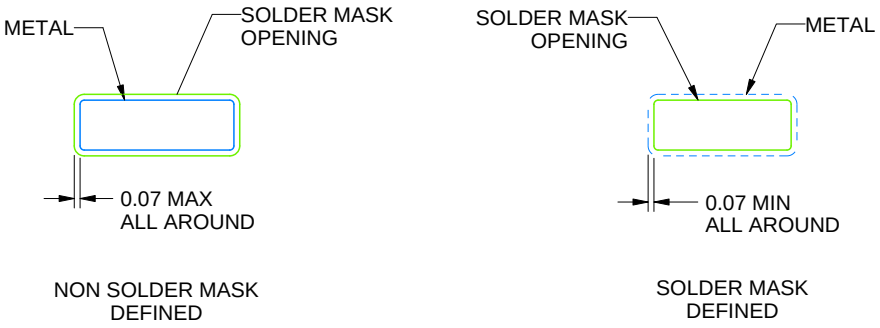


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

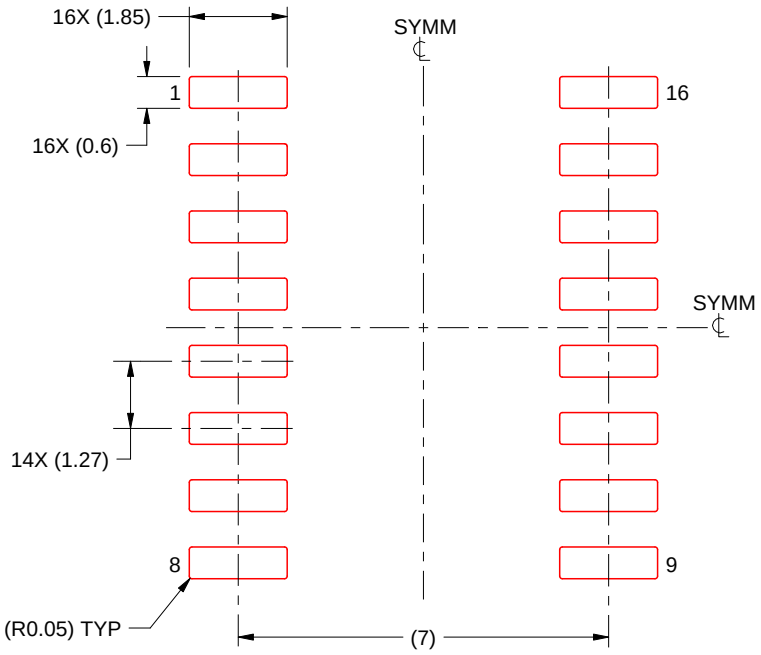
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



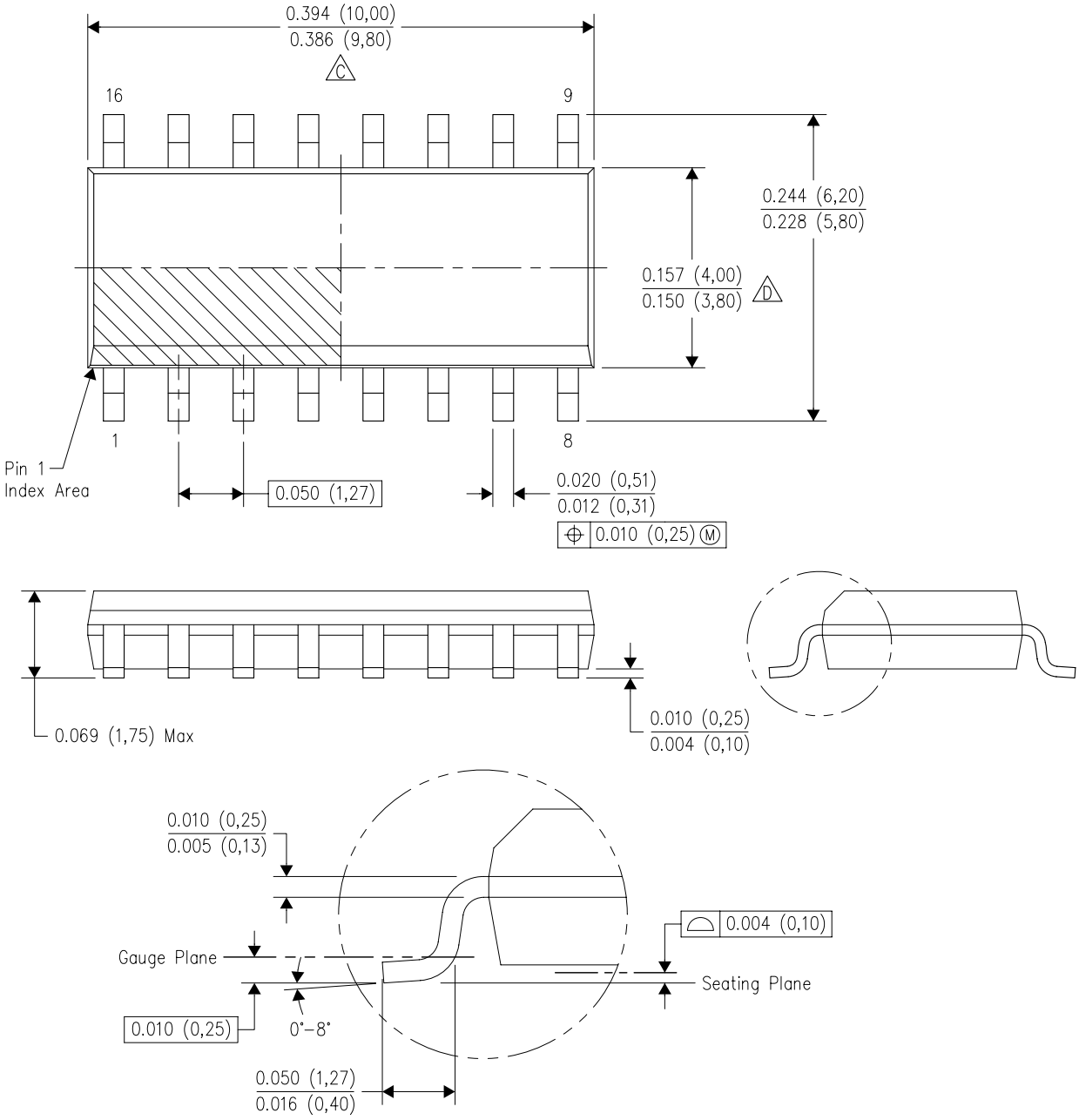
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

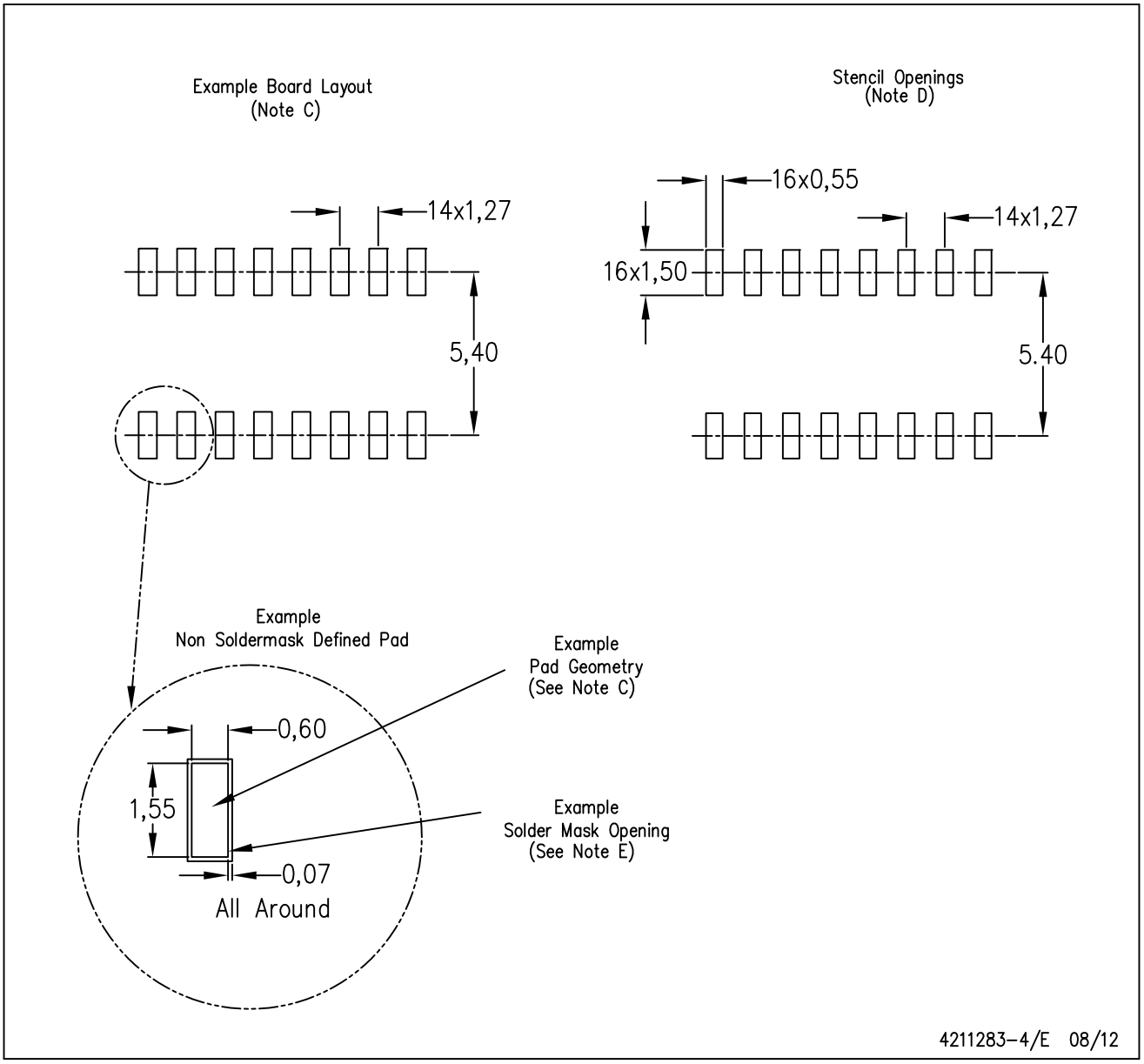
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

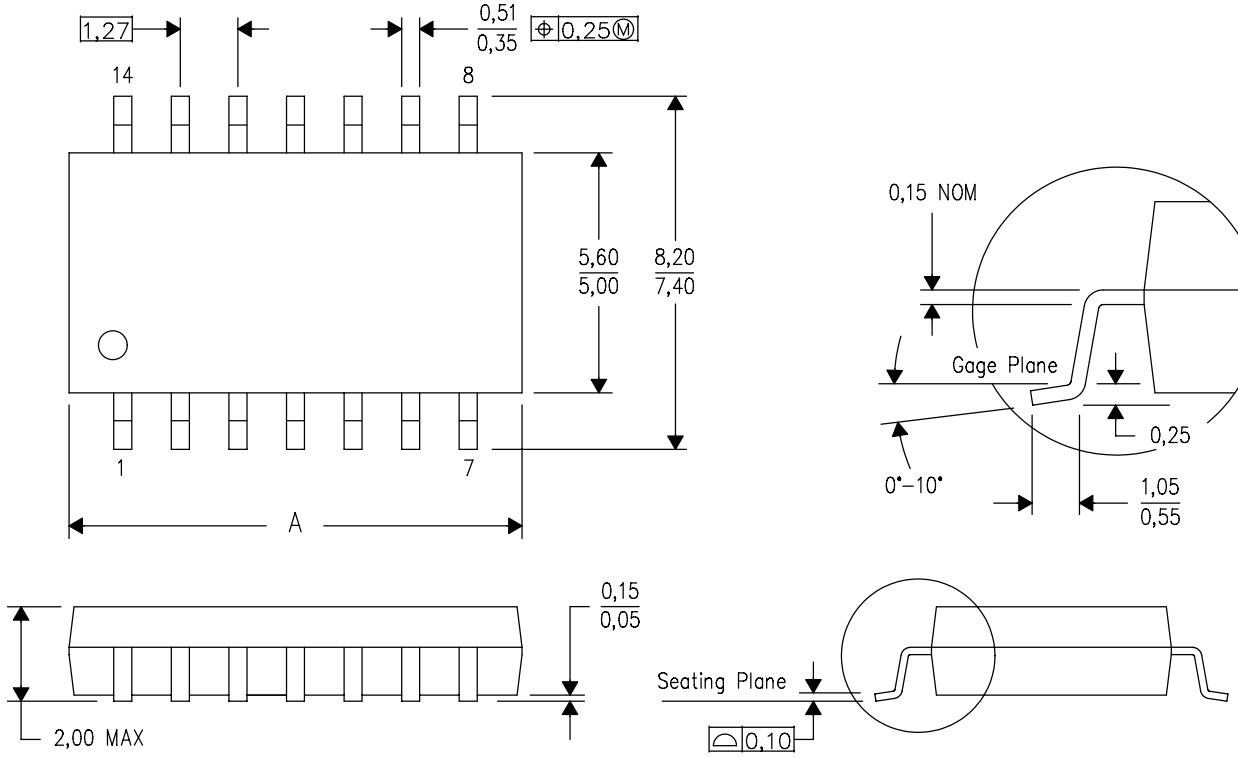


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

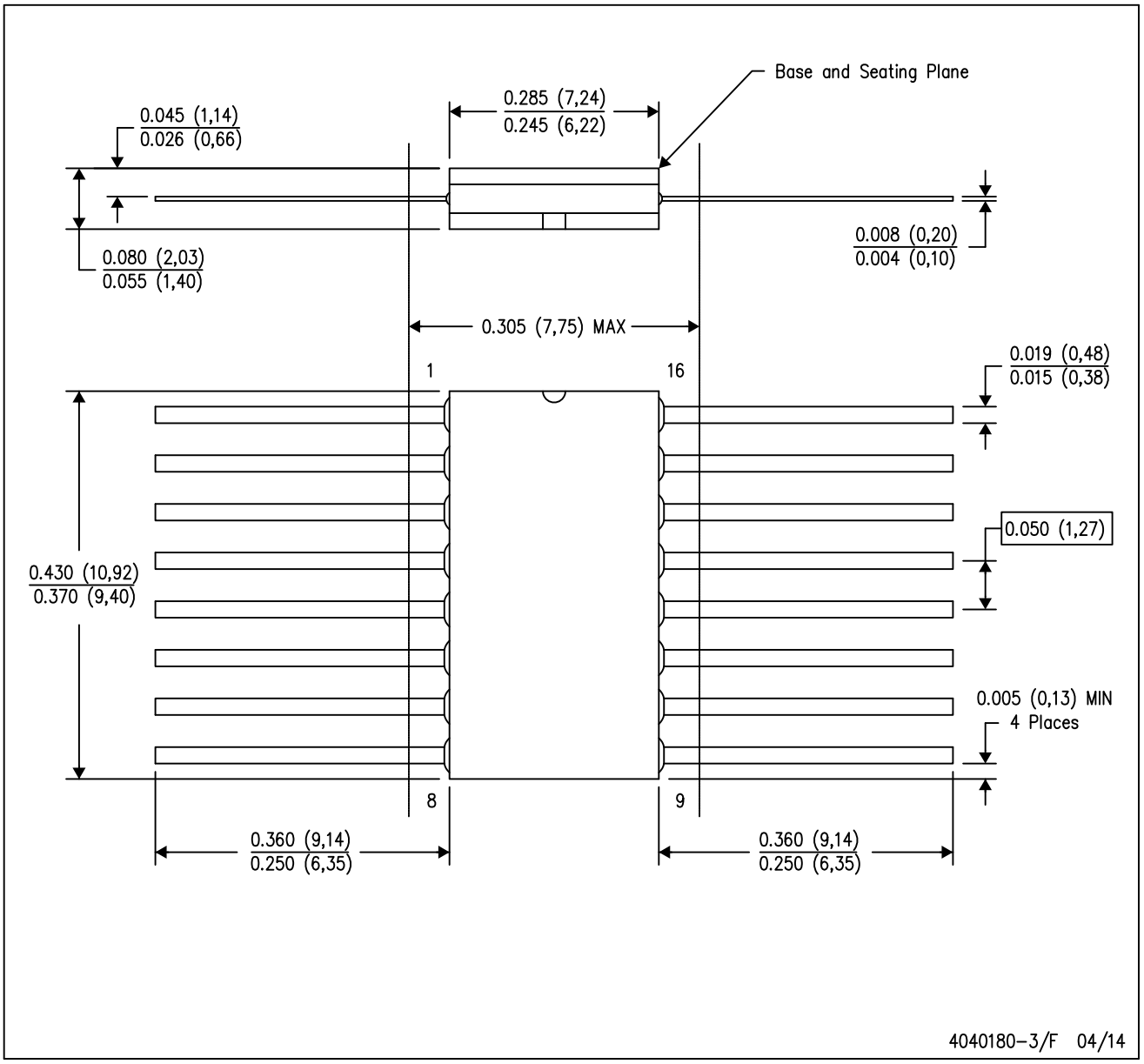


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

GENERIC PACKAGE VIEW

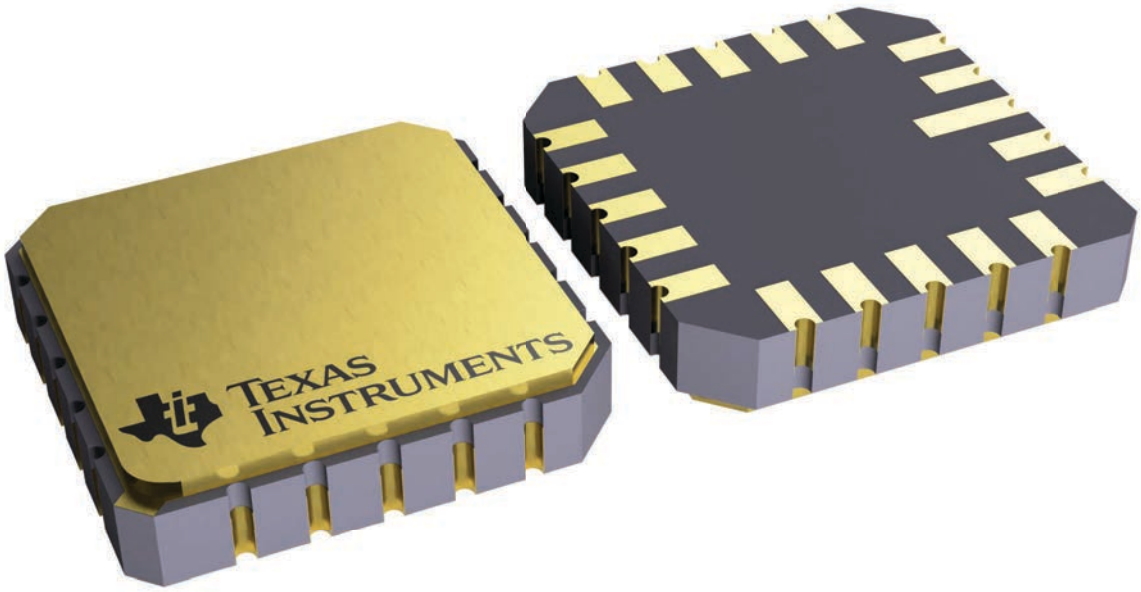
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

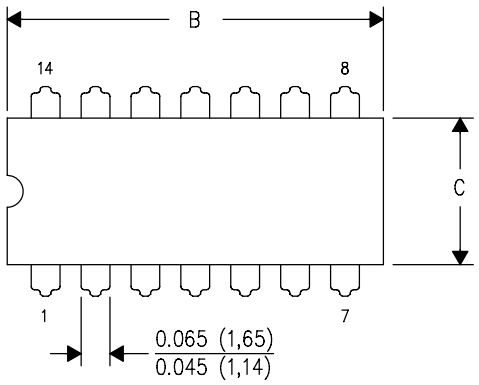


4229370VA\

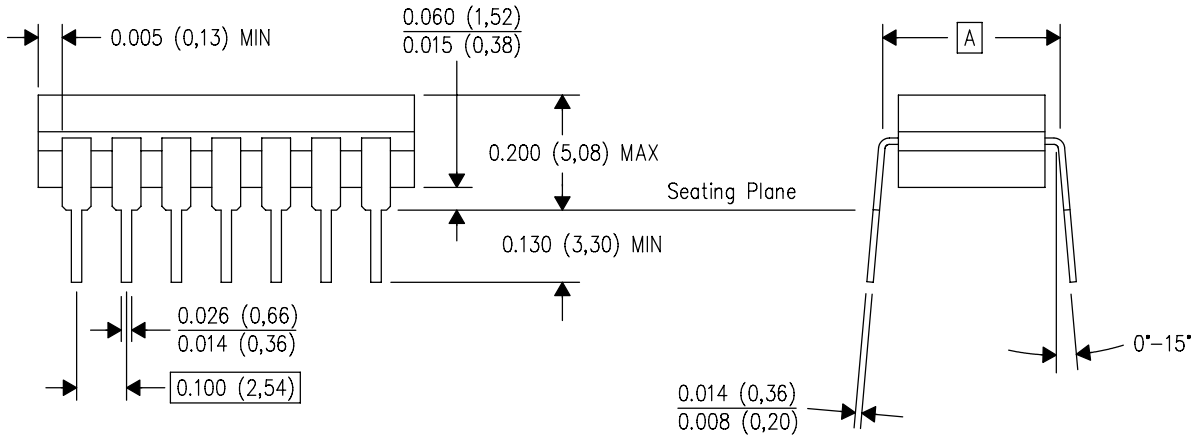
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



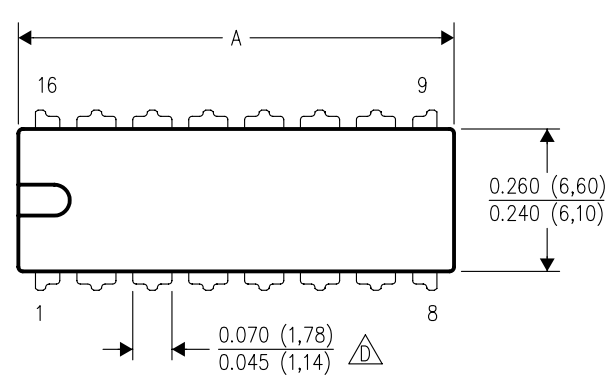
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

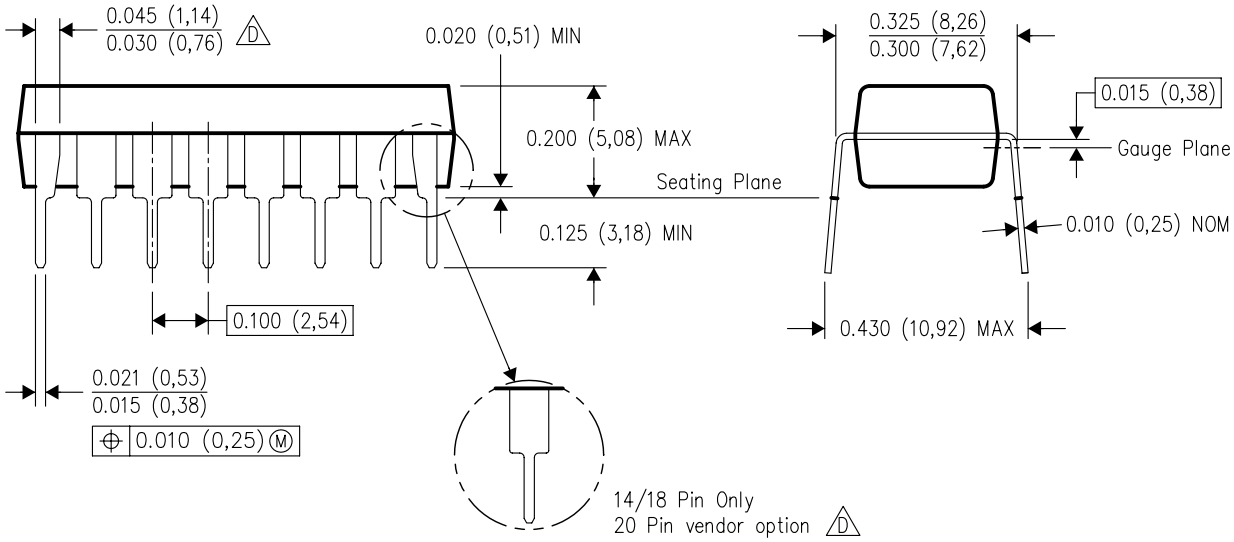
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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