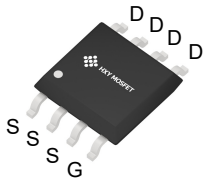
FDS6612A-NB5E029A

N-Channel Enhancement Mode MOSFET

Description

The FDS6612A-NB5E029A uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as . 4.5V This device is suitable for use as a Battery protection or in other Switching application.



SOP-8
(SOIC-8)

General Features

V_{DS} = 30V I_D = 9A

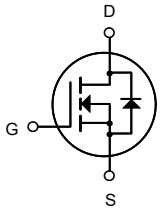
$R_{DS(ON)}$ < 20mΩ @ V_{GS}=10V

Application

Battery protection

Load switch

Uninterruptible power supply



N-Channel MOSFET

Ordering Information

Product ID	Pack	Brand	Qty(PCS)
FDS6612A-NB5E029A	SOP-8(SOIC-8)	HXY MOSFET	3000

Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Continuous Drain Current	9	A
I_D@T_A=100℃	Continuous Drain Current	5.4	A
I_{DM}	Pulsed Drain Current	30	A
EAS	Single Pulse Avalanche Energy	20	mJ
I_{AS}	Avalanche Current	20	A
P_D@T_A=25℃	Total Power Dissipation	3.1	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{\theta JA}$	Thermal Resistance Junction-ambient[1](t≤10s)	113	℃/W
	Thermal Resistance Junction-ambient	25	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Sourtce Breakdown Voltage	V_{GS}=0V,I_D=250μA	30	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS}=0V, V_{DS}=30V	---	---	1	μA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V, V_{DS}=0A	---	---	±100	nA
$V_{GS(th)}$	GATE-Source Threshold Voltage	V_{GS}=V_{DS}, I_D=250μA	1.2	1.7	2.2	V
$R_{DS(ON)}$	Drain-Source On Resistance[4]	V_{GS}=10V,I_D=5.5A	---	16	20	mΩ
		V_{GS}=4.5V,I_D=4.5A	---	24	30	mΩ
C_{iss}	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz	---	484	---	pF
C_{oss}	Output Capacitance		---	68	--	
C_{rss}	Reverse Transfer Capacitance		---	52	---	
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=15V, I_D=5A, R_{ENG}=3Ω,V_{GS}=10V	---	3	---	ns
t_r	Rise Time		---	10	---	ns
$t_{d(off)}$	Turn-Off Delay Time		---	13	---	ns
t_f	Fall Time		---	1	---	ns
Q_g	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=5A	---	9	---	nc
Q_{gs}	Gate-Source Charge		---	1	---	nc
Q_{gd}	Gate-Drain “Miller” Charge		---	1	---	nc
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_{SD}=5.8A	---	---	1.2	V
I_S	Continuous Drain Curren	VD=VG=0V	---	---	9	A
I_{SM}	Pulsed Drain Current		---	---	30	A
Trr	Reverse Recovery Time	I_F=5A,T_J=25℃dI/dt=100A/us	---	7.5	---	ns
Qrr	Reverse Recovery Charge		---	2	---	nc

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2. RθJA is measured with the device mounted on a 1inch2 pad of 2oz copper FR4 PCB
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%.

Typical Characteristics

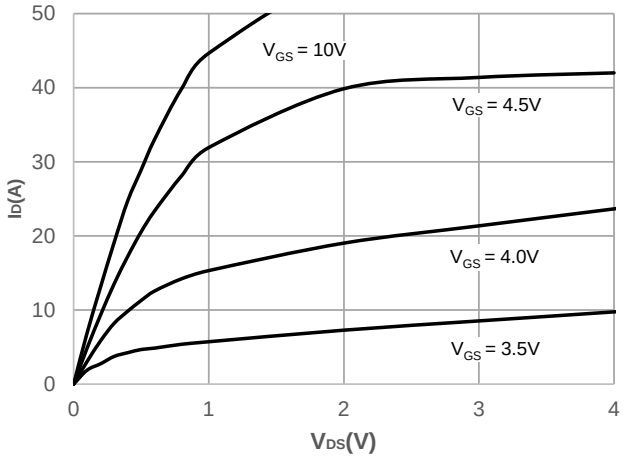


Figure 1: Output Characteristics

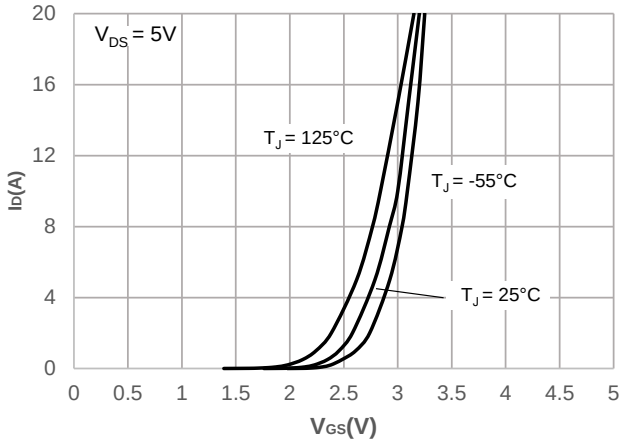


Figure 2: Typical Transfer Characteristics

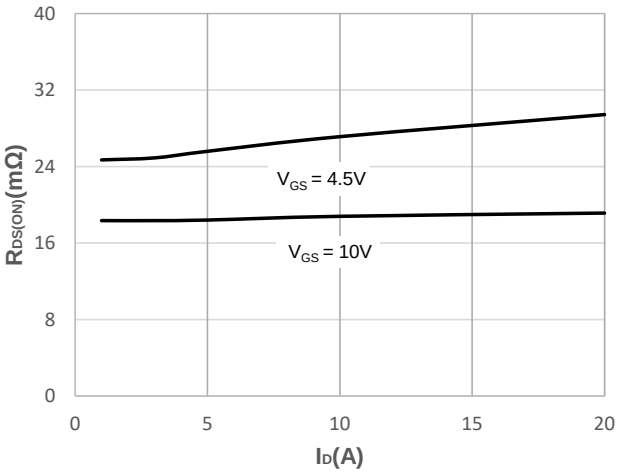


Figure 3: On-resistance vs. Drain Current

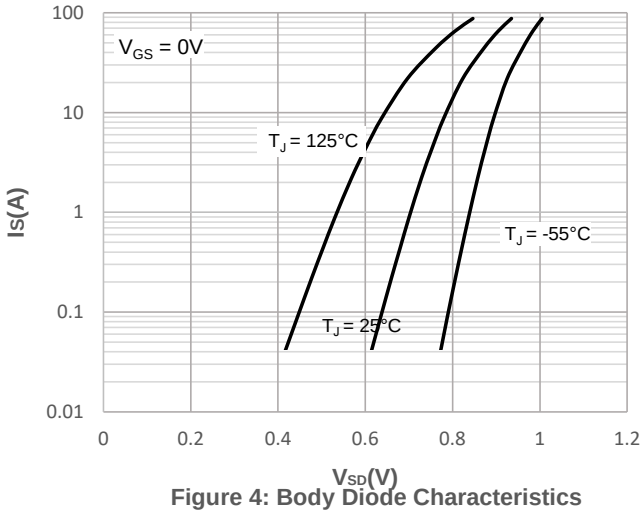


Figure 4: Body Diode Characteristics

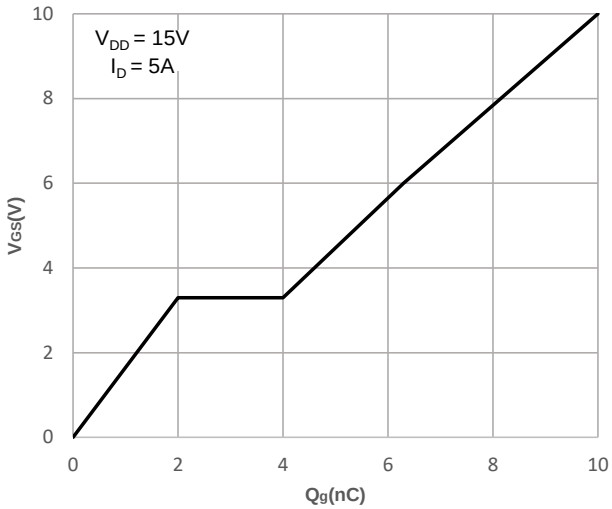


Figure 5: Gate Charge Characteristics

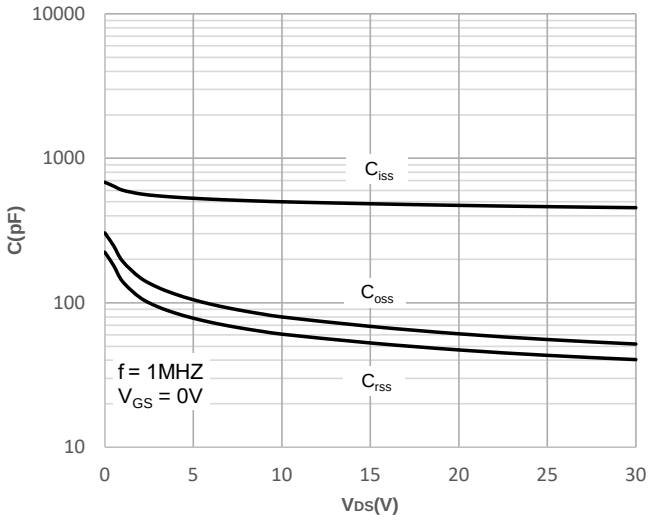


Figure 6: Capacitance Characteristics

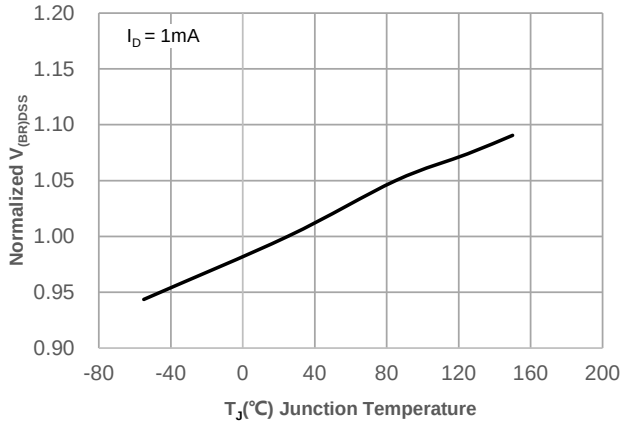


Figure 7: Normalized Breakdown voltage vs. Junction Temperature

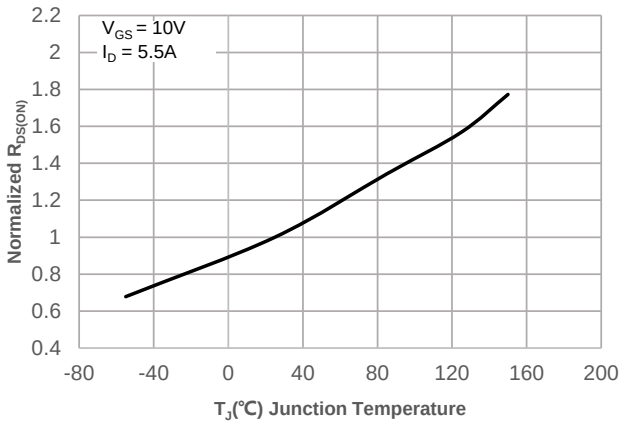


Figure 8: Normalized on Resistance vs. Junction Temperature

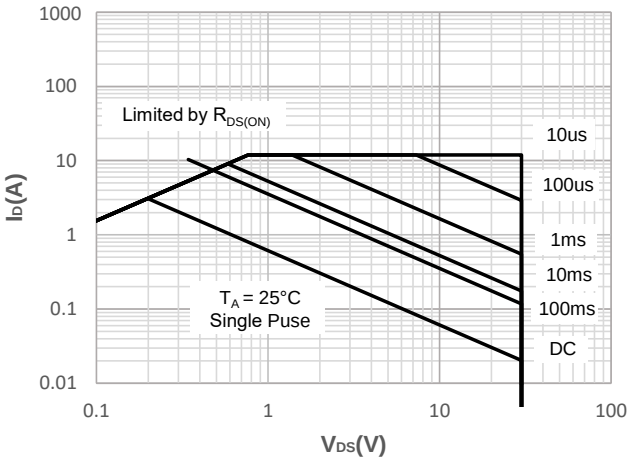


Figure 9: Maximum Safe Operating Area

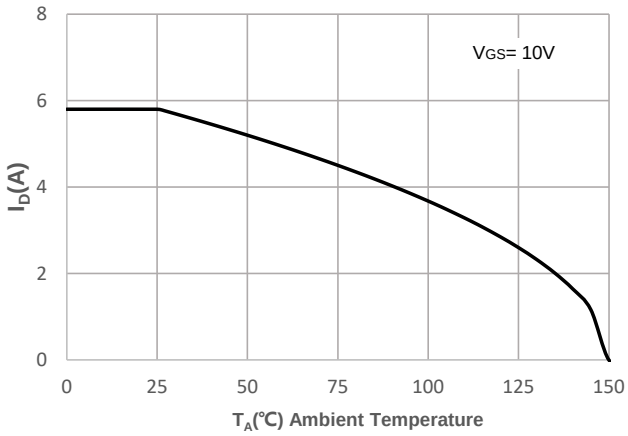


Figure 10: Maximum Continuous Drian Current vs. Ambient Temperature

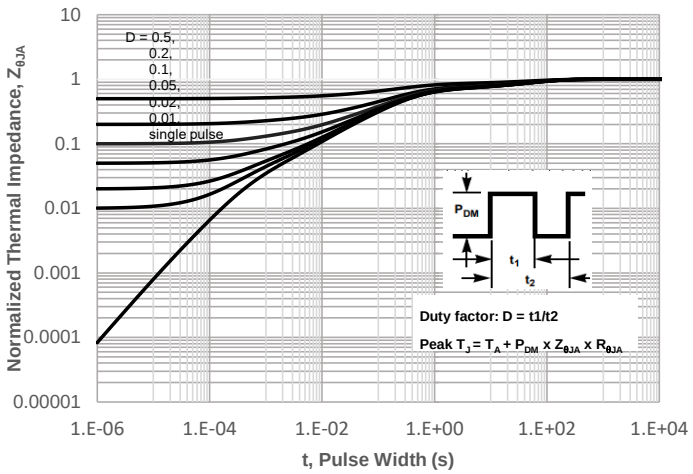


Figure 11: Normalized Maximum Transient Thermal Impedance

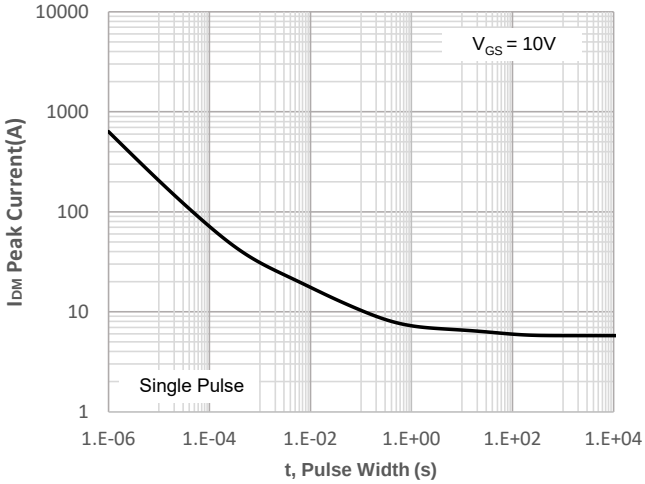
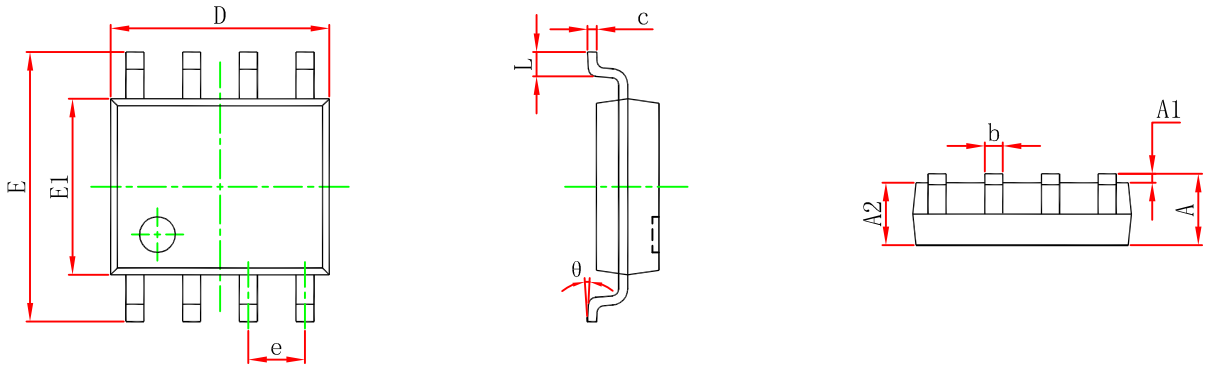
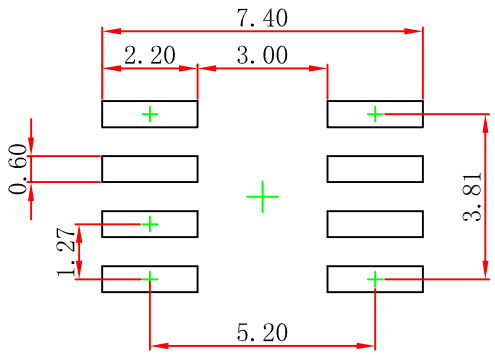


Figure 12: Peak Current Capacity

SOP-8(SOIC-8) Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

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