

钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65ALS1176

差分总线收发器

网址 www.sztdbdt.com

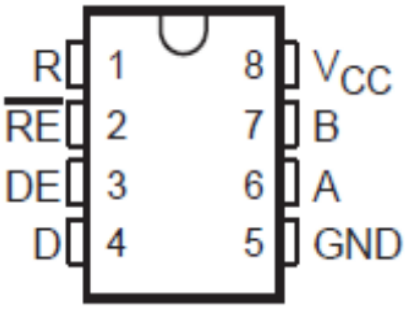
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

特性

●符合或超出 TIA/EIA-422-B、TIA/EIA-485-A 和 ITU 建议 V.11 和 X.27 的要求
●在高达 35MBaud 的数据速率下运行
●工作温度范围：－25 ° C 至 85 ° C
●适用于嘈杂环境中的长距离总线线路上的多点传输
●低电源电流要求：30 mA（最大值）
●宽正负输入/输出总线电压范围
● 热关断保护
●驱动器正负电流限制
●接收器输入迟滞
●无干扰上电和断电保护
●接收器开路失效防护设计
●封装选项包括塑料小外形尺寸 (D) 封装和 (P) 突降



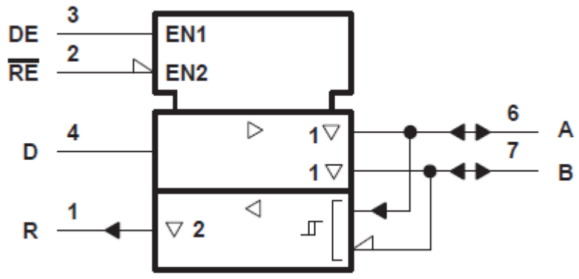
D Package (Top View)

应用

●PROFIBUS

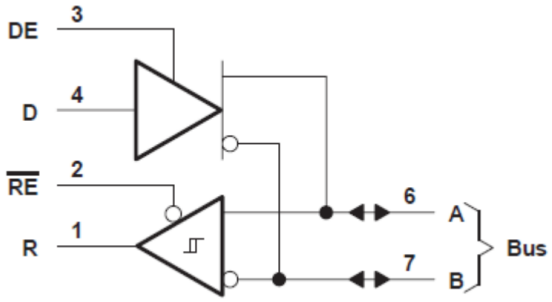
说明

SN65ALS1176 差分总线收发器旨在实现多点总线传输 线路上的双向数据通信。该器件专为平衡传输线路而设 计，符合 TIA/EIA-422-B 和 TIA/EIA-485-A 以及 ITU 建议 V.11 和 X.27。
SN65ALS1176 将一个三态差分线路驱动器和一个差分 输入线路接收器组合在一起，这两个器件由一个 5V 单电源供电。驱动器和接收器分别具有高电平有效和低电 平有效使能端，它们可以在外部连接在一起以用作方向 控制。驱动器差分输出端和接收器差分输入端在内部连 接以形成差分输入/输出 (I/O) 总线端口，这些端口用于 在禁用驱动器或 Vcc = 0 时为总线提供最小负载。该端 口具有正负宽共模电压范围，使得该器件非常适用于合 用线应用。
SN65ALS1176 的额定工作温度范围是 －25 ° C 至 85 ° C。



A. 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。

逻辑符号



逻辑图（正逻辑）

表 **5-1. Pin Functions**

NO	Name	Type	Description
1	R	O	Receive data output
2	$\overline{RE}$	I	Receiver enable, active low
3	DE	I	Driver enable, active high
4	D	I	Driver data input
5	GND	GND	Local device ground
6	A	I/O	Driver output or receiver input (complementary to B)
7	B	I/O	Driver output or receiver input (complementary to A)
8	V_{CC}	SUPPLY	4.75-V to 5.25-V supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		7	V
	Voltage range at any bus terminal	-7	12	V
V_I	Enable input voltage		5.5	V
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds)		260	℃
T_{stg}	Storage temperature range	-65	150	℃

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

(2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

6.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_I or V_{IC}	Input voltage at any bus terminal (separately or common mode)				12	V
					-7	
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage(1)				± 12	V
I_{OH}	High-level output current	Driver			-60	mA
		Receiver			-400	μA
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_A	Operating free-air temperature		-25		85	°C

(1) Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

6.3 Thermal Information

THERMAL METRIC(1)		D (SOIC) 8-Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case thermal resistance	56.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.4 Electrical Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = − 18 mA				− 1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω	See 图 7-1	½ V_{OD1} or 2(3)			V
		R_L = 54 Ω	See 图 7-1	2.1	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = − 7 V to 12 V	See 图 7-2	1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(4)	R_L = 54 Ω or 100 Ω	See 图 7-1			± 0.2	V
V_{OC}	Common-mode output voltage					3 − 1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(4)					± 0.2	V
I_O	Output current	Outputs disabled(6)	V_O = 12 V			1	mA
			V_O = − 7 V			− 0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				− 400	μA
I_{OS}	Short-circuit output current(5)	V_O = − 4 V				− 250	mA
		V_O = 0				− 150	
		V_O = V_{CC}				250	
		V_O = 8 V				250	
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

(1) The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
(4) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from one logic state to the other.
(5) Duration of the short circuit should not exceed one second for this test.
(6) This applies for both power on and power off; refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal

6.5 Switching Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω See 图 7-3	C_L = 50 pF,			15	ns
$t_{sk(p)}$	Pulse skew(2)				0	2	ns
$t_{t(OD)}$	Differential output transition time				8		ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω See 图 7-4	C_L = 50 pF,			80	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω See 图 7-5	C_L = 50 pF,			30	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω See 图 7-4	C_L = 50 pF,			50	ns

6.5 Switching Characteristics - Driver (continued)

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLZ}	Output disable time from low level	R_L = 110 Ω See 图 7-5	C_L = 50 pF,			30	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C
(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

6.6 Symbol Equivalents

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$	None	V_t (test termination measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|V_t\|\|$	$\|\|V_t\| - \|V_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - V_{os}\|$	$\|V_{os} - V_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	None
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

6.7 Electrical Characteristics - Receiver

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = – 0.4 mA			0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	– 0.2(2)			V
V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-})				60		mV
V_{IK}	Enable-input clamp voltage	I_I = – 18 mA				– 1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, SeeFigure 6	I_{OH} = – 400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = – 200 mV, See 图 7-6	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				± 20	μA
V_I	Line input current	Other input = 0 V(3)	V_I = 12 V			1	mA
			V_I = – 7 V			– 0.8	
I_{IH}	High-level-enable input current	V_{IH} = 2.7 V				20	mμA
I_{IL}	Low-level-enable input current	V_{IL} = 0.4 V				– 100	μA
r_I	Input resistance			12	20		kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0	– 15		– 85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

6.8 Switching Characteristics - Receiver

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation time	V_{ID} = – 1.5 V to 1.5 V, See 图 7-7	C_L = 15 pF,			25	ns
$t_{sk(p)}$	Pulse skew(2)				0	2	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See 图 7-8		11	18	ns
t_{PZL}	Output enable time to low level				11	18	ns
t_{PHZ}	Output disable time from high level					50	ns
t_{PLZ}	Output disable time from low level					30	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

7 Parameter Measurement Information

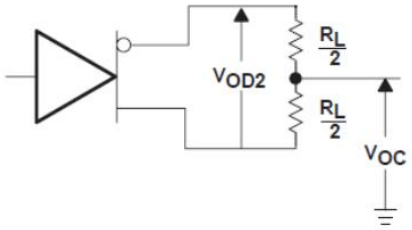


图 7-1. Driver V_{OD2} and V_{OC} Test Circuit

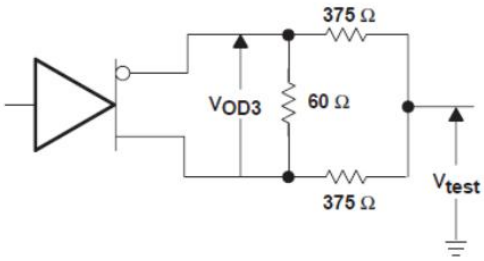
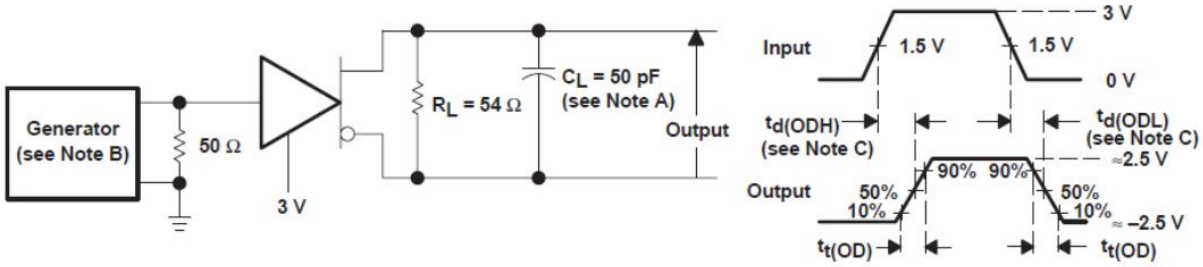


图 7-2. Driver V_{OD3} Test Circuit



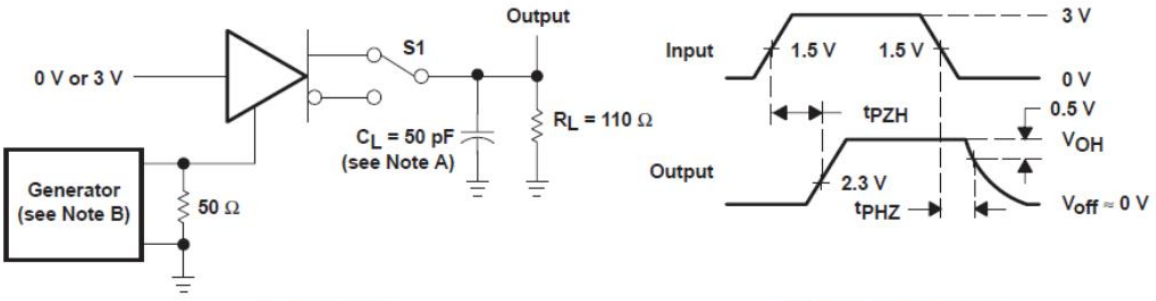
TEST CIRCUIT VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.

C. $t_{d(OD)} = t_{d(ODH)}$ or $t_{d(ODL)}$.

图 7-3. Driver Differential-Output Delay and Transition Times

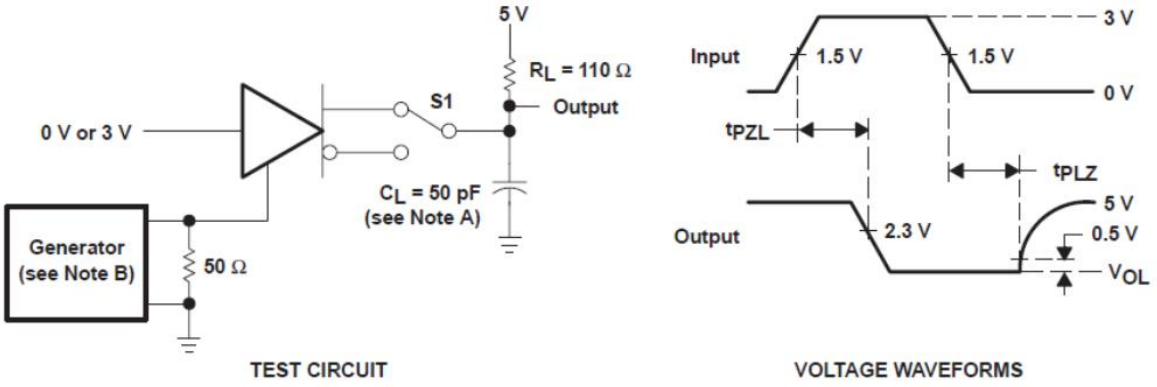


TEST CIRCUIT VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

图 7-4. Driver Enable and Disable Times



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

图 7-5. Driver Enable and Disable Times

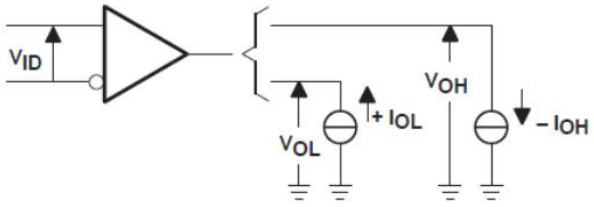
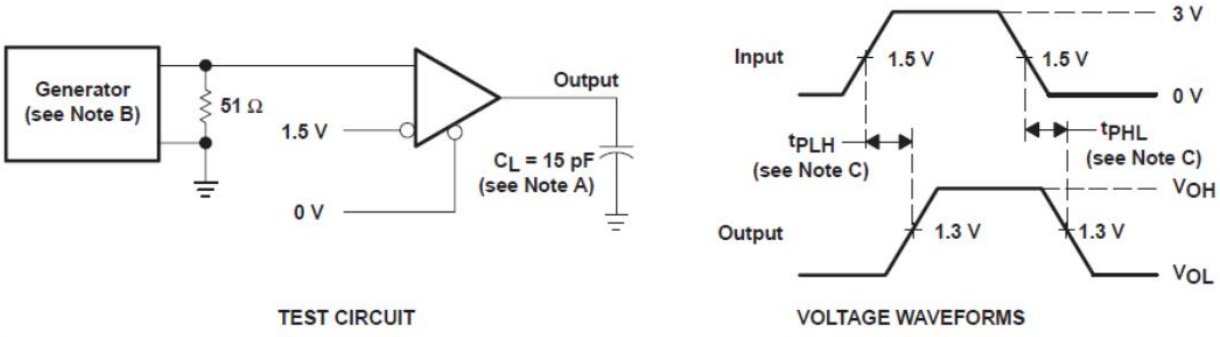


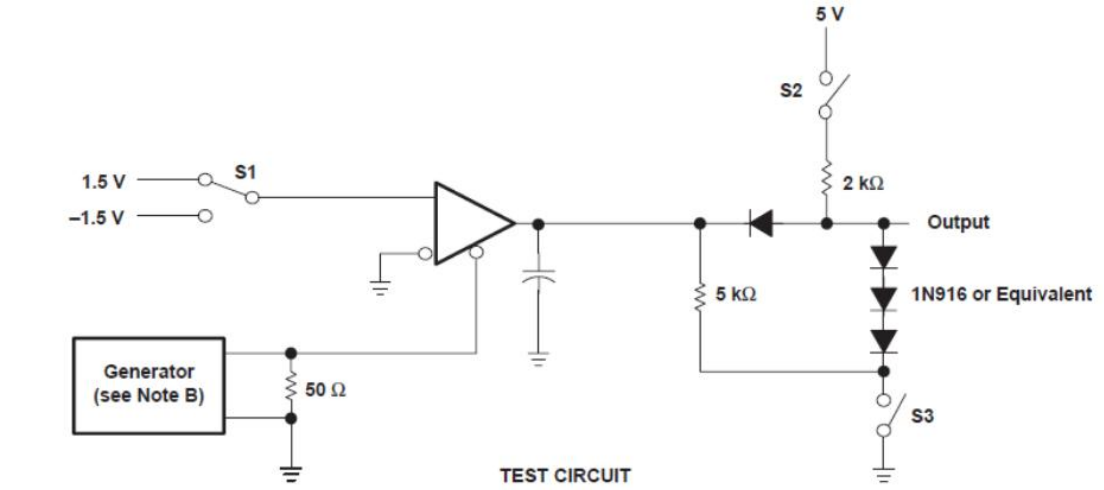
图 7-6. Receiver V_{OH} and V_{OL} Test Circuit



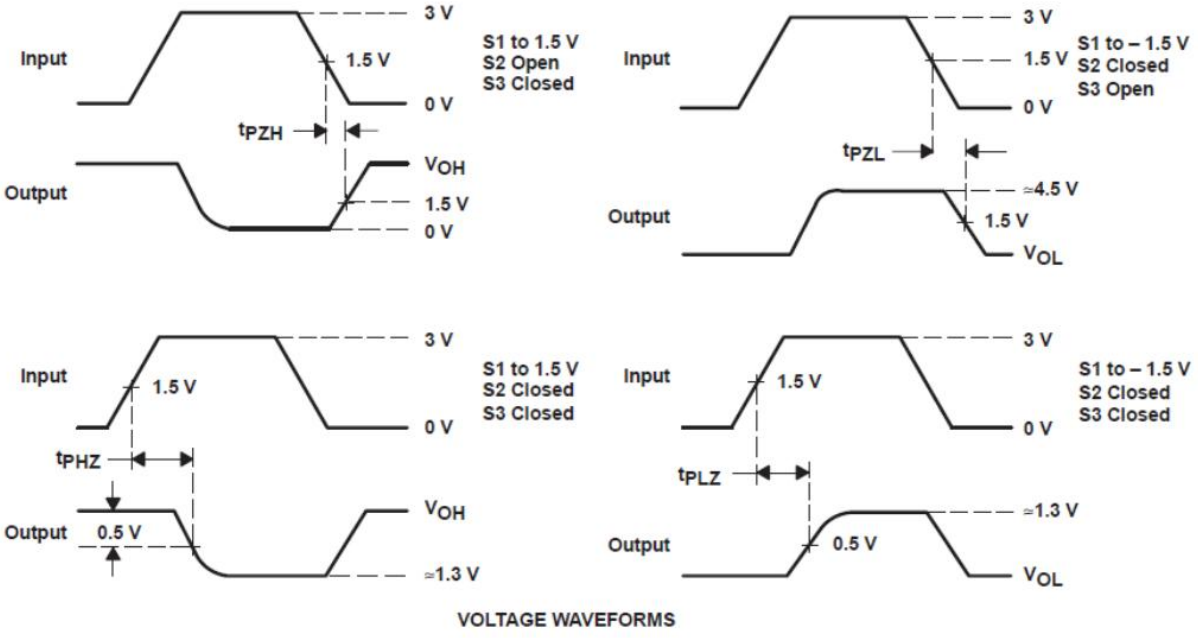
A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

C. $t_{pd} = t_{PLH}$ or t_{PHL}.



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.

8 Detailed Description

8.1 Functional Block Diagram

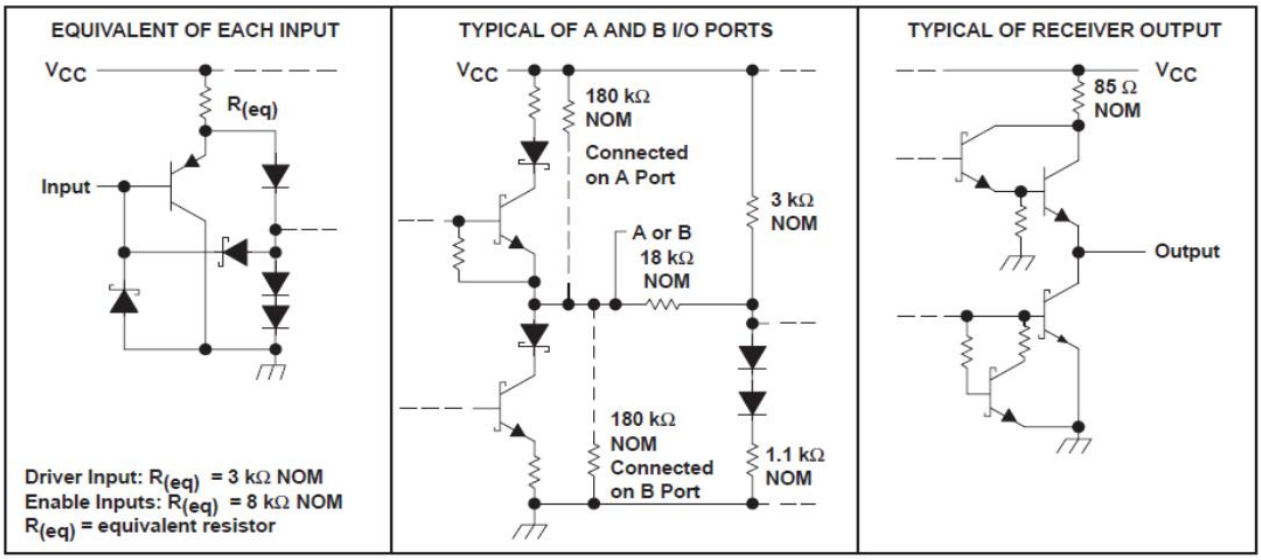


图 8-1. Schematics of Inputs and Outputs

8.2 Device Functional Modes

Function Tables

表 8-1. Driver(1)

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off).

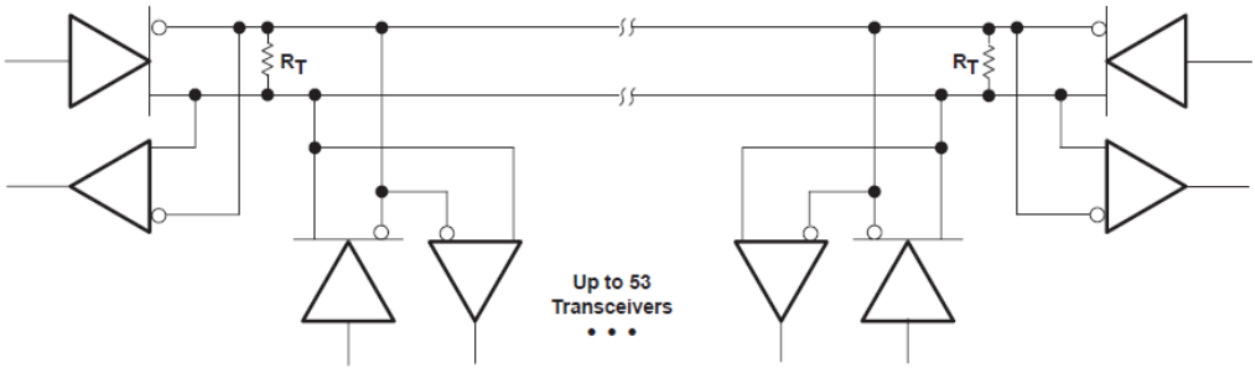
表 8-2. Receiver(1)

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
– 0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq$ – 0.2 V	L	L
X	H	Z
Inputs open	L	H

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off).

9.1 Application Information

9.1.1 Typical Application



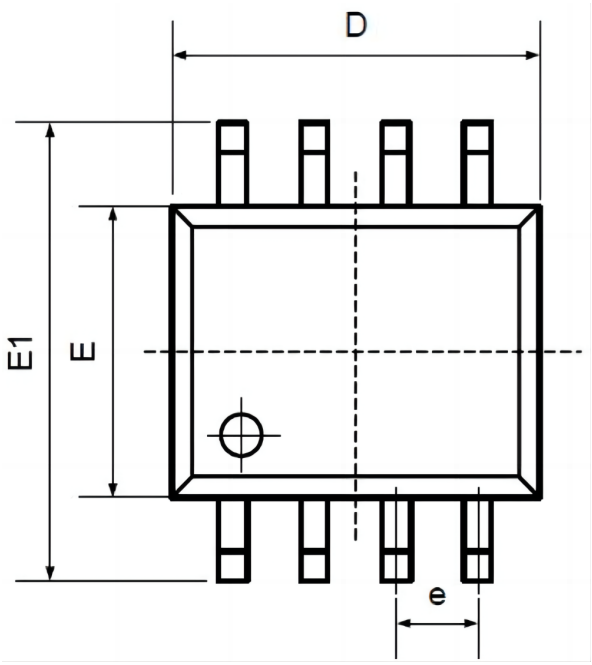
A. The line should terminate at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

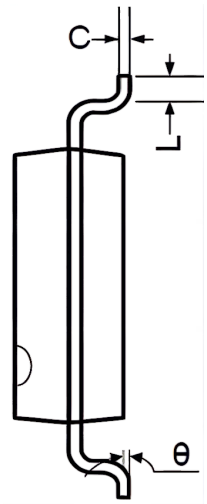
图 9-1. Typical Application Circuit

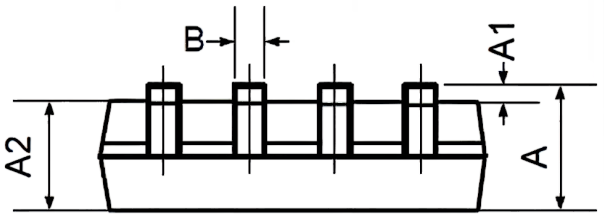
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65ALS1176DR-TUDI	SOP8	Tape,Reel,2500	SN65ALS1176DR

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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