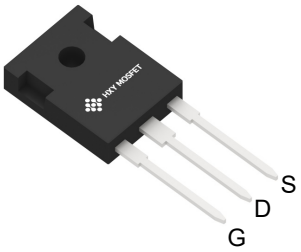
UF3C120080K3S

SiC Power MOSFET N-Channel Enhancement Mode

Features

- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Resistant to Latch-Up
- Halogen Free, RoHS Compliant



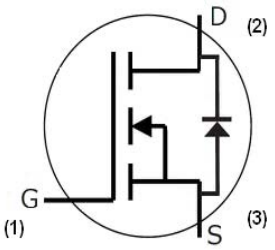
TO-247

Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

Applications

- Solar Inverters
- Switch Mode Power Supplies
- High Voltage DC/DC converters
- Battery Chargers
- Motor Drives
- Pulsed Power Applications



Part Number	Package	Qty(PCS)
UF3C120080K3S	TO-247	30

Maximum Ratings (T_C = 25 ˚C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1200	V	V_{GS} = 0 V, I_D = 100 µA	
V_{GSmax}	Gate - Source Voltage	-10/+25	V	Absolute maximum values	
V_{GSop}	Gate - Source Voltage	-5/+20	V	Recommended operational values	
I_D	Continuous Drain Current	36	A	V_{GS} = 20 V, T_C = 25˚C	Fig. 19
		24		V_{GS} = 20 V, T_C = 100˚C	
$I_{D(pulse)}$	Pulsed Drain Current	80	A	Pulse width t_P limited by T_{jmax}	Fig. 22
P_D	Power Dissipation	192	W	T_C=25˚C, T_J = 150 ˚C	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +150	˚C		
T_L	Solder Temperature	260	˚C	1.6mm (0.063”) from case for 10s	
M_d	Mounting Torque	1 8.8	Nm lbf-in	M3 or 6-32 screw	

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, I_D = 100 µA	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.9	4	V	V_{DS} = V_{GS}, I_D = 5 mA	Fig. 11
			2.4		V	V_{DS} = V_{GS}, I_D = 5 mA, T_J = 150ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	100	µA	V_{DS} = 1200 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current			250	nA	V_{GS} = 20 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		80	98	mΩ	V_{GS} = 20 V, I_D = 20 A	Fig. 4, 5, 6
			144			V_{GS} = 20 V, I_D = 20A, T_J = 150ºC	
g_{fs}	Transconductance		10		S	V_{DS}= 20 V, I_{DS}= 20 A	Fig. 7
			9			V_{DS}= 20 V, I_{DS}= 20 A, T_J = 150ºC	
C_{iss}	Input Capacitance		1130		pF	V_{GS} = 0 V V_{DS} = 1000 V f = 1 MHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		92				
C_{rss}	Reverse Transfer Capacitance		7.5				
E_{oss}	C_{oss} Stored Energy		50		µJ		Fig. 16
E_{AS}	Avalanche Energy, Single Pluse		1		J	I_D = 20A, V_{DD} = 50V	Fig. 29
E_{ON}	Turn-On Switching Energy		523		µJ	V_{DS} = 800 V, V_{GS} = -5/20 V, I_D = 20A, $R_{G(ext)}$ = 2.5Ω, L= 156 µH	Fig. 25
E_{OFF}	Turn Off Switching Energy		72				
$t_{d(on)}$	Turn-On Delay Time		15		ns	V_{DD} = 800 V, V_{GS} = -5/20 V I_D = 20 A, $R_{G(ext)}$ = 2.5 Ω, R_L = 40 Ω, Timing relative to V_{DS} Per IEC60747-8-4 pg 83	Fig. 27
t_r	Rise Time		22				
$t_{d(off)}$	Turn-Off Delay Time		24				
t_f	Fall Time		14				
$R_{G(int)}$	Internal Gate Resistance		3.9		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		17		nC	V_{DS} = 800 V, V_{GS} = -5/20 V I_D = 20 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		29				
Q_g	Total Gate Charge		71				

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.3		V	V_{GS} = - 5 V, I_{SD} = 10 A	Fig. 8, 9, 10
		3.8		V	V_{GS} = - 5 V, I_{SD} = 10 A, T_J = 150 °C	
I_S	Continuous Diode Forward Current		36	A	T_C = 25˚C	Note 1
t_{rr}	Reverse Recover time	24		ns	V_{GS} = - 5 V, I_{SD} = 20 A, V_R = 800 V dif/dt = 1950 A/µs	Note 1
Q_{rr}	Reverse Recovery Charge	152		nC		
I_{rrm}	Peak Reverse Recovery Current	10		A		

Note (1): When using SiC Body Diode the maximum recommended V_{GS} = -5V

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.60	0.65	°C/W		Fig. 21
$R_{\theta JA}$	Thermal Resistance From Junction to Ambient		40			

Typical Performance

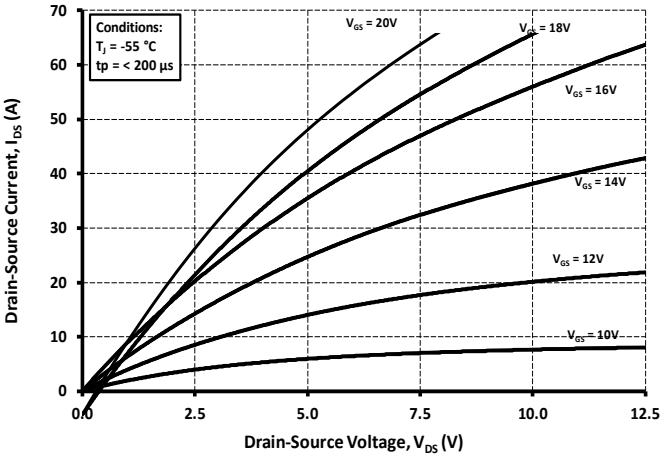


Figure 1. Output Characteristics T_J = -55 °C

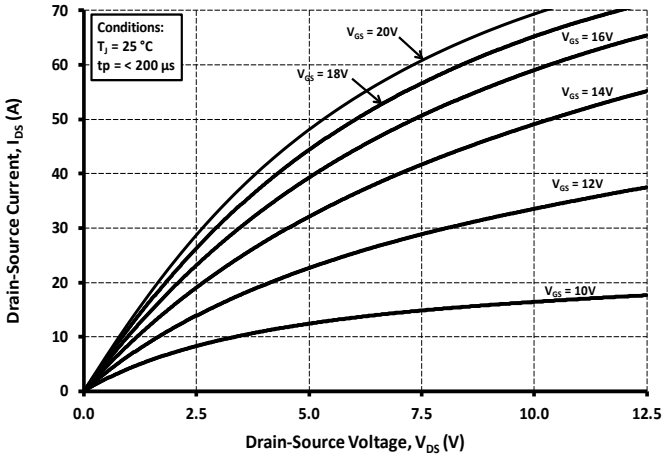


Figure 2. Output Characteristics T_J = 25 °C

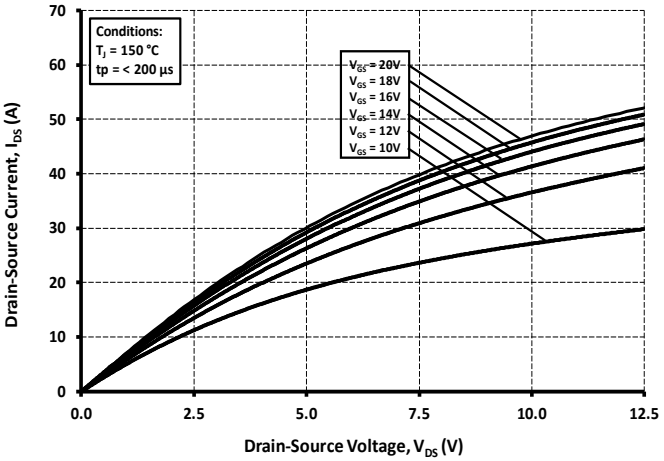


Figure 3. Output Characteristics T_J = 150 °C

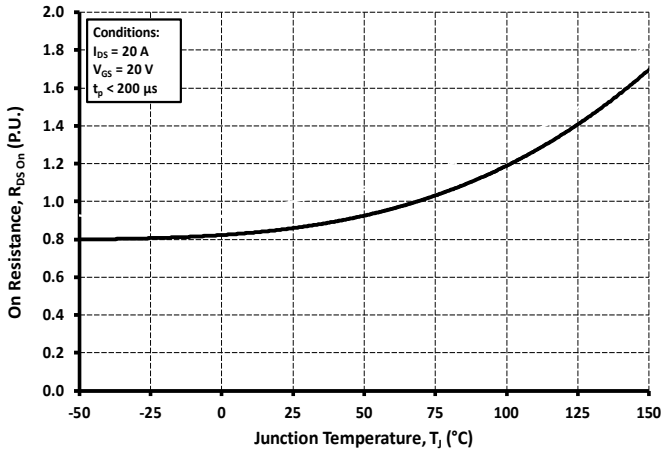


Figure 4. Normalized On-Resistance vs. Temperature

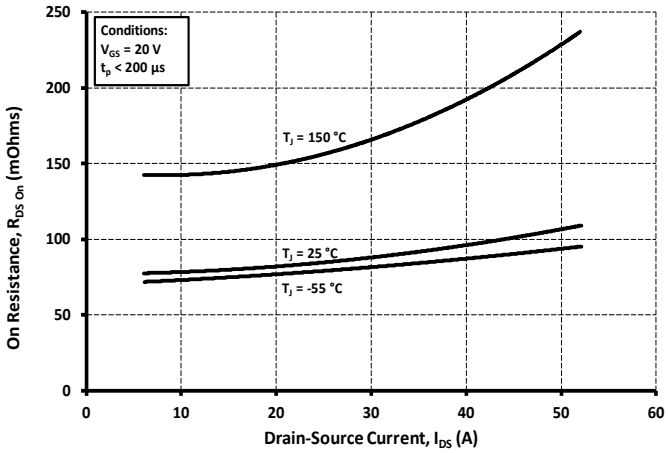


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

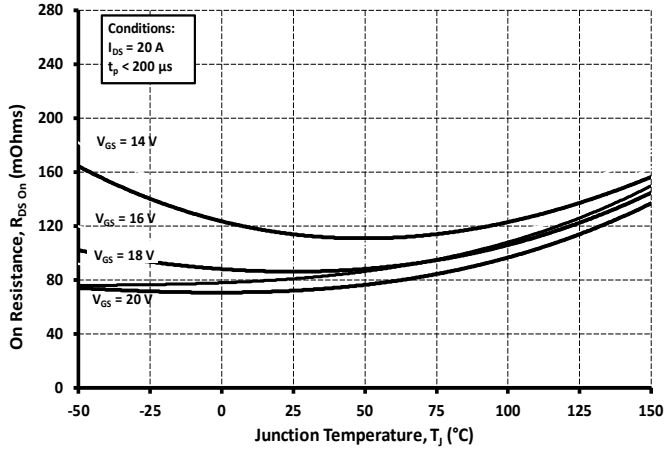


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

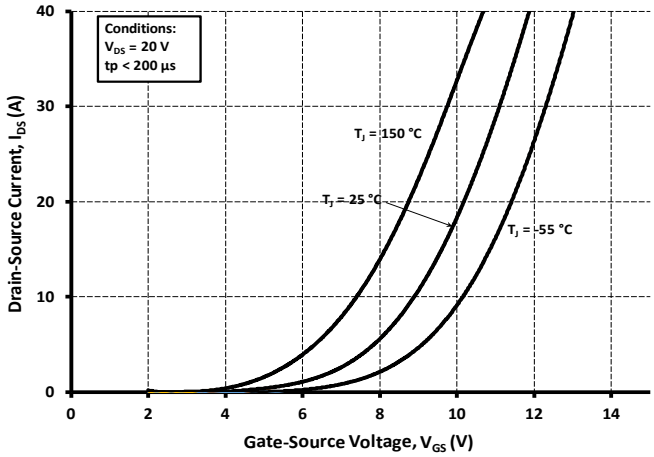


Figure 7. Transfer Characteristic for Various Junction Temperatures

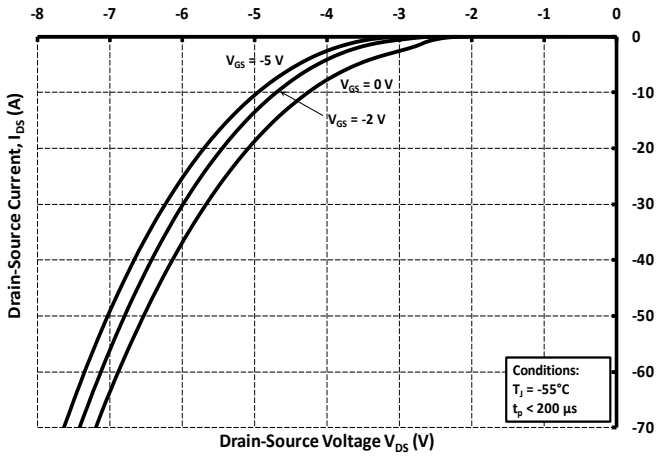


Figure 8. Body Diode Characteristic at -55 °C

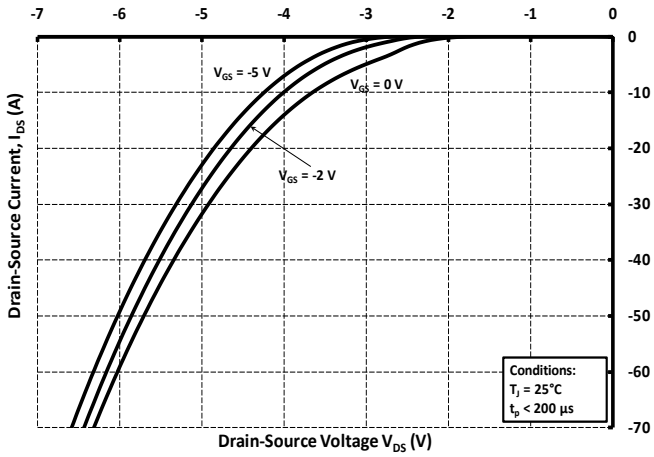


Figure 9. Body Diode Characteristic at 25 °C

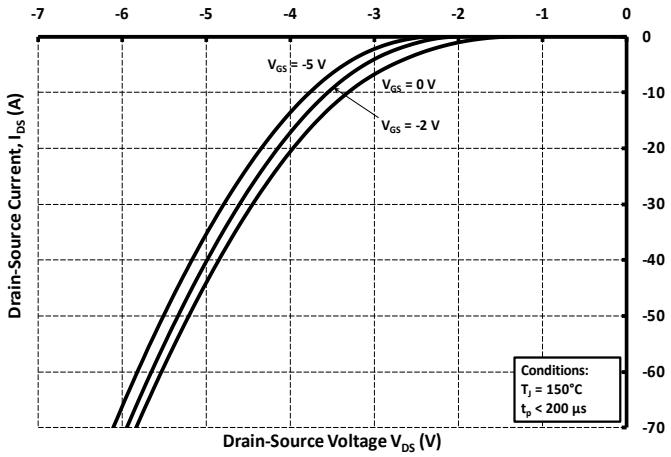


Figure 10. Body Diode Characteristic at 150 °C

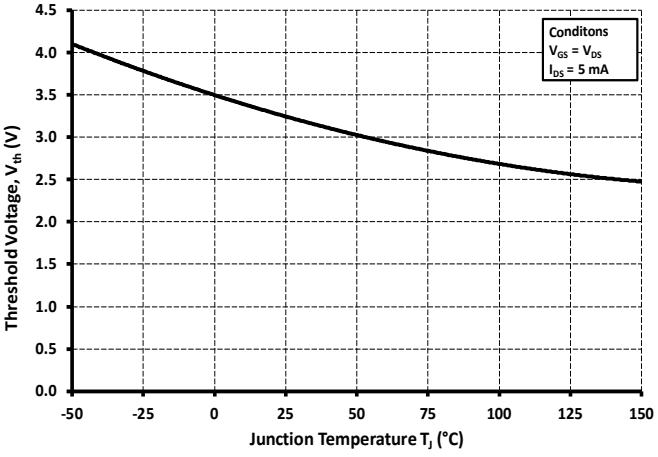


Figure 11. Threshold Voltage vs. Temperature

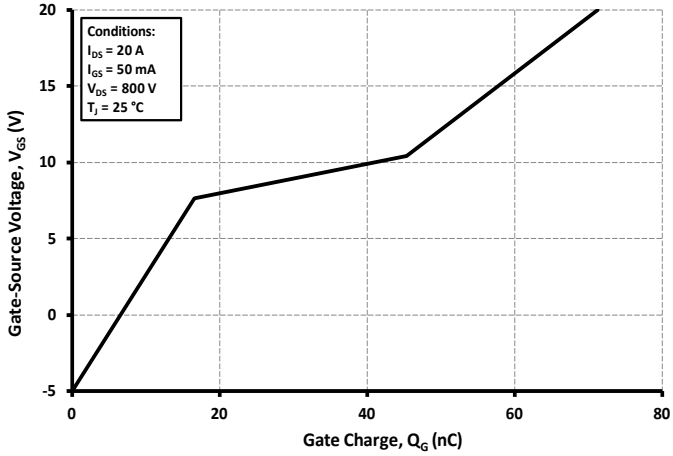


Figure 12. Gate Charge Characteristics

Typical Performance

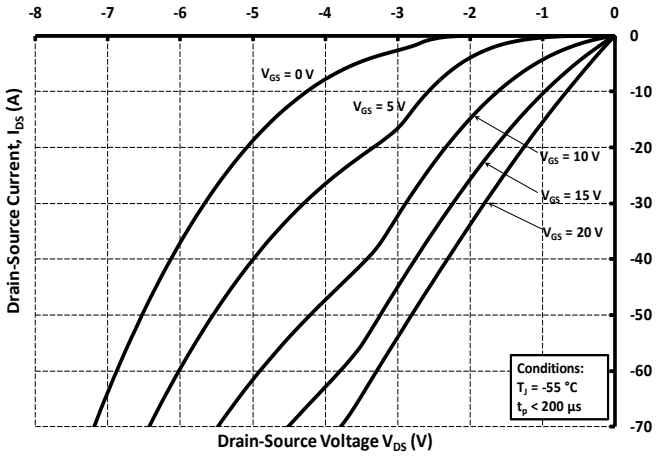


Figure 13. 3rd Quadrant Characteristic at -55 ºC

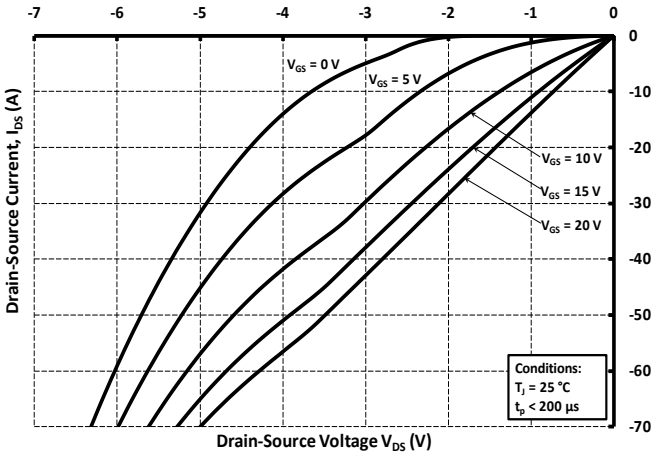


Figure 14. 3rd Quadrant Characteristic at 25 ºC

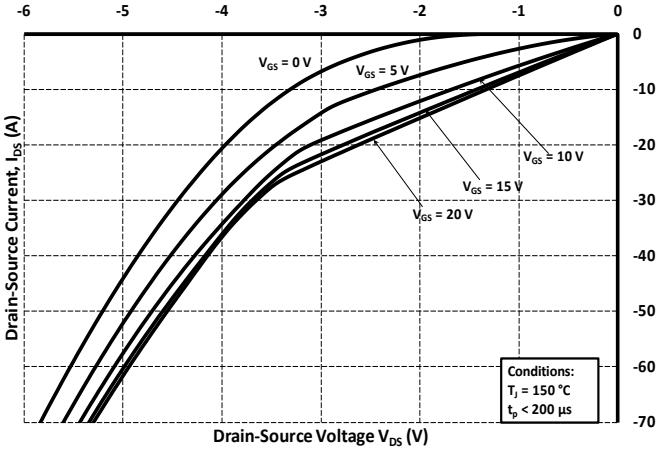


Figure 15. 3rd Quadrant Characteristic at 150 ºC

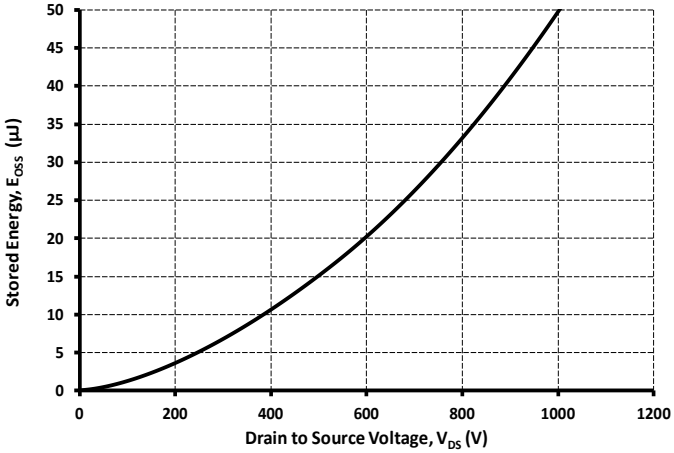


Figure 16. Output Capacitor Stored Energy

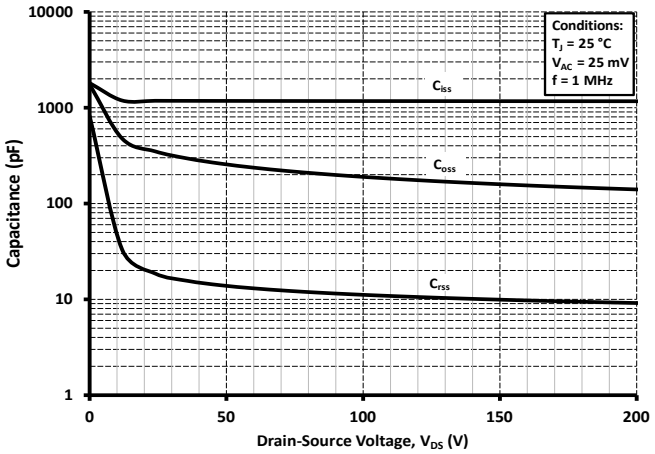


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

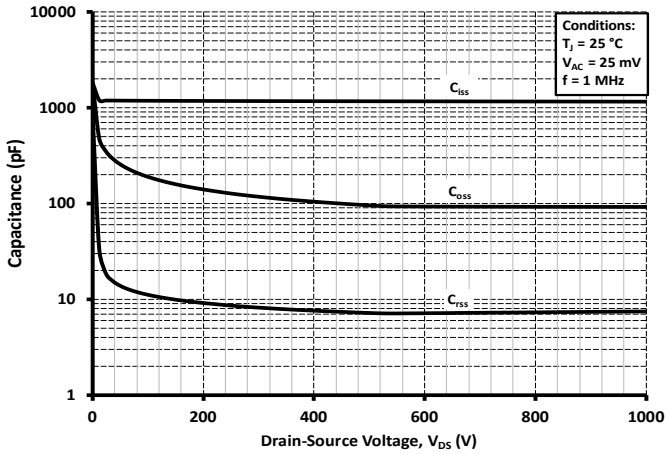


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1000V)

Typical Performance

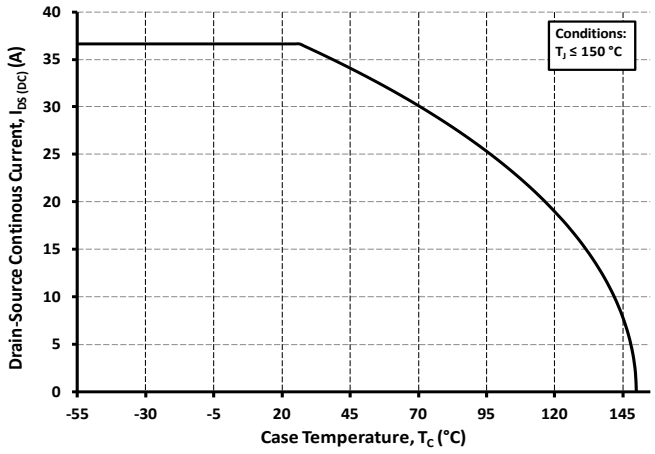


Figure 19. Continuous Drain Current Derating vs. Case Temperature

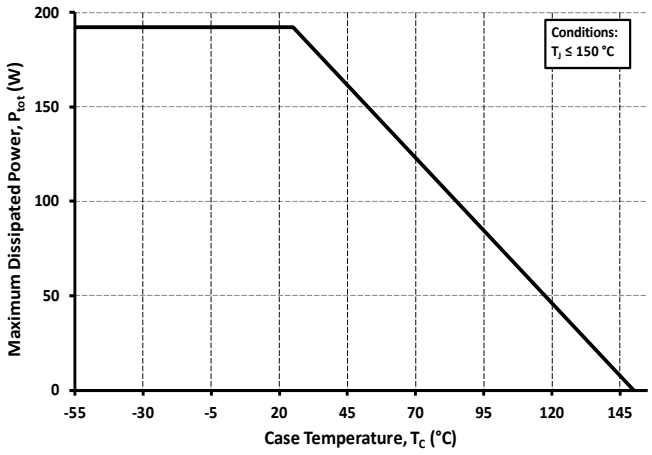


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

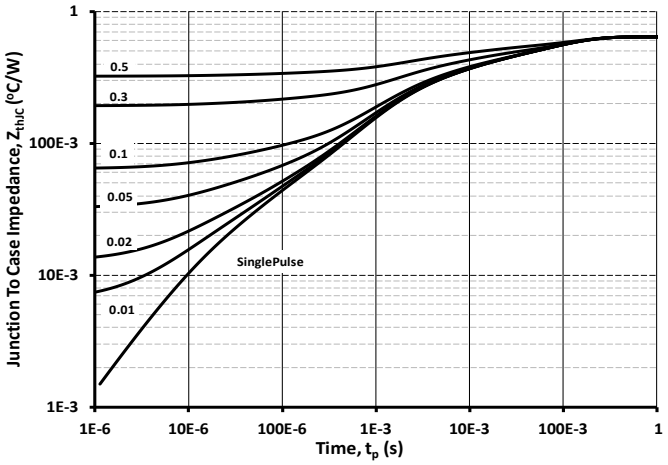


Figure 21. Transient Thermal Impedance (Junction - Case)

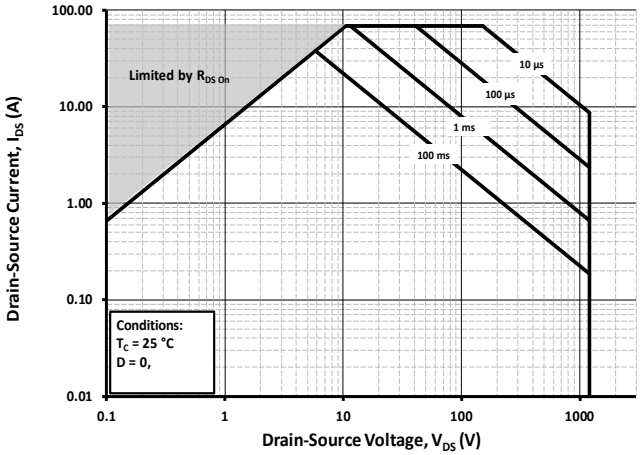


Figure 22. Safe Operating Area

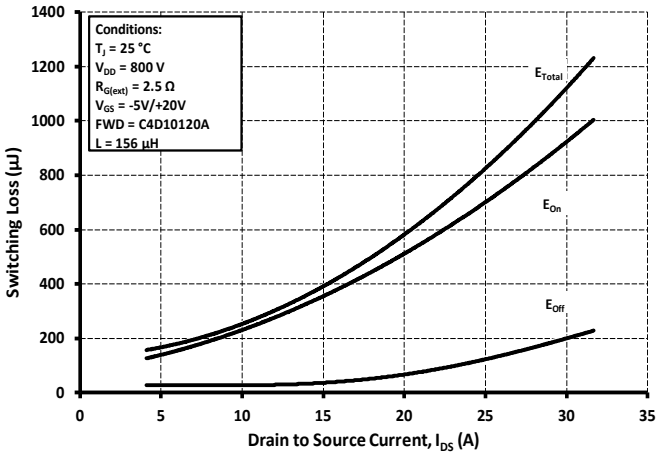


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 800V)

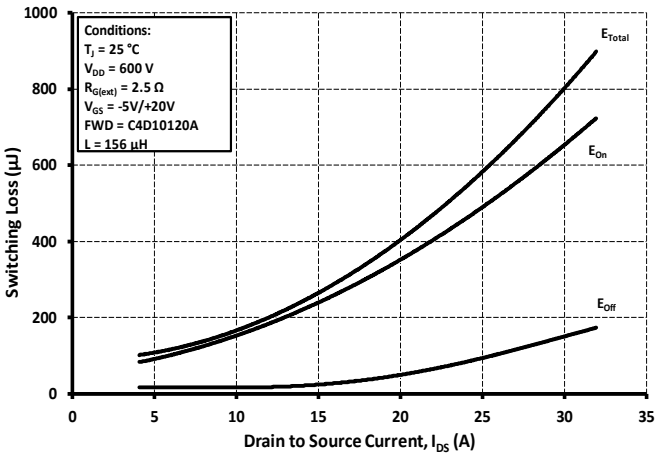


Figure 24. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 600V)

Typical Performance

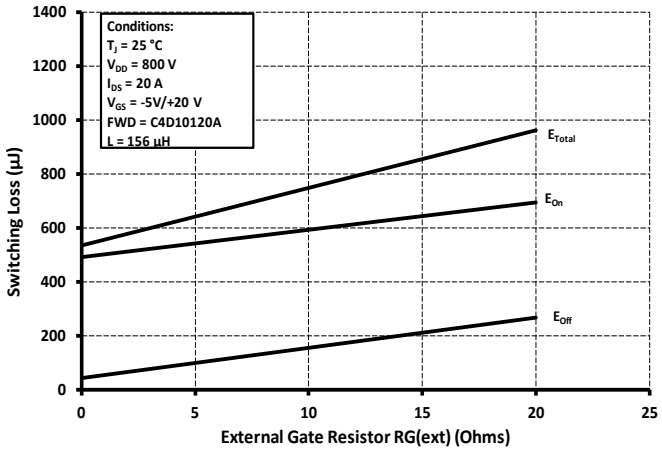


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

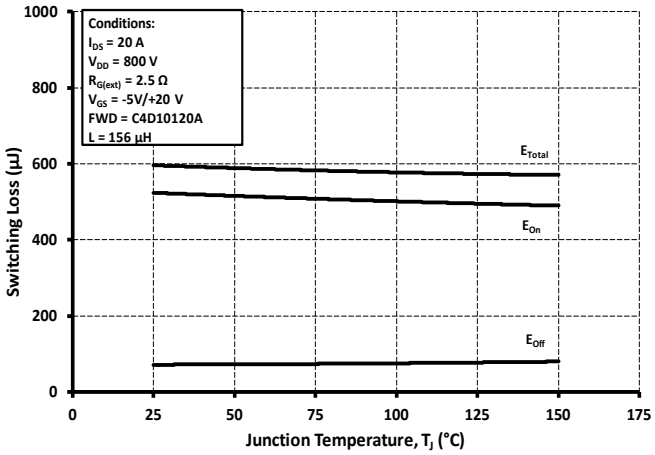


Figure 26. Clamped Inductive Switching Energy vs. Temperature

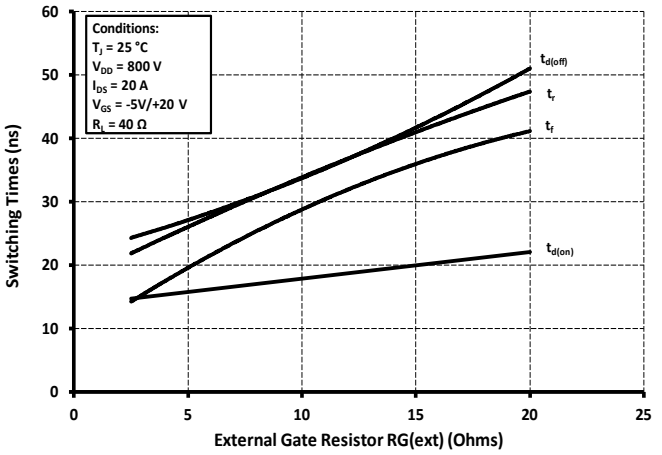


Figure 27. Switching Times vs. $R_{G(ext)}$

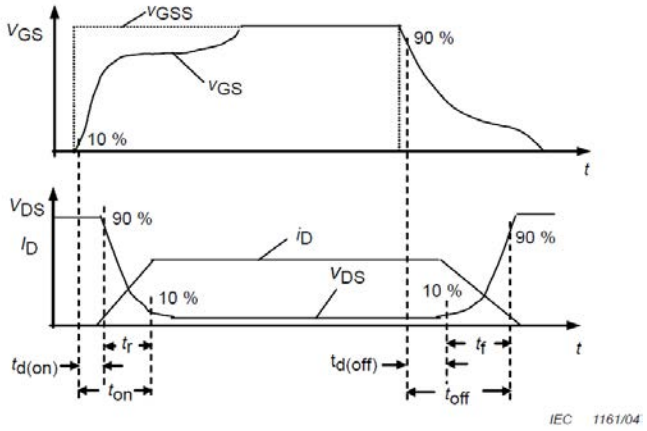


Figure 28. Switching Times Definition

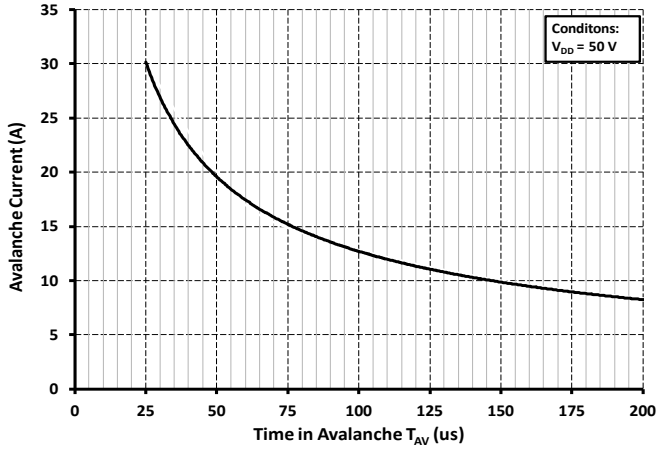


Figure 29. Single Avalanche SOA curve

Test Circuit Schematic

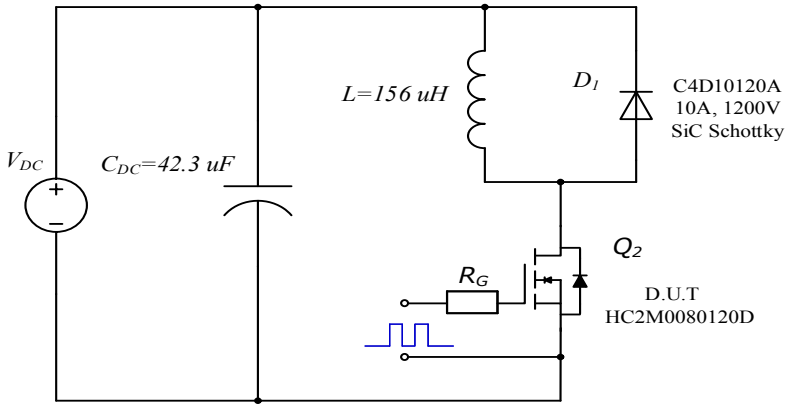


Figure 30. Clamped Inductive Switching Waveform Test Circuit

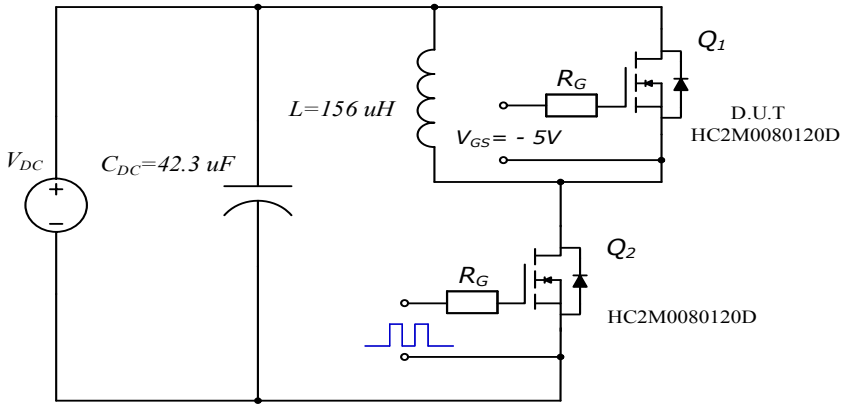


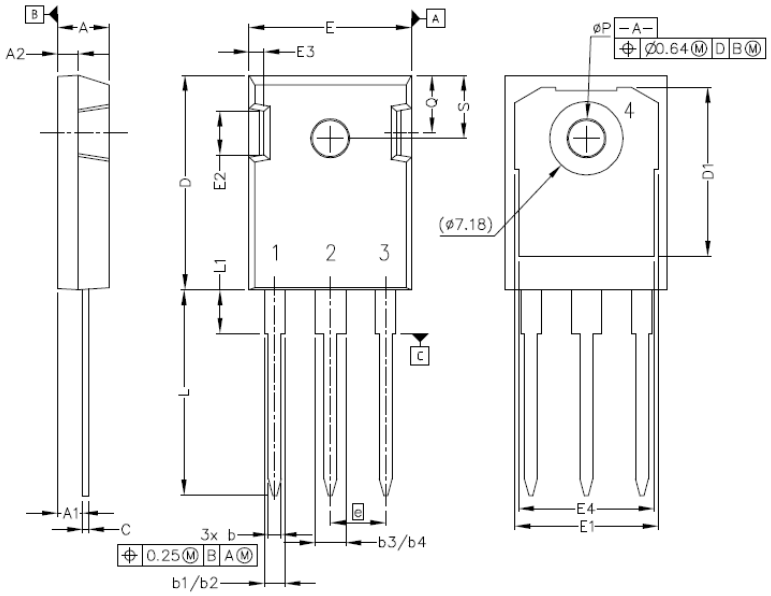
Figure 31. Body Diode Recovery Test Circuit

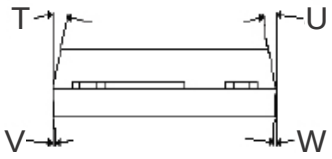
ESD Ratings

ESD Test	Total Devices Sampled	Resulting Classification
ESD-HBM	All Devices Passed 1000V	2 (>2000V)
ESD-MM	All Devices Passed 400V	C (>400V)
ESD-CDM	All Devices Passed 1000V	IV (>1000V)

Package Dimensions

Package TO-247



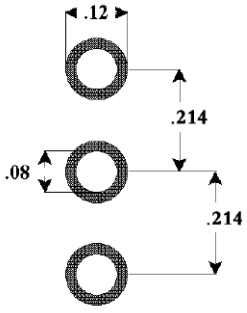


Pinout Information:

- Pin 1 = Gate
- Pin 2, 4 = Drain
- Pin 3 = Source

POS	Inches		Millimeters	
	Min	Max	Min	Max
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.042	.052	1.07	1.33
b1	.075	.095	1.91	2.41
b2	.075	.085	1.91	2.16
b3	.113	.133	2.87	3.38
b4	.113	.123	2.87	3.13
c	.022	.027	0.55	0.68
D	.819	.831	20.80	21.10
D1	.640	.695	16.25	17.65
D2	.037	.049	0.95	1.25
E	.620	.635	15.75	16.13
E1	.516	.557	13.10	14.15
E2	.145	.201	3.68	5.10
E3	.039	.075	1.00	1.90
E4	.487	.529	12.38	13.43
e	.214 BSC		5.44 BSC	
N	3		3	
L	.780	.800	19.81	20.32
L1	.161	.173	4.10	4.40
ØP	.138	.144	3.51	3.65
Q	.216	.236	5.49	6.00
S	.238	.248	6.04	6.30
T	9°	11°	9°	11°
U	9°	11°	9°	11°
V	2°	8°	2°	8°
W	2°	8°	2°	8°

Recommended Solder Pad Layout



TO247-3L

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give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

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HXY MOSFET:

HPTVSUC3D5VB PESDNC2XD5VBF TPSMB100CA-VR ESD5L5.0C-HXY ESD5LM5.0C-HXY HESDSLC3V3D3B HSTS521050B331 LM393DR-HXY PESDNC2XD5VBL TPSMB28A-VR AZ4007-01H HAZ4007-01H HCEZ36V,L3F HSD15C.TCT HSEN2411D3 PJEC5V0M1FN2 PJSD24CW_R1 HACPDQC5V0-HF HLY323BC1524L HSEN3611D3 HSG3D15B3.3MA PESDLC2FD3V3BH RLSD32A121V 60N06 AZ4836-01L HESD36VD3B HRCLAMP3371ZCTFT AQ15C-01FTG BV05C-H PESDSC2FD5VU