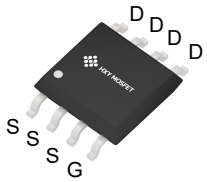
SI4435DYPBF

P-Channel Enhancement Mode MOSFET

Description

The SI4435DYPBF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



SOP-8

General Features

V_{DS} = -30V I_D = -11A

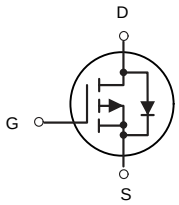
$R_{DS(ON)}$ < 16mΩ @ V_{GS}=10V

Application

Battery protection

Load switch

Uninterruptible power supply



P-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
SI4435DYPBF	SOP-8	HXY MOSFET	3000

Absolute Maximum Ratings (Tc=25℃ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Drain Current[3], V_{GS} @ 10V	-11	A
I_D@T_A=70℃	Drain Current[3], V_{GS} @ 10V	-9.1	A
I_{DM}	Pulsed Drain Current[1]	-40	A
P_D@T_A=25℃	Total Power Dissipation	2.5	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	50	℃/W

Electrical Characteristics@T_j=25 °C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V, I_D=-10A	-	12.5	16	mΩ
		V_{GS}=-4.5V, I_D=-6A	-	17	21	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1	-	-3	V
g_{fs}	Forward Transconductance	V_{DS}=-10V, I_D=-10A	-	22	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-24V, V_{GS}=0V	-	-	-10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge	I_D=-6A V_{DS}=-15V V_{GS}=-4.5V	-	28	45	nC
Q_{gs}	Gate-Source Charge		-	7	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge		-	11	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=-15V I_D=-1A R_G=3.3Ω V_{GS}=-10V	-	13	-	ns
t_r	Rise Time		-	10	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	80	-	ns
t_f	Fall Time		-	37	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V V_{DS}=-15V f=1.0MHz	-	2940	4700	pF
C_{oss}	Output Capacitance		-	290	-	pF
C_{rss}	Reverse Transfer Capacitance		-	210	-	pF
R_g	Gate Resistance	f=1.0MHz	-	6.2	12.4	Ω
V_{SD}	Forward On Voltage[2]	I_S=-2.1A, V_{GS}=0V	-	-	-1.2	V
t_{rr}	Reverse Recovery Time	I_S=-10A, V_{GS}=0V, dI/dt=100A/μs	-	19	-	ns
Q_{rr}	Reverse Recovery Charge		-	6	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤ 10s ; 125 ℃/W when mounted on Min. copper pad.

Typical Characteristics

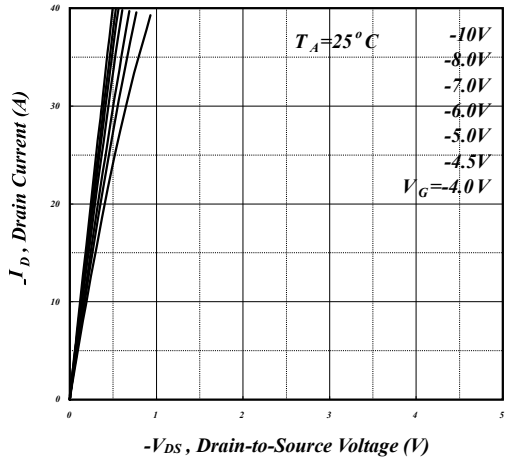


Fig 1. Typical Output Characteristics

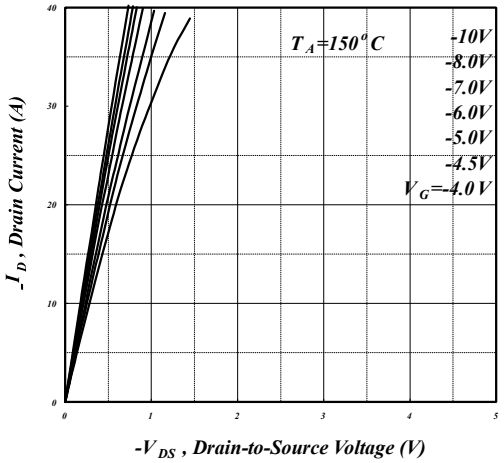


Fig 2. Typical Output Characteristics

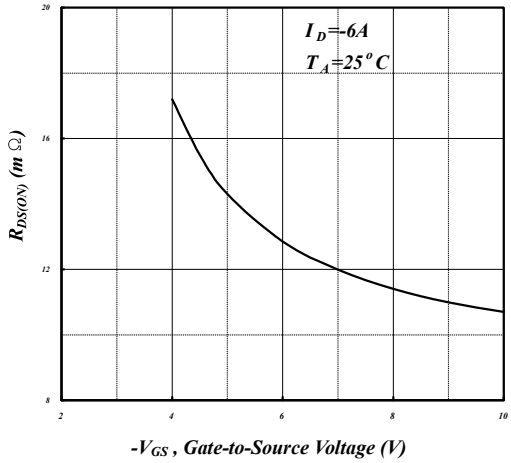


Fig 3. On-Resistance v.s. Gate Voltage

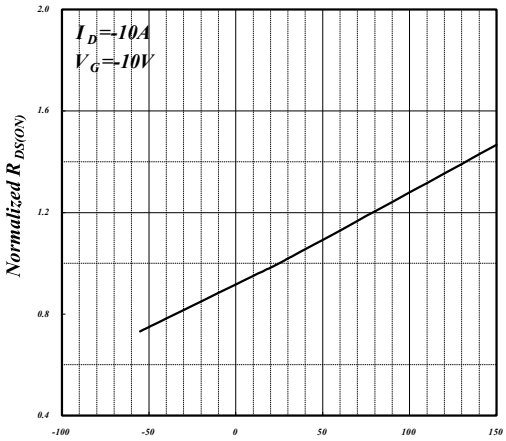
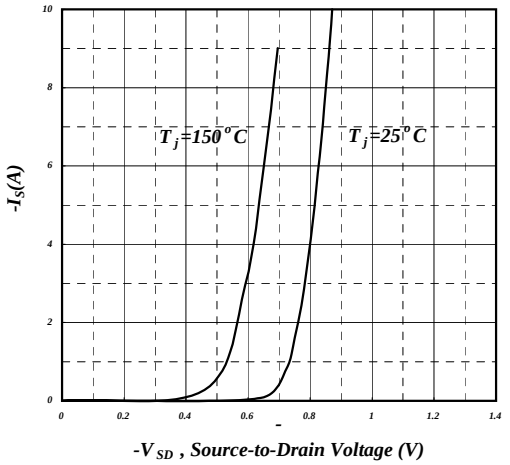


Fig 4. Normalized On-Resistance v.s. Junction Temperature



Reverse Diode

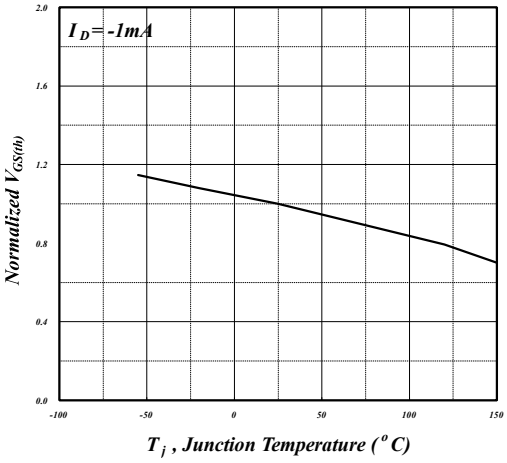


Fig 6. Gate Threshold Voltage v.s. Junction Temperatur

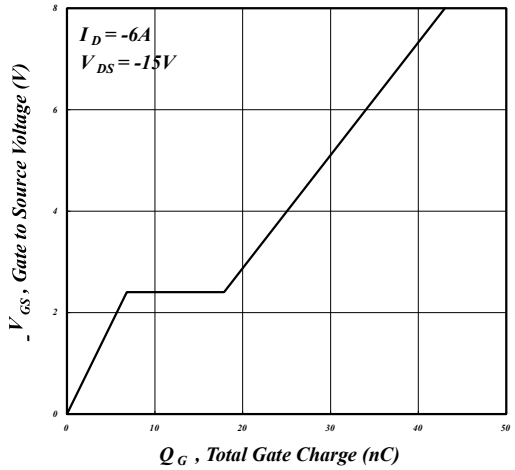


Fig 7. Gate Charge Characteristics

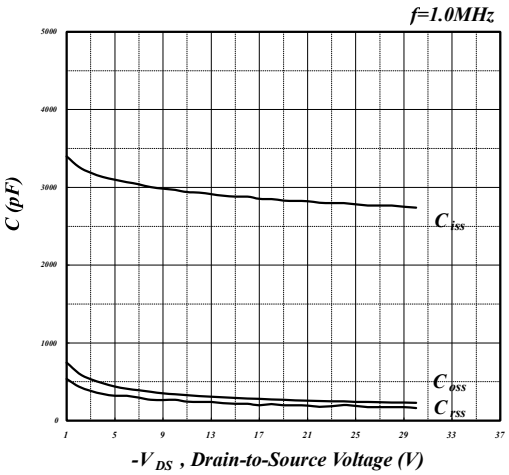


Fig 8. Typical Capacitance Characteristics

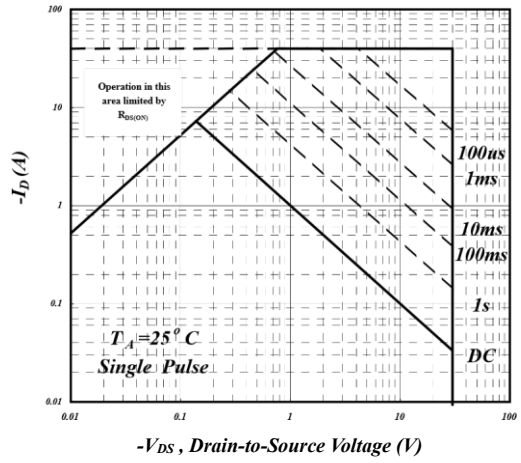


Fig 9. Maximum Safe Operating Area

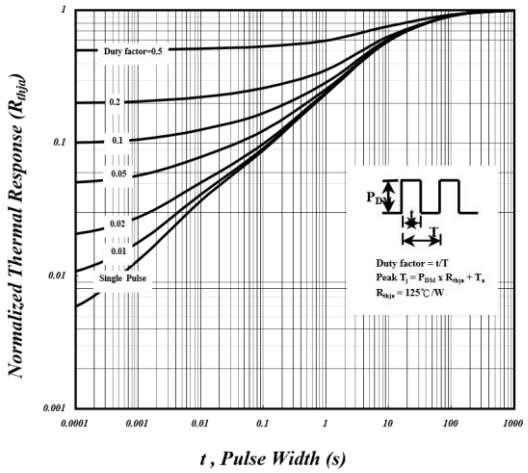


Fig 10. Effective Transient Thermal Impedance

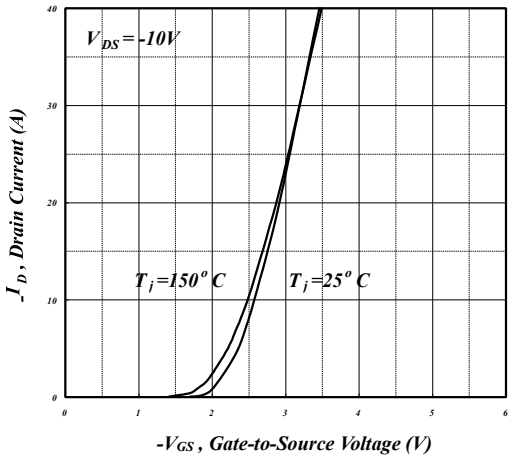


Fig 11. Transfer Characteristics

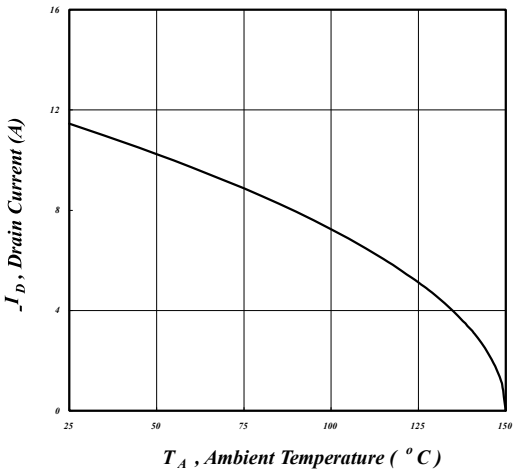


Fig 12. Drain Current v.s. Ambient Temperature

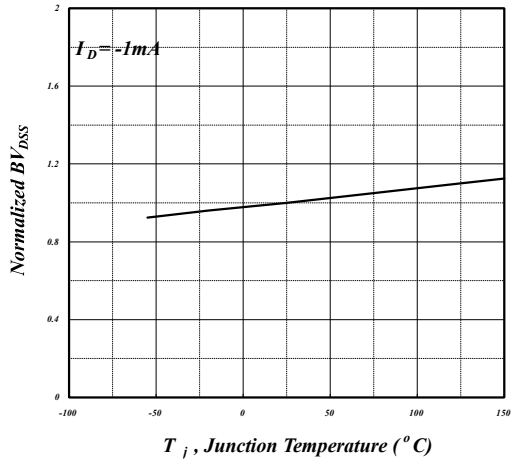


Fig 13. Normalized BV_{DSS} v.s. JunctionTemperature

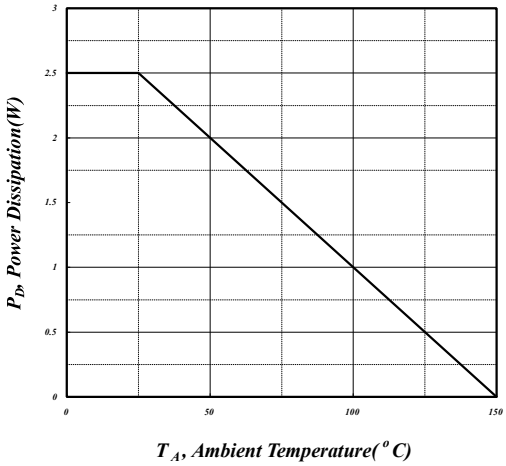


Fig 14. Total Power Dissipation

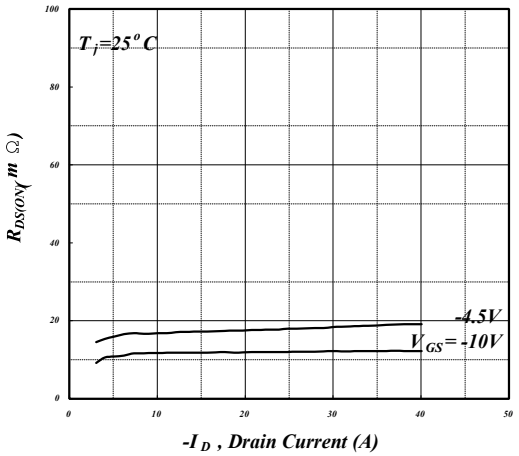
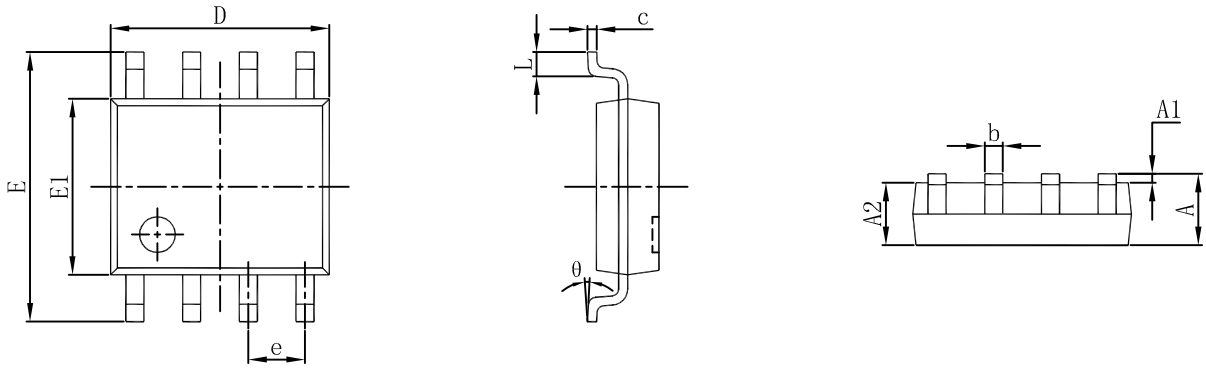
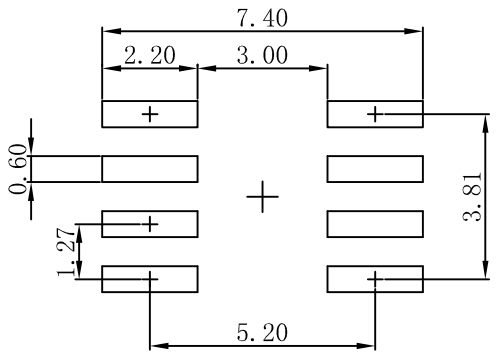


Fig 15. Typ. Drain-Source on State Resistance

SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

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