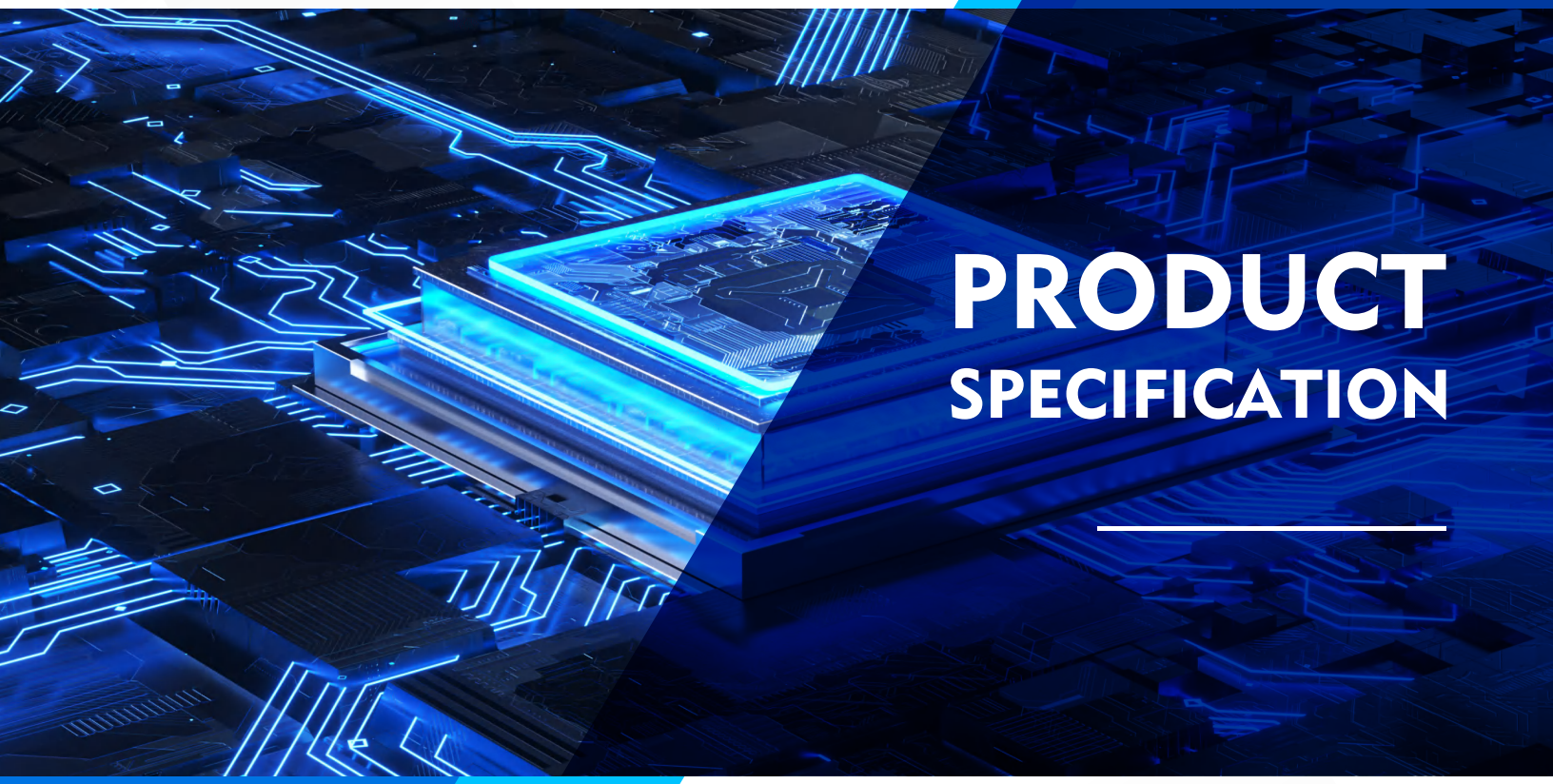
HJKE

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PRODUCT SPECIFICATION

MAIN PRODUCTS

1 FEATURES

- Bus-Pin Fault Protection to ±70V
- Common-Mode Voltage Range (-30V to 30V)
- Operation With 3.3V to 5V Supply Range
- ±16kV HBM Protection on Bus Pins
- Reduced Unit Load for Up to 320 Nodes
- LVTTL I/O withstands up to 5V
- Failsafe Receiver for Open-Circuit, Short-Circuit,and Idle-Bus Conditions
- Low Power Consumption:
  Low Standby Supply Current, 2 μA Maximum
  I_{CC} 0.5mA Quiescent Current During Operation
- Signaling Rates of 10Mbps

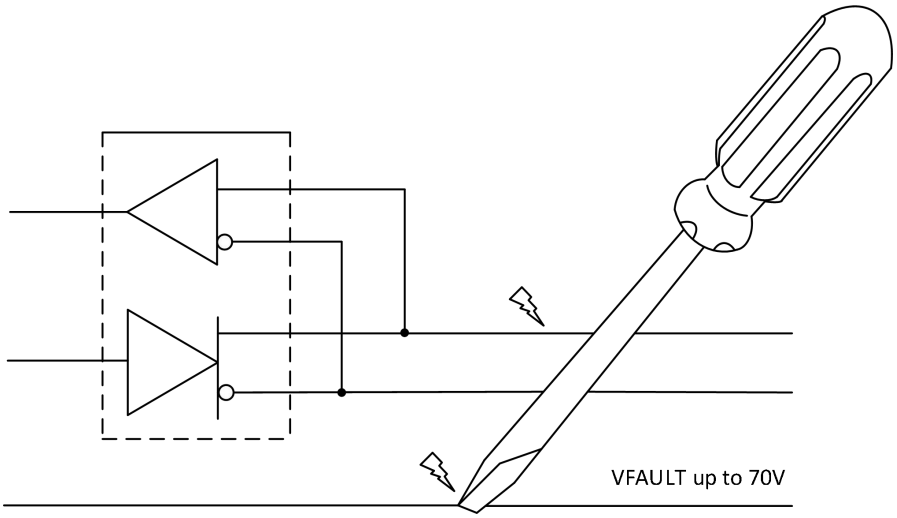
2 APPLICATIONS

- HAVC Networks
- Security Electronics
- Building Automation
- Telecommunication Equipment
- Motion Control
- Industrial Networks

3 DESCRIPTION

The SN65HVD1782 devices are designed to survive overvoltage faults such as direct shorts to power supplies, mis-wiring faults, connector failures, cable crushes, and tool mis-applications. The devices are also robust to ESD events with high levels of protection to the human-body-model specification.
The SN65HVD1782
devices combine a differential driver and a differential receiver, which operate from a single power supply. In the SN65HVD1782 ,
the driver differential outputs
and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus)communication. This port features a wide common mode voltage range, making the devices suitable for multipoint applications over long cable runs. These devices are characterized from –40°C to 125°C. These devices are fully compliant with ANSI TIA/EIA 485A with a 5V supply and can operate with a 3.3V supply with reduced driver output voltage for low power applications.

Protection Against Bus Shorts

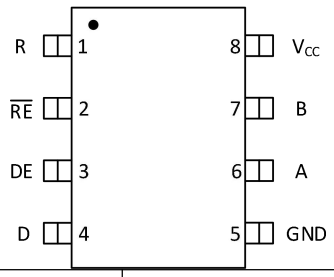


Device Comparison Table

TRANSCEIVER	SLGNALING RATE	NUMBER OF NODES
SN65HVD1782DR	Up to 10Mbps	Up to 320

4 Pin Configuration and Functions

D Package and P Package
8-Pin SOIC and 8-Pin PDIP
(Top View)



Pin		I/O	Description
Name	No.		
R	1	Digital output	Receive data output
/RE	2	Digital input	Receiver enable low
DE	3	Digital input	Driver enable high
D	4	Digital input	Driver data input
GND	5	Reference potential	Local device ground
A	6	Bus input/output	Driver output or receiver input (complimentary to B)
B	7	Bus input/output	Driver output or receiver input (complimentary to A)
V_{CC}	8	Supply	3V to 5.5V supply

5 Specifications

5.1 Absolute Maximum Ratings(1)

Parameter	Description		MIN	MAX	UNIT
V_{CC}	Supply voltage		-0.5	7	V
	voltage at bus pin SN65HVD1782	A,B pins	-70	70	V
V_I	Input voltage at any logic pin		–0.3	V_{CC}+0.3	V
V_O	Transient overvoltage pulse through 100Ω per TIA-485		–70	70	V
I_O	Receiver output current		–24	24	mA
T_J	junction temperature			170	°C
T_{stg}	Storage temperature		-55	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

				Value	Unit
V(ESD)	Electrostatic discharge	Human body model (HBM)(1)	Bus pins and GND	±16000	V
			All pins	±4000	
		Charged device model (CDM), all pins(2)		±2000	
		Machine model ,all pins		±400	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Condition

Parameter	Description		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15	5	5.5	V
	voltage at any bus terminal (separately or common mode)(1)		-30		30	V
V_{IH}	High-level input voltage	driver, driver enable, and receiver enable inputs	2		V_{CC}	V
V_{IL}	Low-level input voltage	driver, driver enable, and receiver enable inputs	0		0.8	V
V_{ID}	Differential input voltage		-30		30	V
I_O	output current	Driver	-60		60	mA
		Receiver	-8		8	mA
R_L	Differential load resistance		54	60		
C_L	Differential load capacitance			50		
$1/t_{U1}$	Signaling rate	SN65HVD1782			1	Mbps
					10	
T_A	Operating free-air temperature(1)	5V supply	-40		105	°C
		3.3V supply	-40		125	
T_J	junction temperature		-40		150	°C

(1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

5.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

Parameter	Description	Test Conditions		MIN	TYP	MAX	UNIT
$\|V_{OD(D)}\|$	Driver differential output voltage magnitude	R_L = 60Ω, 4.75V ≤ V_{CC},375 Ω on each output to –7 V to 12 V,See Figure 1	T_A<85℃	1.9			V
			T_A<125℃	1.8			
		R_L = 54Ω,4.75V ≤ V_{CC} ≤ 5.25V	T_A<85℃	2.1	2.4		
			T_A<125℃	2.0			
		R_L = 54Ω,3.15V ≤ V_{CC} ≤ 3.45V		1.1	1.4		
		R_L = 100Ω,4.75V ≤ V_{CC} ≤ 5.25V	T_A<85℃	2.5	3.0		
			T_A<125℃	2			
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54Ω		-50	0	50	mV
$V_{OC(SS)}$	Steady-state common mode output voltage			1	V_{CC}/2	3	V
ΔV_{OC}	Change in differential driver output common mode voltage			-50	0	50	mV
$V_{OC(PP)}$	Peak-to-peak driver common mode output voltage	Center of two 27Ω load resistors See Figure 2			500		mV
C_{OD}	Differential output capacitance				23		pF
V_{IT+}	Positive-going receiver differential input voltage threshold				-100	-35	mV
V_{IT-}	Negative-going receiver differential input voltage threshold			-300	-150		mV
V_{hys}	Receiver differential input voltage threshold hysteres is ($V_{IT+} - V_{IT-}$)			30	100		mV
V_{OH}	Receiver high-level output voltage	I_{OH}=-8mA		2.4	V_{CC}-0.6		V
V_{OL}	Receiver low-level output voltage	I_{OL}=8mA	TA < 85°C		0.4	0.6	V
			TA < 125°C			0.7	
$I_{I(LOGIC)}$	Driver input, driver enable, and receiver enable input current standby			-50		50	μA
I_{OZ}	Receiver output high impedance current	V_O=0V or V_{CC},/RE at V_{CC}		-1		1	μA
I_{OS}	Driver short-circuit output current			-200		200	mA
$I_{I(BUS)}$	Bus input current (disabled driver)	V_{CC} = 3.15 to 5.5V or V_{CC} = 0V, DE at 0V	V_I=12V		150	200	μA
			V_I=-7V	-150	-90		
I_{CC}	Driver and receiver enabled	DE = V_{CC},RE = GND,no load			0.6	1	mA
	Driver enabled, receiver disabled	DE = V_{CC},RE = V_{CC},no load			0.6	1	
	Driver disabled, receiver enabled	DE = GND,RE = GND,no load			0.5	1	
	Driver disabled, receiver disabled(standby mode)	DE = GND,D = open,RE = V_{CC},no load,TA < 85°C			2	3	μA
		DE = GND,D = open,RE = V_{CC},no load,TA < 125°C				12	

5.5 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

Parameter	Description	Test Conditions		MIN	TYP(1)	MAX	UNIT
t_f, t_r	Driver differential output rise or fall time	R_L = 54Ω, C_L = 50pF, See Figure 3	SN65HVD1782	50		300	ns
		All V_{CC} and Temperature				50	
		V_{CC} > 4.5V and T< 105°C			16		
t_{PHL}, t_{PLH}	Driver propagation delay	R_L = 54Ω, C_L = 50pF, See Figure 3	SN65HVD1782			200	ns
						55	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	R_L = 54Ω, C_L = 50pF, See Figure 3	SN65HVD1782			25	ns
						10	
t_{PHZ},t_{PLZ}	Driver disable time	See Figure 4 and Figure 5	SN65HVD1782			3	µs
						3	
t_{PZH},t_{PzL}	Driver enable time	Receiver enabled,See Figure 4 and Figure 5	SN65HVD1782			300	ns
						300	ns
		Receiver disabled,See Figure 4 and Figure 5	SN65HVD1782			10	ns
						9	µs
t_f,t_r	Receiver output rise or fall time	C_L = 15pF,See Figure 6	All devices		4	15	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time	C_L = 15pF,See Figure 6	SN65HVD1782		100	200	ns
						80	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	C_L = 15pF,See Figure 6	SN65HVD1782		6	20	
						5	
t_{PHZ},t_{PLZ}	Receiver disable time	Driver enabled, See Figure 7			15	100	ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled, See Figure 7			80	300	ns
		Driver disabled, See Figure 8			3	9	µs

6 Parameter Measurement Information

Input generator rate is 100kbps, 50% duty cycle, rise or fall time is less than 6ns, output impedance is 50 Ω.

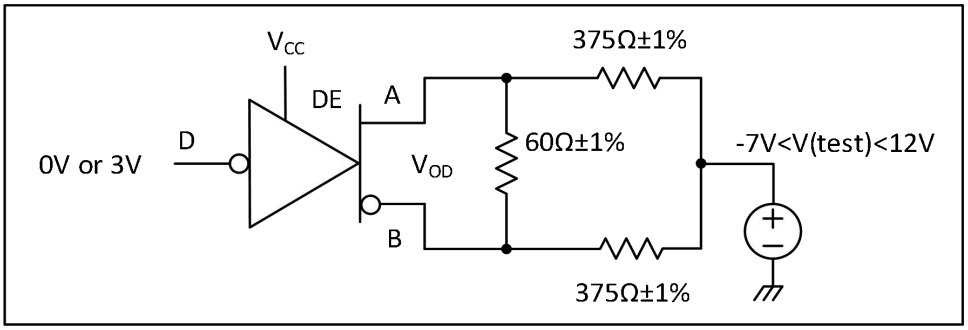


Figure 1. Measurement of Driver Differential Output Voltage With Common-Mode Load

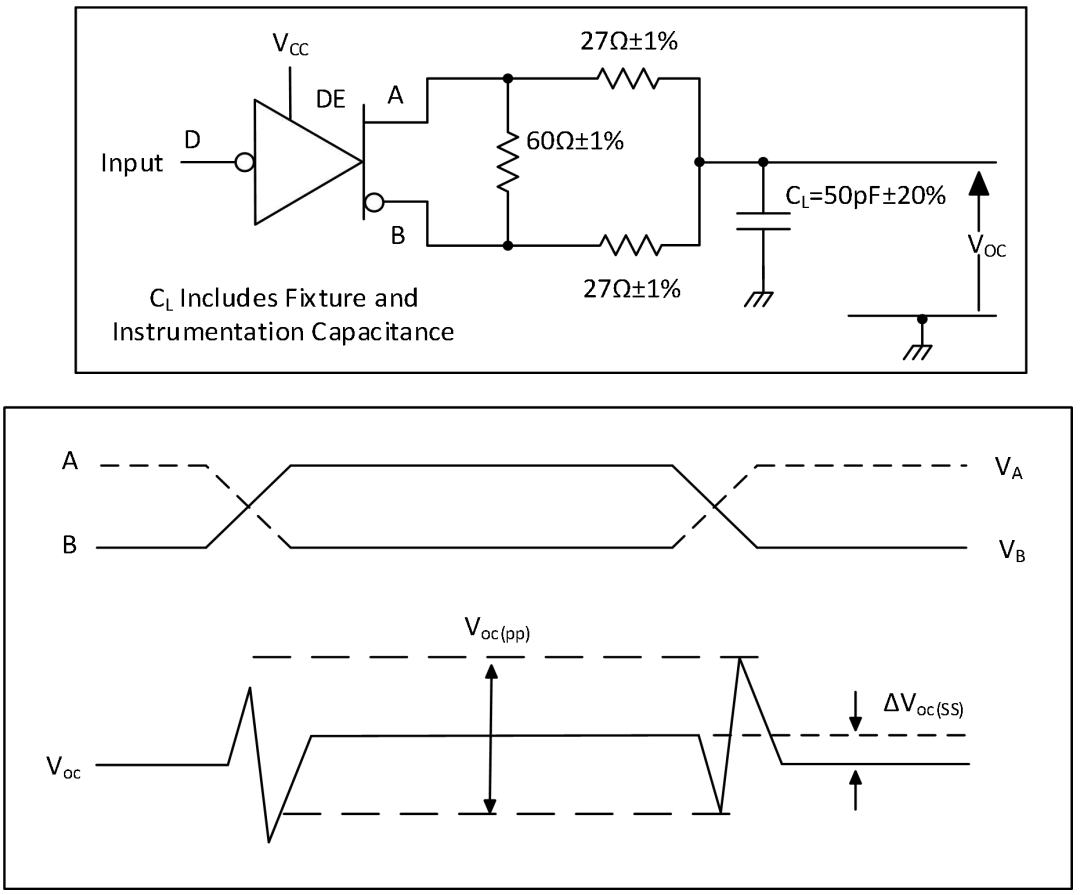


Figure 2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

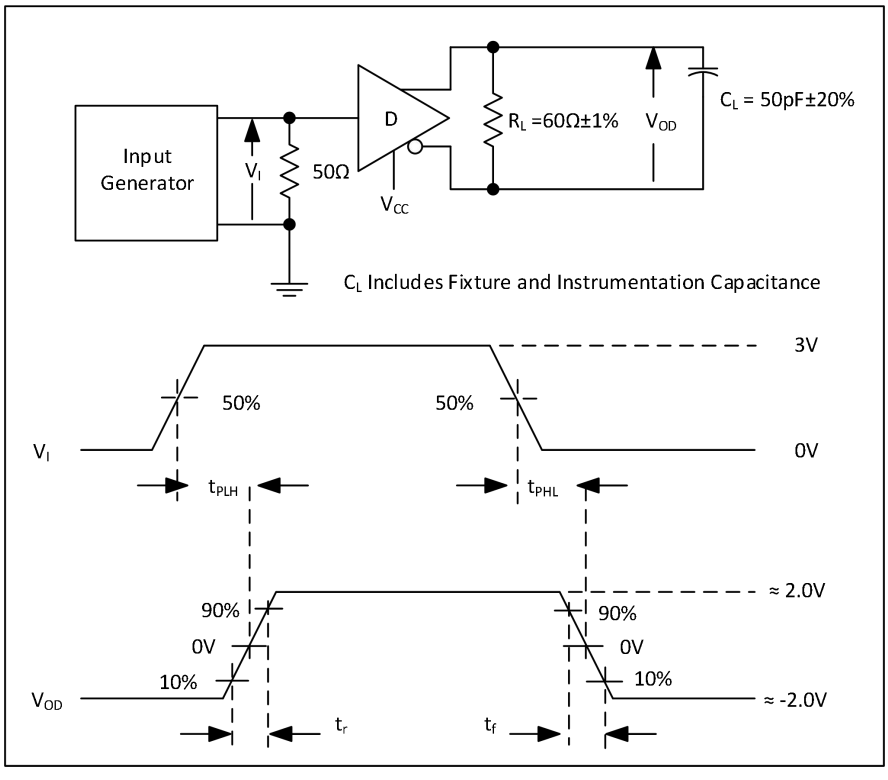


Figure 3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

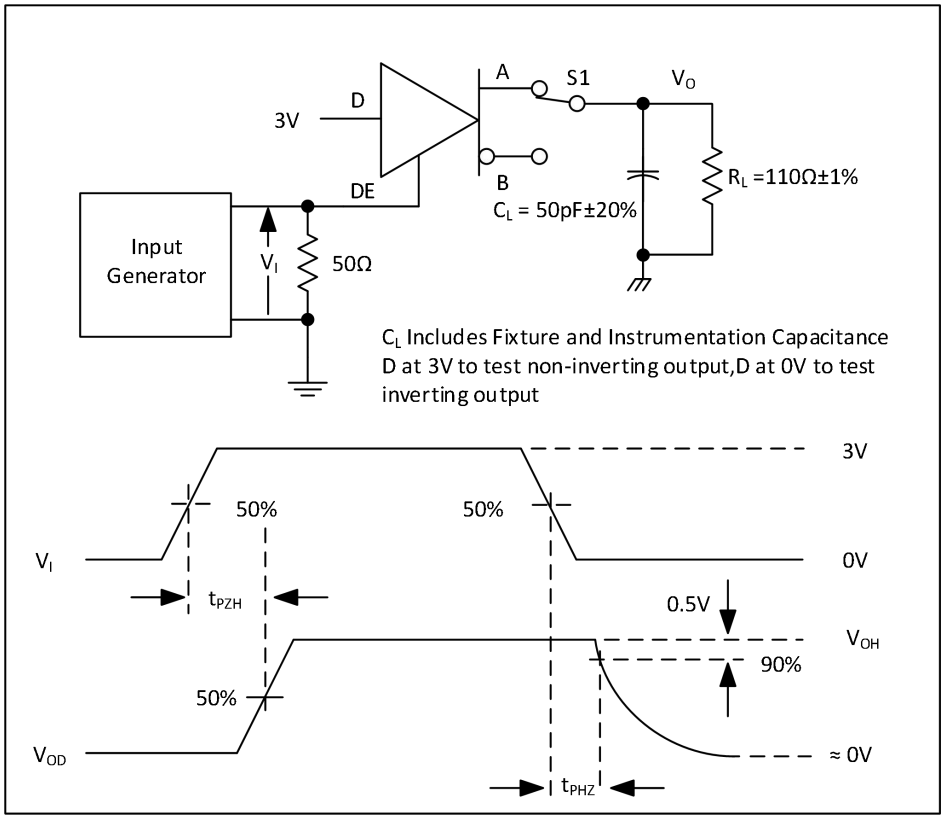


Figure 4. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load

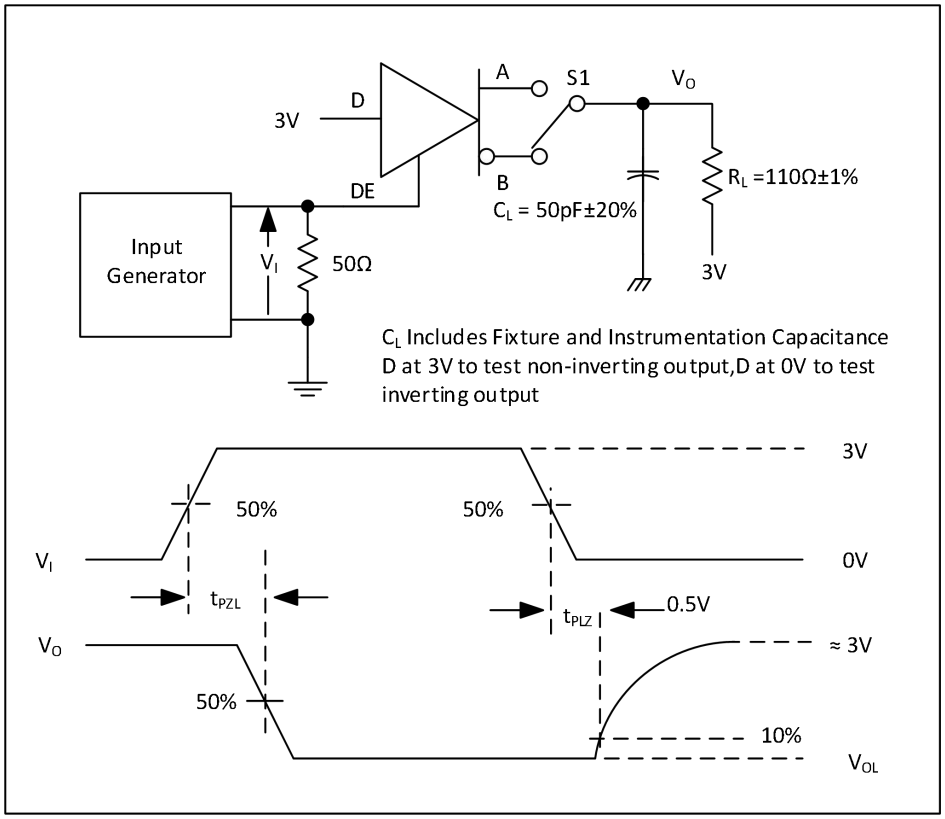


Figure 5. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load

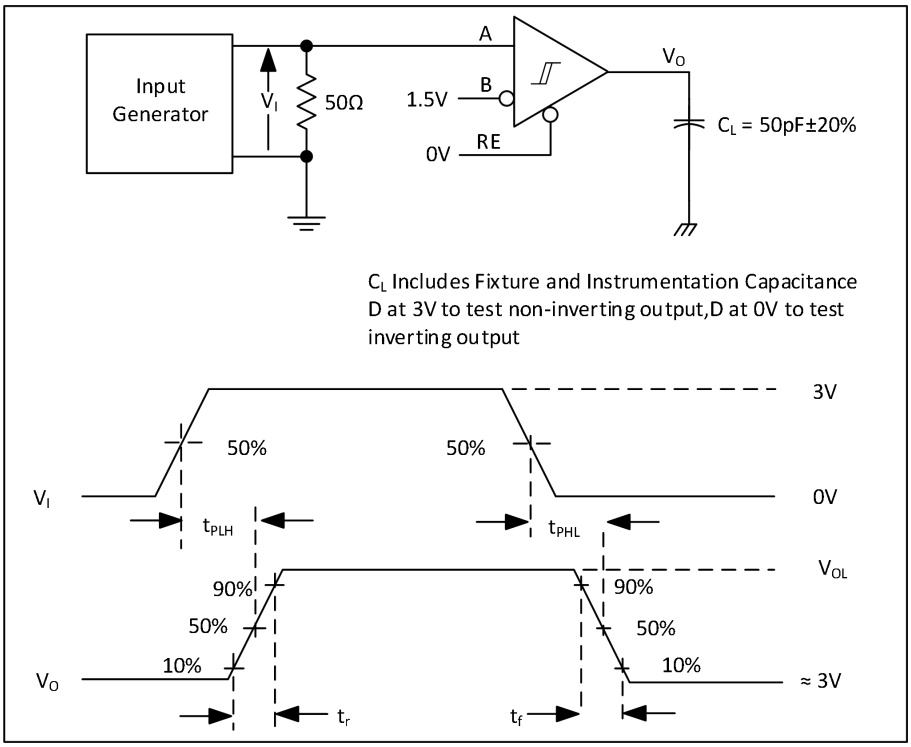


Figure 6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

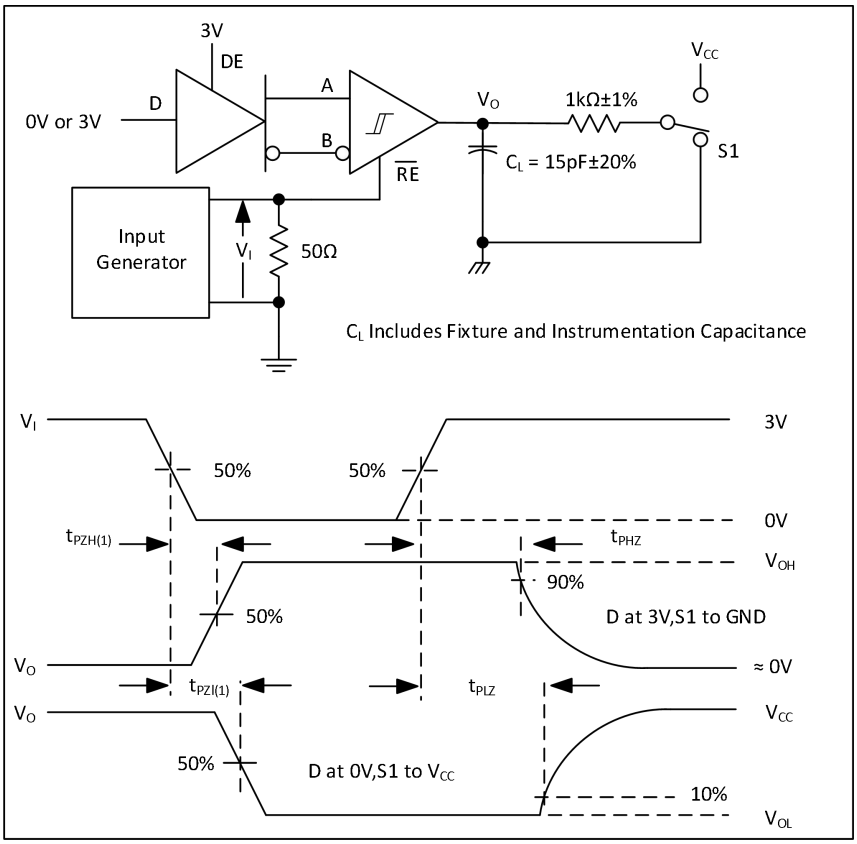


Figure 7. Measurement of Receiver Enable and Disable Times With Driver Enabled

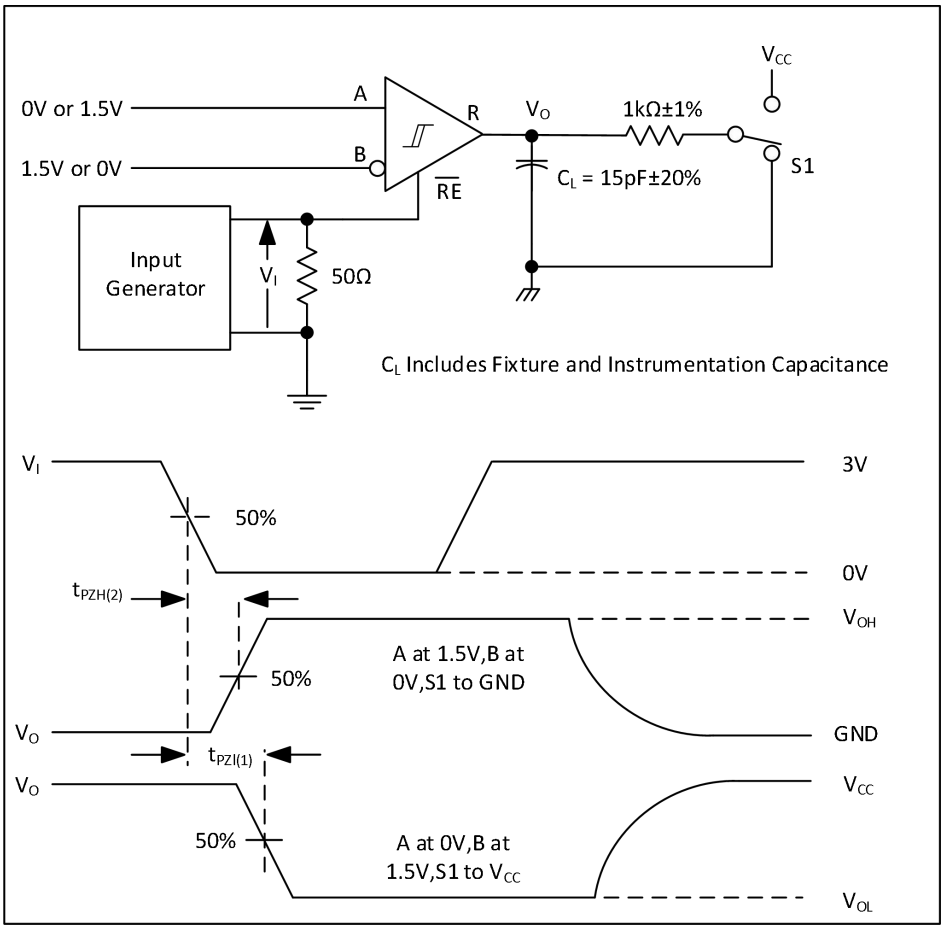


Figure 8. SN65HVD1782 **Measurement of Receiver Enable Times With Driver Disabled**

6.1 Equivalent Input Schematic

When the input digital pins float, internal high value resistors pull D/REB pins to VCC and DE pin to GND to place the device into known states. If the voltage level of D/REB input pins is higher than that of power rail, input current can flow through the input resistor and pull up resistor to VCC.

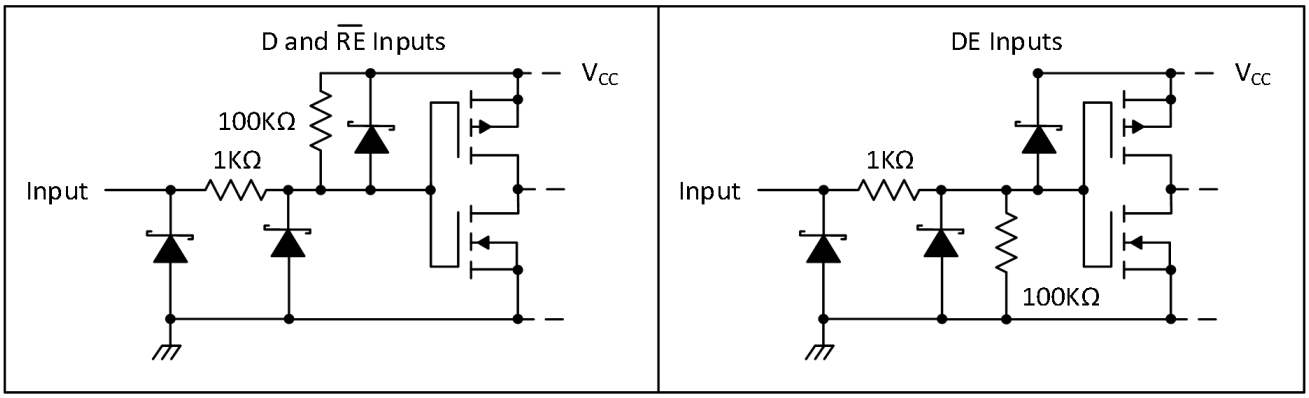


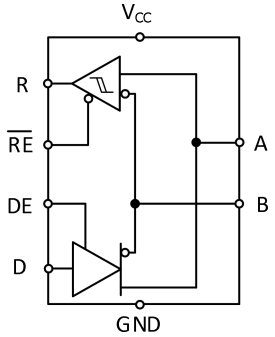
Figure 9. Equivalent Input Schematic Diagrams

7 Detailed Description

7.1 Overview

The SN65HVD1782 devices are half-duplex RS-485 transceivers available in two speed grades suitable for data transmission up to 1Mbps, and 10Mbps. These devices feature a wide common-mode operating range and bus-pin fault protection up to ±70 V. Each device has an active-HIGH driver enable and active-LOW receiver enable. A standby current of less than 2 µA can be achieved by disabling both driver and receiver.

7.2 Functional Block Diagrams



7.3 Feature Description

Internal ESD protection circuits protect the transceiver bus terminals against ±16kV human body model (HBM) electrostatic discharges.Device operation is specified over a wide temperature range from –40°C to 125°C.

7.3.1 70V Fault Protection

The SN65HVD1782 family of RS-485 transceivers is designed to survive bus pin faults up to ±70 V. The SN65HVD1782 will not survive a bus pin fault with a direct short to voltages above 30 V when:The device is powered on, and The driver is enabled (DE = HIGH), and D = HIGH AND the bus fault is applied to the A pin, OR D = LOW AND the bus fault is applied to the B pin. Under other conditions, the device will survive shorts to bus pin faults up to ±70 V. Table 1 summarizes the conditions under which the device may be damaged, and the conditions under which the device will not be damaged.

Table 1. Device Conditions

POWER	DE	D	A	B	RESULTS
OFF	X	X	-70V<V_A<70V	-70V<V_B<70V	Device survives
ON	L	X	-70V<V_A<70V	-70V<V_B<70V	Device survives
ON	H	L	-70V<V_A<70V	-70V<V_B<30V	Device survives
ON	H	L	-70V<V_A<70V	30V<V_B	Damage may occur
ON	H	H	-70V<V_A<30V	-70V<V_B<30V	Device survives
ON	H	H	30V<V_A	-70V<V_B<30V	Damage may occur

7.3.2 Receiver Failsafe

The SN65HVD1782 family of half-duplex transceivers provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. At a positive input threshold of V_{IT+} = –35mV and an input hysteresis of V_{HYS} = 30mV, the receiver output remains logic high under bus-idle, bus-short, or open bus conditions in the presence of up to 130mVPP differential noise without the need for external failsafe biasing resistors.

7.3.3 Hot-Plugging

These devices are designed to operate in "hot swap" or "hot pluggable" applications. Key features for hot pluggable applications are power-up and power-down glitch-free operation, default disabled input and output pins, and receiver failsafe.

An internal power-on reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no problems will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in Device Functional Modes, the enable inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

7.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative. When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus, when left open, the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 2. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled (1)
X	OPEN	Z	Z	Driver disabled by default (1)
OPEN	H	H	L	Actively drive bus high by default

(1) When both the driver and receiver are disabled, the device enters a low-power standby mode.

When the receiver enable pin, /RE, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R,turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-}, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-} the output is indeterminate.

When /RE is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 3. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A – V_B$	/RE	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus high
$V_{IT–} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT–}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled (1)
X	OPEN	Z	Receiver disabled by default (1)
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

(1) When both the driver and receiver are disabled, the device enters a low-power standby mode.

8 Application and Implementation

8.1 Application Information

The SN65HVD1782 devices are half-duplex RS-485 transceivers commonly used for asynchronous data transmissions.

The driver and receiver enable pins allow for the configuration of different operating modes.

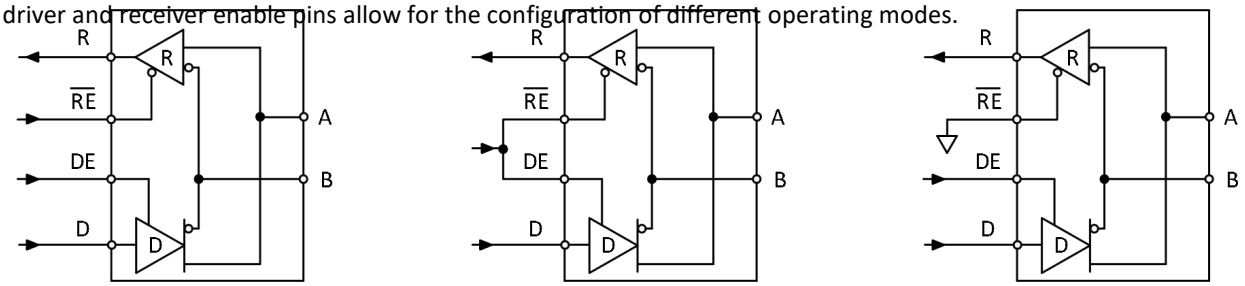


Figure 10. Half-Duplex Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high, and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node not only receives the data from the bus, but also the data it sends and can verify that the correct data have been transmitted.

8.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, RT, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

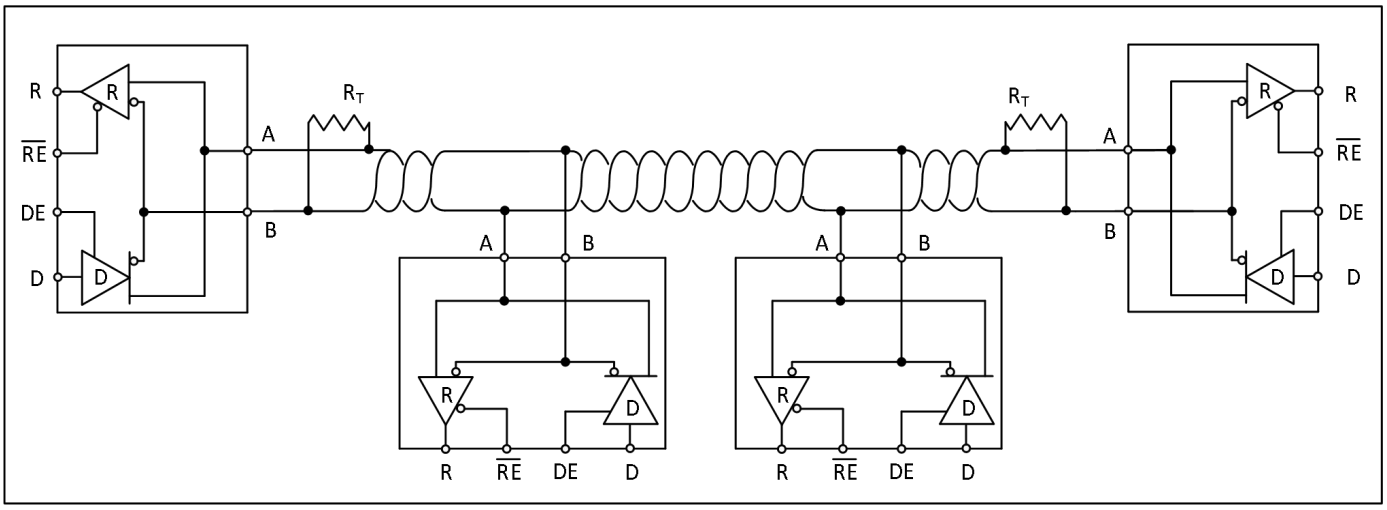


Figure 11. Typical RS-485 Network With Half-Duplex Transceivers

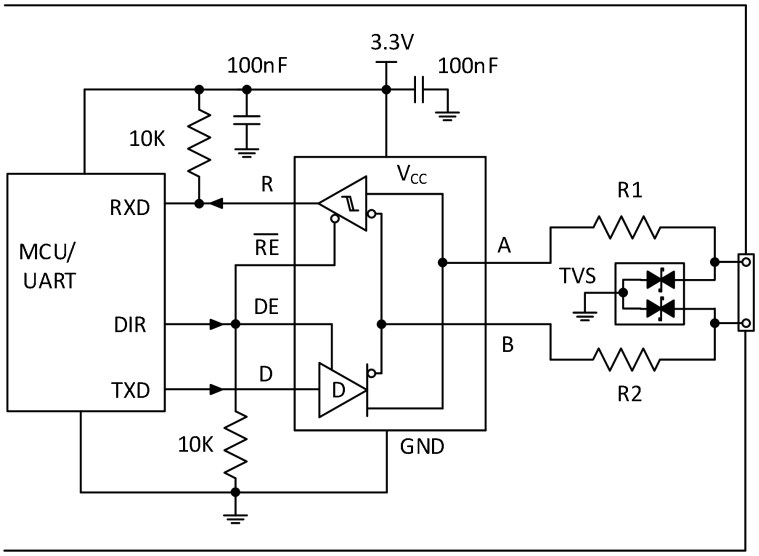


Figure 12. RS-485 Transceiver With External Transient Protection

Figure 12 shows a protection circuit intended to withstand 8kV IEC ESD (per IEC 61000-4-2) as well as 4kV EFT (per IEC 61000-4-4).

9 Layout

9.1 Layout Guidelines

On-chip IEC-ESD protection is good for laboratory and portable equipment but often insufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices.Because ESD and EFT transients have a wide-frequency bandwidth from approximately 3MHz to 3GHz, high frequency layout techniques must be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use V_{CC} and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100nF to 220nF bypass capacitors as close as possible to the V_{CC} pins of the transceiver, UART, or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1kΩ to 10kΩ pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. While pure TVS protection is sufficient for surge transients up to 1kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1mA.

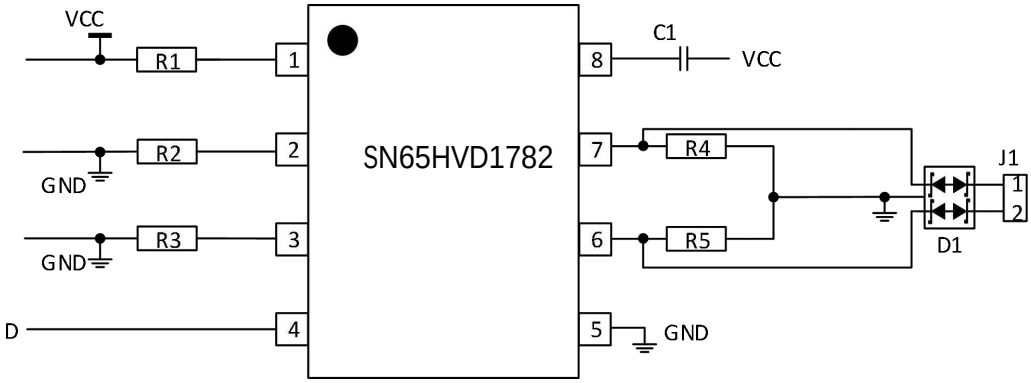
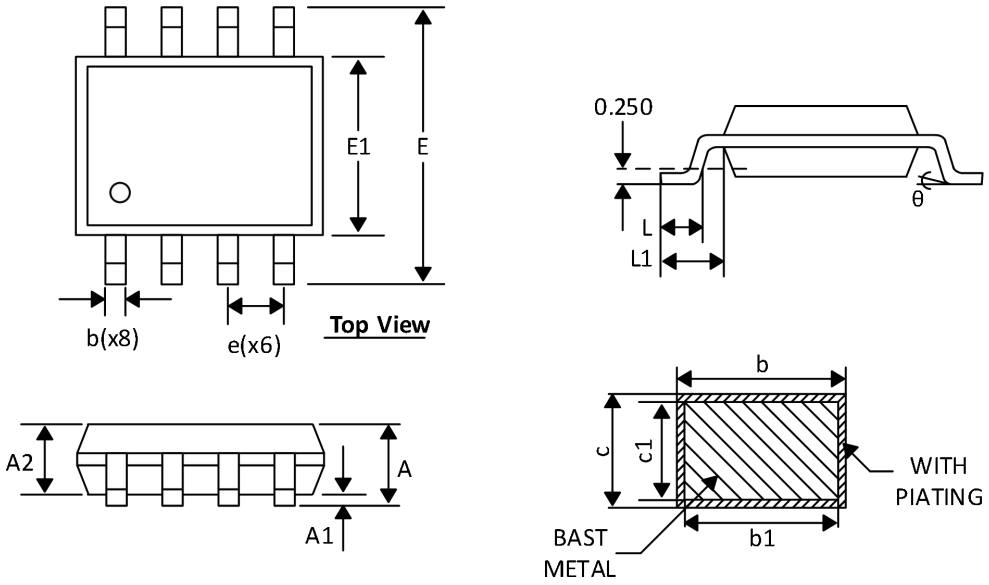


Figure 13. SN65HVD1782 **Half-Duplex Layout Example**

PACKAGE DIMENSION
SOP-8L



SYMBOLS	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.175	0.25
A2	1.30	1.40	1.50
b	0.31	-	0.50
b1	0.30	0.40	0.45
c	0.20	-	0.24
c1	0.19	0.203	0.21
D	4.80	-	5.00
E	5.80	6.00	6.20
E1	3.80	-	4.00
e	1.27 BSC		
L	0.40	-	0.80
L1	1.05 REF		
θ	0°	-	8°