IPZ40N04S5L4R8-VB Datasheet

N-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[f]	Q_g (Typ.)
40	0.0045 at V_{GS} = 10 V	40[g]	9.8 nC
	0.0062 at V_{GS} = 4.5 V	40[g]	

FEATURES

- Trench Power MOSFET
- 100 % R_g and UIS Tested
- Capable of Operating with 5 V Gate Drive

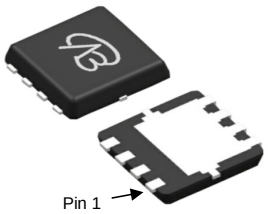
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

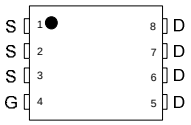
- Synchronous Rectification
- Synchronous Buck Converters
- ORing
- Load Switching
- Motor Drive Switch

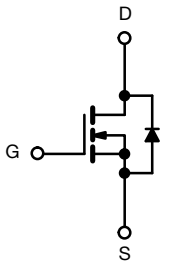
DFN 3x3

Top View Bottom View



Top View





N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	40[g]	A
	T_C = 70 °C		40[g]	
	T_A = 25 °C		19.3[a, b]	
	T_A = 70 °C		15.5[a, b]	
Pulsed Drain Current (t = 100 µs)		I_{DM}	100	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	40[g]	
	T_A = 25 °C		3.1[a, b]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	20	
Single Pulse Avalanche Energy		E_{AS}	20	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	52	W
	T_C = 70 °C		33	
	T_A = 25 °C		3.7[a, b]	
	T_A = 70 °C		2.4[a, b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)[c, d]			260	

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a, e]	t ≤ 10 s	R_{thJA}	26	33	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.9	2.4	

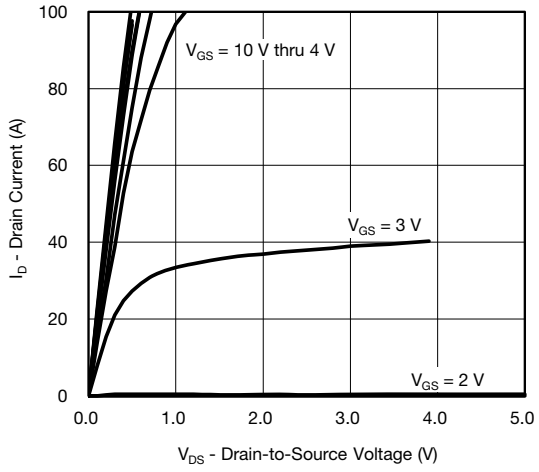
Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. t = 10 s.
c. The DFN 3 x 3 EP is a leadless package. The end of the lead terminal is exposed copper (not platedas a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
e. Maximum under steady state conditions is 81 °C/W.
f. Based on T_C = 25 °C.
g. Package limited.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		56		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 250 µA	1.1		2.2	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			1	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A		0.0045		Ω
		V_{GS} = 4.5 V, I_D = 10 A		0.0062		
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 20 A		65		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz		1330		pF
Output Capacitance	C_{oss}			1200		
Reverse Transfer Capacitance	C_{rss}			66		
Total Gate Charge	Q_g	V_{DS} = 20 V, V_{GS} = 10 V, I_D = 10 A		21.3	32	nC
		V_{DS} = 20 V, V_{GS} = 4.5 V, I_D = 10 A		9.8	15	
Gate-Source Charge	Q_{gs}			3.2		
Gate-Drain Charge	Q_{gd}			2.5		
Output Charge	Q_{oss}	V_{DS} = 20 V, V_{GS} = 0 V		32	48	
Gate Resistance	R_g	f = 1 MHz	0.2	0.9	1.5	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 20 V, R_L = 2 Ω $I_D \cong$ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω		22	44	ns
Rise Time	t_r			65	120	
Turn-Off Delay Time	$t_{d(off)}$			24	45	
Fall Time	t_f			9	18	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 20 V, R_L = 2 Ω $I_D \cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω		11	22	
Rise Time	t_r			11	22	
Turn-Off Delay Time	$t_{d(off)}$			22	44	
Fall Time	t_f			9	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			40	A
Pulse Diode Forward Current (t = 100 µs)	I_{SM}				100	
Body Diode Voltage	V_{SD}	I_S = 4 A, V_{GS} = 0 V		0.75	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 10 A, dI/dt = 100 A/µs, T_J = 25 °C		31	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			17	34	nC
Reverse Recovery Fall Time	t_a			13		ns
Reverse Recovery Rise Time	t_b			18		

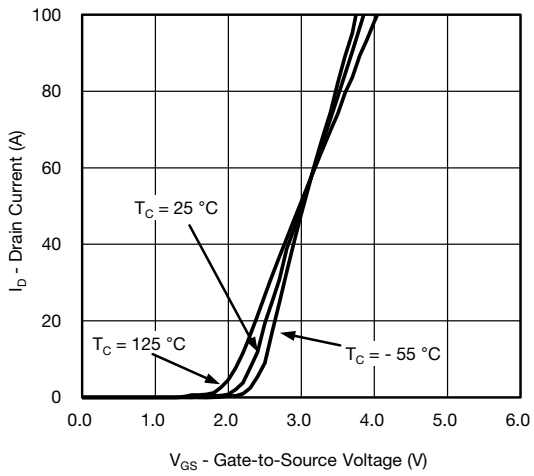
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

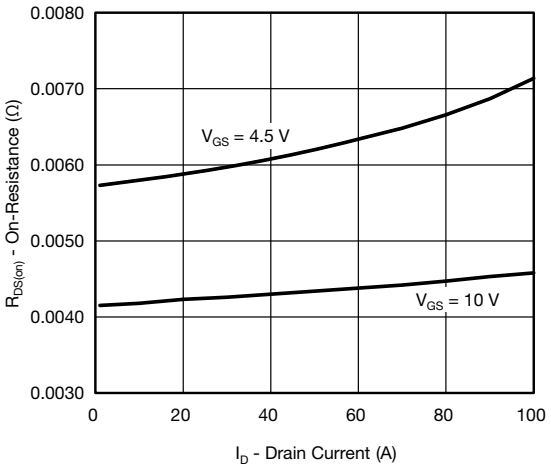
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



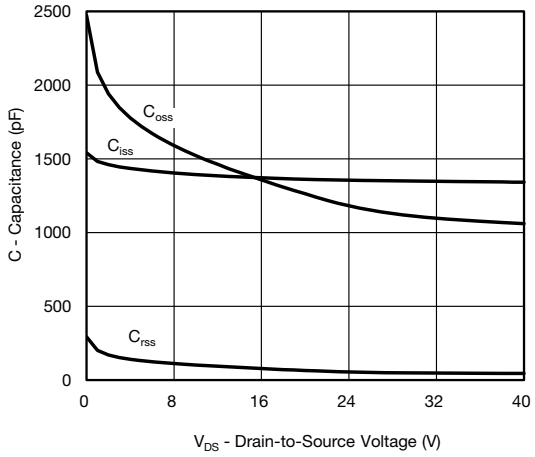
Output Characteristics



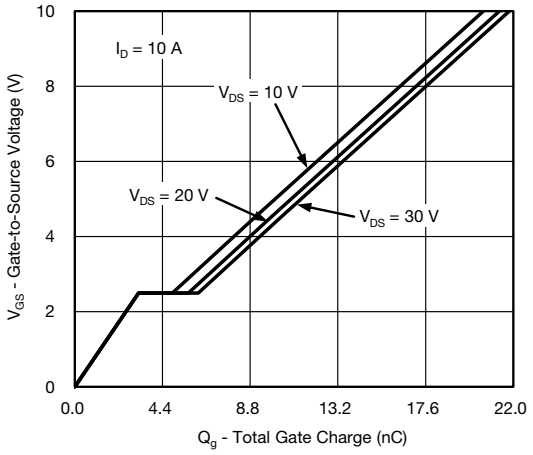
Transfer Characteristics



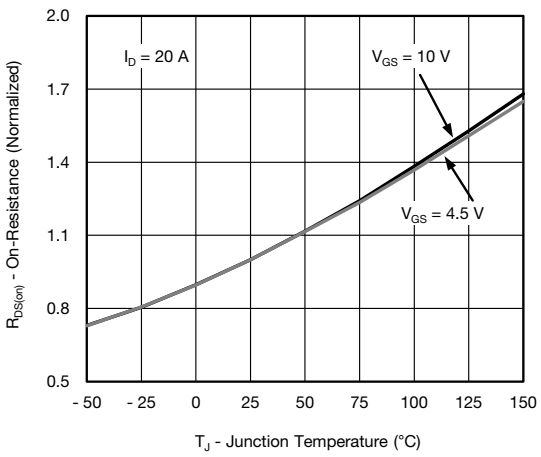
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

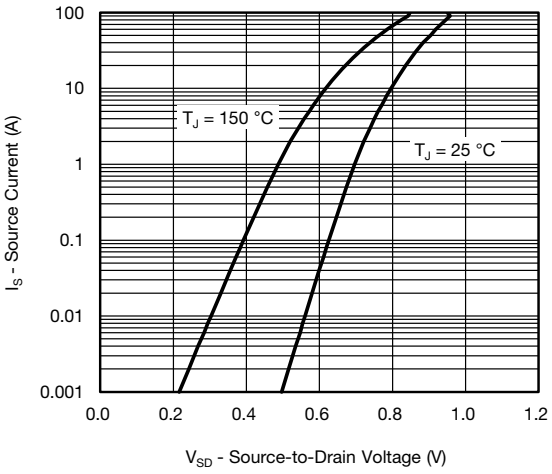


Gate Charge

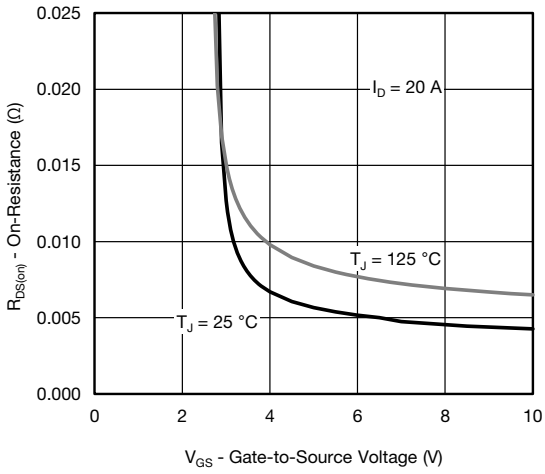


On-Resistance vs. Junction Temperature

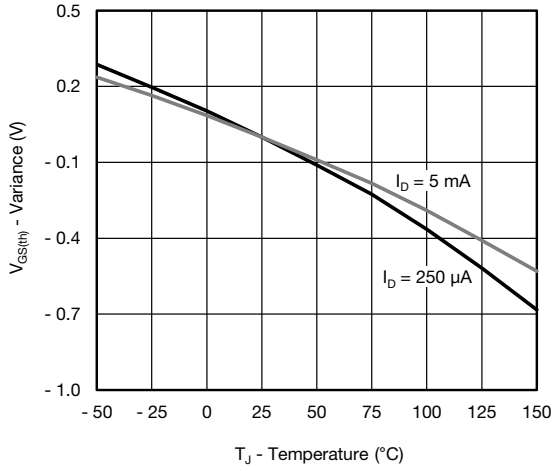
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



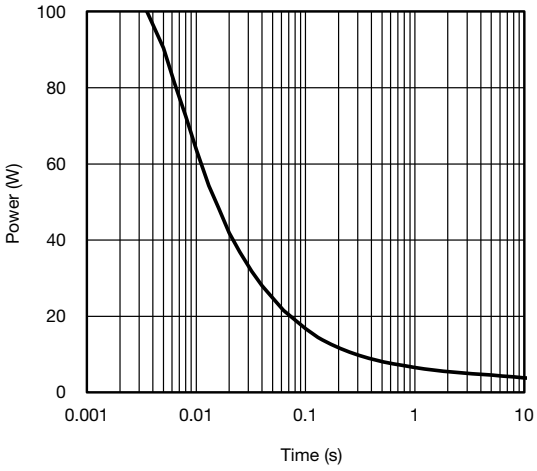
Source-Drain Diode Forward Voltage



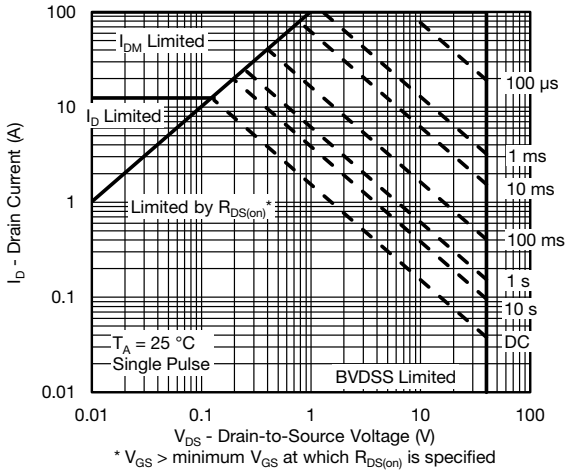
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

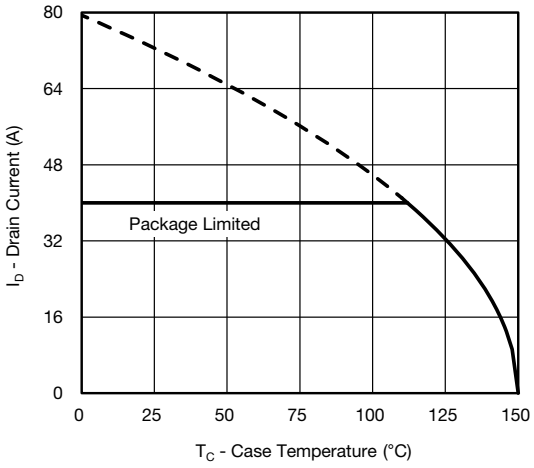


Single Pulse Power, Junction-to-Ambient

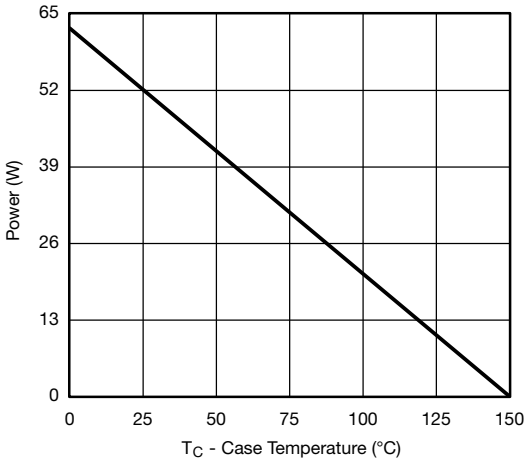


Safe Operating Area, Junction-to-Ambient

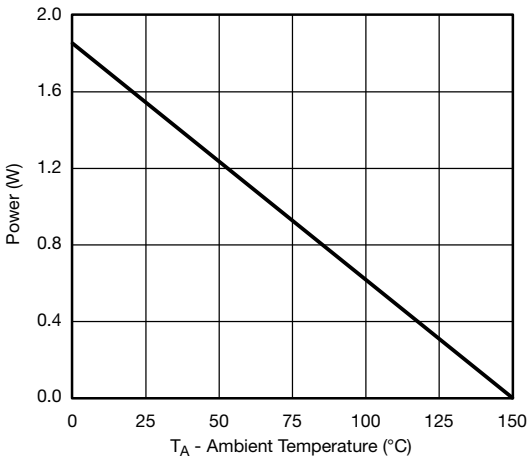
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



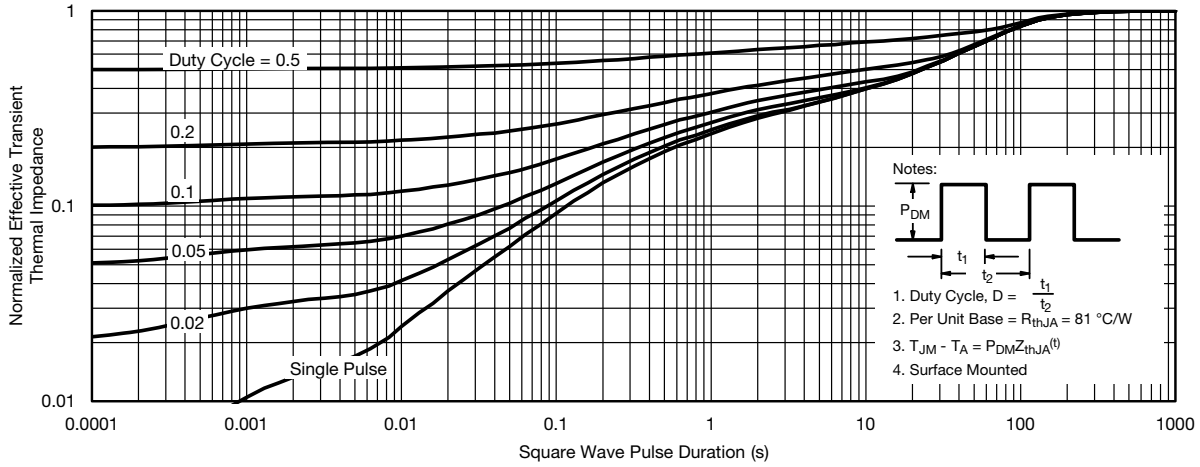
Power, Junction-to-Case



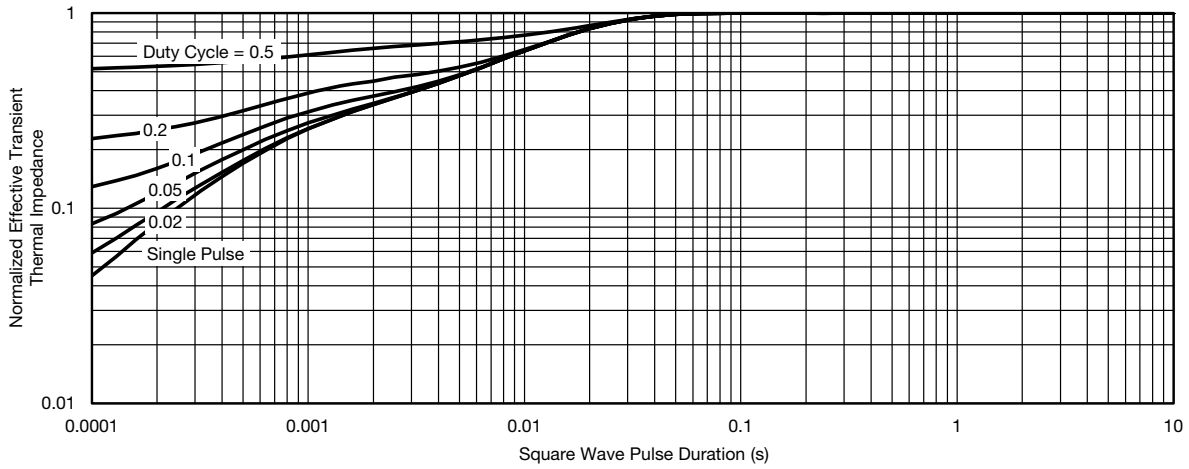
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

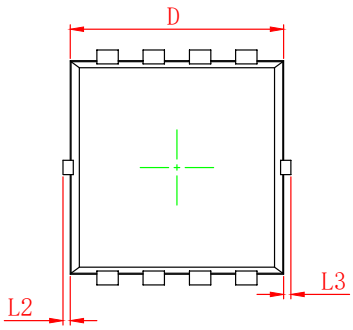


Normalized Thermal Transient Impedance, Junction-to-Ambient

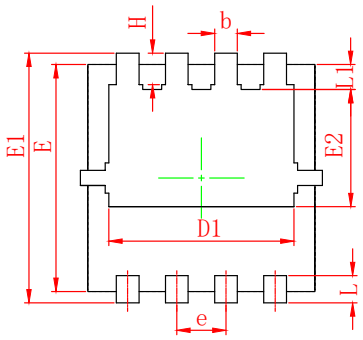


Normalized Thermal Transient Impedance, Junction-to-Case

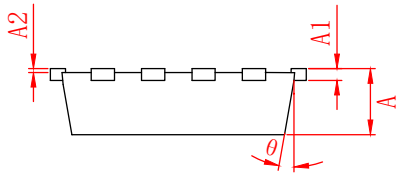
PDFNWB3×3-8L Package Outline Dimensions



Top View
[顶视图]



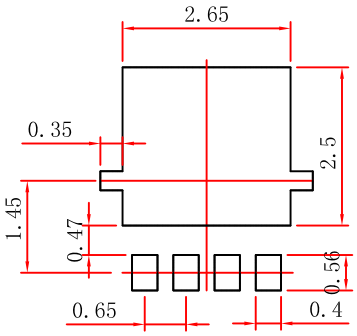
Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.650	0.850	0.026	0.033
A1	0.203REF.		0.008REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.050	2.550	0.081	0.100
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.450	1.650	0.057	0.065
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
Φ	9°	13°	9°	13°

Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

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