# ADP3208D

# 7-Bit, Programmable, Dual-Phase, Mobile, CPU, Synchronous Buck Controller

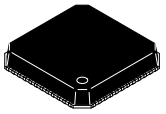
The ADP3208D is a highly efficient, multiphase, synchronous buck switching regulator controller. With its integrated drivers, the ADP3208D is optimized for converting the notebook battery voltage into the core supply voltage required by high performance Intel processors. An internal 7−bit DAC is used to read a VID code directly from the processor and to set the CPU core voltage to a value within the range of 0.3 V to 1.5 V. The phase relationship of the output signals ensures interleaved 2−phase operation.

The ADP3208D uses a multi−mode architecture run at a programmable switching frequency and optimized for efficiency depending on the output current requirement. The ADP3208D switches between single− and dual−phase operation to maximize efficiency with all load conditions. The chip includes a programmable load line slope function to adjust the output voltage as a function of the load current so that the core voltage is always optimally positioned for a load transient. The ADP3208D also provides accurate and reliable short−circuit protection, adjustable current limiting, and a delayed power−good output. The IC supports On−The−Fly (OTF) output voltage changes requested by the CPU.

The ADP3208D is specified over the extended commercial temperature range of −10°C to 100°C and is available in a 48−lead LFCSP.

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LFCSP48
CASE 932AD

**MARKING DIAGRAM**




A = Assembly Location
WL = Wafer Lot
YYWW = Date Code
G = Pb−Free Package

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 36 of this data sheet.

### Features

- Single−Chip Solution
- Fully Compatible with the Intel® IMVP−6+™ Specifications
- Integrated MOSFET Drivers
- Input Voltage Range of 3.3 V to 22 V
- Selectable 1− or 2−Phase Operation with Up to 1 MHz per Phase Switching Frequency
- Guaranteed ±8 mV Worst−Case Differentially Sensed Core Voltage Error Overtemperature
- Automatic Power−Saving Mode Maximizes Efficiency with Light Load During Deeper Sleep Operation
- Soft Transient Control Reduces Inrush Current and Audio Noise
- Active Current Balancing Between Output Phases
- Independent Current Limit and Load Line Setting Inputs for Additional Design Flexibility
- Built−In Power−Good Blanking Supports Voltage Identification (VID) OTF Transients
- 7−Bit, Digitally Programmable DAC with 0.3 V to 1.5 V Output
- Short−Circuit Protection with Latchoff Delay
- Clock Enable Output Delays the CPU Clock Until the Core Voltage is Stable
- Output Load Current Monitor
- This is a Pb−Free Device

### Applications

- Notebook Power Supplies for Next Generation Intel® Processors

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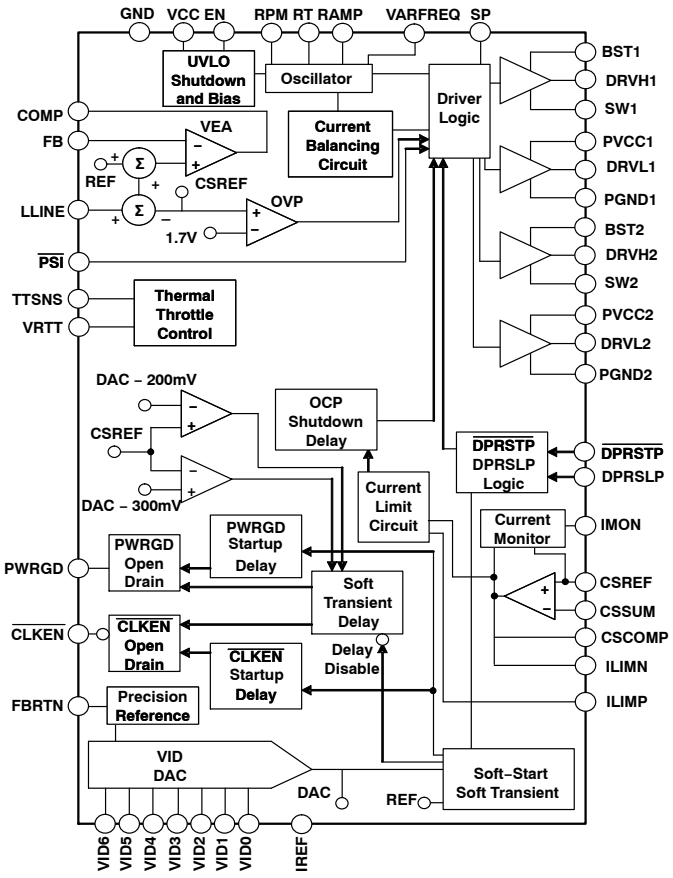



**Figure 1. Functional Block Diagram**

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Rating | Unit |
|---|---|---|
| VCC, PVCC1, PVCC2 | –0.3 to +6.0 | V |
| FBRTN, PGND1, PGND2 | –0.3 to +0.3 | V |
| BST1, BST2<br>DC<br>t < 200 ns | <br>–0.3 to +28<br>–0.3 to +33 | V |
| BST1 to SW1, BST2 to SW2 | –0.3 to +6.0 | V |
| SW1, SW2<br>DC<br>t < 200 ns | <br>–5.0 to +22<br>–10 to +28 | V |
| DRVH1 to SW1, DRVH2 to SW2 | –0.3 to +6.0 | V |
| DRVL1 to PGND1, DRVL2 to PGND2<br>DC<br>t < 200 ns | <br>–0.3 to +6.0<br>–5.0 to +6.0 | V |
| RAMP (In Shutdown) DC | –0.3 to +22 | V |
| All Other Inputs and Outputs | –0.3 to +6.0 | V |
| Storage Temperature | –65 to +150 | °C |
| Operating Ambient Temperature Range | –10 to 100 | °C |
| Operating Junction Temperature | 125 | °C |
| Thermal Impedance ($\theta_{JA}$) 2–Layer Board | 40 | °C/W |
| Lead Temperature<br>Soldering (10 sec)<br>Infrared (15 sec) | <br>300<br>260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

## TEST CIRCUITS

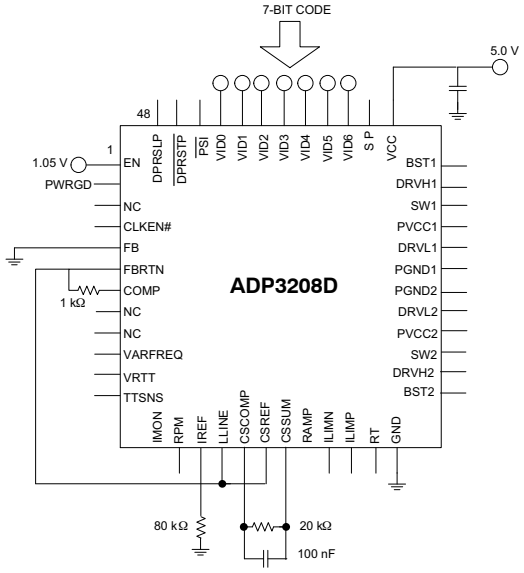



**Figure 2. Closed−Loop Output Voltage Accuracy**

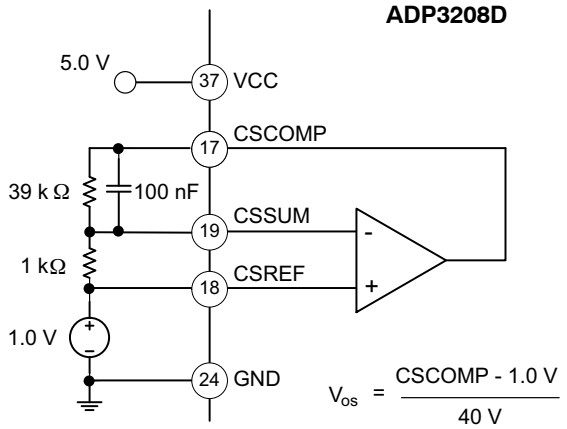



**Figure 3. Current Sense Amplifier, $V_{OS}$**

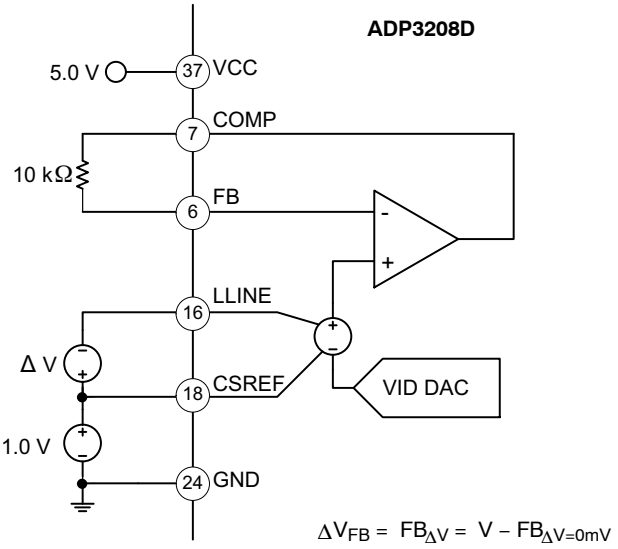



**Figure 4. Positioning Accuracy**

**PIN FUNCTION DESCRIPTIONS**

| Pin No | Mnemonic | Description |
|---|---|---|
| 1 | EN | Enable Input. Driving this pin low shuts down the chip, disables the driver outputs, pulls PWRGD and VRTT low, and pulls $\overline{\text{CLKEN}}$ high. |
| 2 | PWRGD | Power−Good Output. Open−drain output. A low logic state means that the output voltage is outside of the VID DAC defined range. |
| 3 | NC | Not Connected. |
| 4 | $\overline{\text{CLKEN}}$ | Clock Enable Output. Open−drain output. A low logic state enables the CPU internal PLL clock to lock to the external clock. |
| 5 | FBRTN | Feedback Return Input/Output. This pin remotely senses the CPU core voltage. It is also used as the ground return for the VID DAC and the voltage error amplifier blocks. |
| 6 | FB | Voltage Error Amplifier Feedback Input. The inverting input of the voltage error amplifier. |
| 7 | COMP | Voltage Error Amplifier Output and Frequency Compensation Point. |
| 8 | NC | Not Connected. |
| 9 | IRPM/NC | RPM Mode Timing Control Input. A resistor between this pin or RPM pin to ground sets the RPM mode turn−on threshold voltage. If a resistor is connected between this pin to ground, RPM pin must remain floating and not connected. |
| 10 | VARFREQ | Variable Frequency Enable Input. A high logic state enables the PWM clock frequency to vary with VID code. |
| 11 | VRTT | Voltage Regulator Thermal Throttling Output. Logic high state indicates that the voltage regulator temperature at the remote sensing point exceeded a set alarm threshold level. |
| 12 | TTSNS | Thermal Throttling Sense and Crowbar Disable Input. A resistor divider where the upper resistor is connected to VCC, the lower resistor (NTC thermistor) is connected to GND, and the center point is connected to this pin and acts as a temperature sensor half bridge. Connecting TTSNS to GND disables the thermal throttling function and disables the crowbar, or Overvoltage Protection (OVP), feature of the chip. |
| 13 | IMON | Current Monitor Output. This pin sources a current proportional to the output load current. A resistor to FBRTN sets the current monitor gain. |
| 14 | RPM | RPM Mode Timing Control Input. A resistor between this pin or IRPM pin to ground sets the RPM mode turn−on threshold voltage. If a resistor is connected between this pin to ground, IRPM pin must remain floating. |
| 15 | IREF | This pin sets the internal bias currents. A 80 kΩ resistor is connected from this pin to ground. |
| 16 | LLINE | Load Line Programming Input. The center point of a resistor divider connected between CSREF and CSCOMP can be tied to this pin to set the load line slope. |
| 17 | CSCOMP | Current Sense Amplifier Output and Frequency Compensation Point. |
| 18 | CSREF | Current Sense Reference Input. This pin must be connected to the common point of the output inductors. The node is shorted to GND through an internal switch when the chip is disabled to provide soft stop transient control of the converter output voltage. |
| 19 | CSSUM | Current Sense Summing Input. External resistors from each switch node to this pin sum the inductor currents to provide total current information. |
| 20 | RAMP | PWM Ramp Slope Setting Input. An external resistor from the converter input voltage node to this pin sets the slope of the internal PWM stabilizing ramp used for phase−current balancing. |
| 21 | ILIMN | Current Limit Set. An external resistor from ILIMN to ILIMP sets the current limit threshold of the converter. |
| 22 | ILIMP | Current Limit Set. An external resistor from ILIMN to ILIMP sets the current limit threshold of the converter. |
| 23 | RT | PWM Oscillator Frequency Setting Input. An external resistor from this pin to GND sets the PWM oscillator frequency. |
| 24 | GND | Analog and Digital Signal Ground. |
| 25 | BST2 | High−Side Bootstrap Supply for Phase 2. A capacitor from this pin to SW2 holds the bootstrapped voltage while the high−side MOSFET is on. |
| 26 | DRVH2 | High−Side Gate Drive Output for Phase 2. |
| 27 | SW2 | Current Balance Input for Phase 2 and Current Return for High−Side Gate Drive. |
| 28 | PVCC2 | Power Supply Input/Output of Low−Side Gate Driver for Phase 2. |
| 29 | DRVL2 | Low−Side Gate Drive Output for Phase 2. |
| 30 | PGND2 | Low−Side Driver Power Ground for Phase 2. |

| Pin No | Mnemonic | Description |
|---|---|---|
| 31 | PGND1 | Low−Side Driver Power Ground for Phase 1. |
| 32 | DRVL1 | Low−Side Gate Drive Output for Phase 1. |
| 33 | PVCC1 | Power Supply Input/Output of Low−Side Gate Driver for Phase 1. |
| 34 | SW1 | Current Balance Input for Phase 1 and Current Return For High−Side Gate Drive. |
| 35 | DRVH1 | High−Side Gate Drive Output for Phase 1. |
| 36 | BST1 | High−Side Bootstrap Supply for Phase 1. A capacitor from this pin to SW1 holds the bootstrapped voltage while the high−side MOSFET is on. |
| 37 | VCC | Power Supply Input/Output of the Controller. |
| 38 | SP | Single−Phase Select Input. Logic high state sets single−phase configuration. |
| 39 to 45 | VID6 to VID0 | Voltage Identification DAC Inputs. A 7−bit word (the VID code) programs the DAC output voltage, the reference voltage of the voltage error amplifier without a load (see the VID code Table 3). |
| 46 | $\overline{\text{PSI}}$ | Power State Indicator Input. Driving this pin low forces the controller to operate in single−phase mode. |
| 47 | $\overline{\text{DPRSTP}}$ | Deeper Stop Control Input. The logic state of this pin is usually complementary to the state of the DPRSLP pin; however, during slow deeper sleep exit, both pins are logic low. |
| 48 | DPRSLP | Deeper Sleep Control Input. |

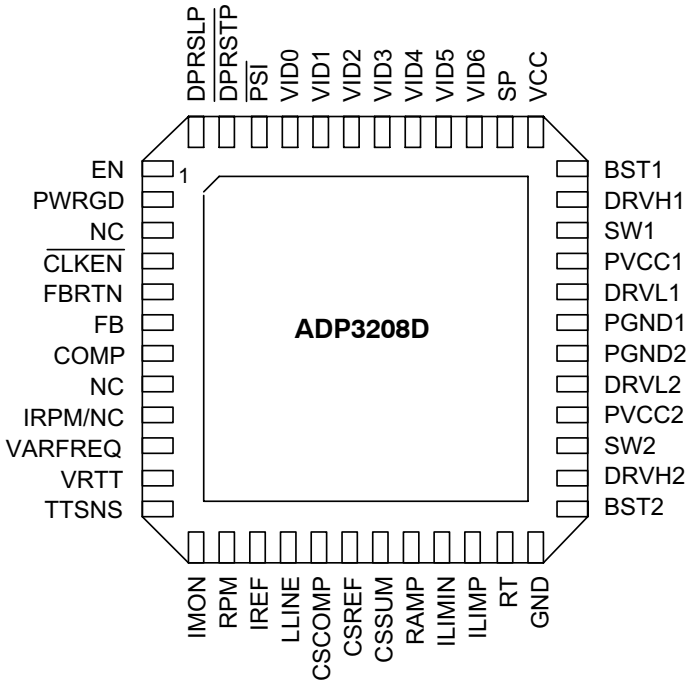



**Figure 5. Pin Configuration**
(Top View)

**ELECTRICAL CHARACTERISTICS** $V_{CC}$ = $P_{VCC1}$ = $P_{VCC2}$ = BST1 = BST2 = High = 5.0V, FBRTN = GND = SW1 = SW2 = PGND1 = PGND2 = Low = 0 V, EN = VATFREQ = High, DPRSLP = 0 V, $\overline{PSI}$ = 1.05 V, $V_{VID}$ = 1.2000 V, $T_A$ = −40°C to 100°C, unless otherwise noted (Note 1). Current entering a pin (sunk by the device) has a positive sign. $R_{REF}$ = 80 kΩ.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VOLTAGE CONTROL − Voltage Error Amplifier (VEAMP)** | | | | | | |
| FB, LLINE Voltage Range (Note 2) | $V_{FB}$, $V_{LLINE}$ | Relative to CSREF = $V_{DAC}$ | −200 | | +200 | mV |
| FB, LLINE Offset Voltage (Note 2) | $V_{OSVEA}$ | Relative to CSREF = $V_{DAC}$ | −0.5 | | +0.5 | mV |
| FB LLINE Bias Current (Note 2) | $I_{FB}$ | | −100 | | 100 | A |
| LLINE Positioning Accuracy | $V_{FB}$ − $V_{VID}$ | Measured on FB relative to $V_{VID}$, LLINE forced 80 mV below CSREF | −78 | −80 | −82 | mV |
| COMP Voltage Range | $V_{COMP}$ | Operating Range | 0.85 | | 4.0 | V |
| COMP Current | $I_{COMP}$ | COMP = 2.0 V, CSREF = $V_{DAC}$<br>FB forced 200 mV below CSREF<br>FB forced 200 mV above CSREF | | <br>−0.75<br>6.0 | | mA |
| COMP Slew Rate | $SR_{COMP}$ | $C_{COMP}$ = 10 pF, CSREF = $V_{DAC}$,<br>Open loop configuration<br>FB forced 200 mV below CSREF<br>FB forced 200 mV above CSREF | | <br><br>15<br>−20 | | V/μs |
| Gain Bandwidth (Note 2) | GBW | Non−inverting unit gain configuration, $R_{FB}$ = 1 kΩ | | 20 | | MHz |
| **VID DAC VOLTAGE REFERENCE** | | | | | | |
| $V_{DAC}$ Voltage Range (Note 3) | | See VID Code Table | 0 | | 1.5 | V |
| $V_{DAC}$ Accuracy | $V_{FB}$ − $V_{VID}$ | Measured on FB (includes offset), relative to $V_{VID}$, for VID table see Table 3,<br>$V_{VID}$ = 1.2125 V to 1.5000 V<br>$V_{VID}$ = 0.3000 V to 1.2000 V | <br><br>−9.0<br>−7.5 | | <br><br>+9.0<br>+7.5 | mV |
| $V_{DAC}$ Differential Non−linearity (Note 2) | | | −1.0 | | +1.0 | LSB |
| $V_{DAC}$ Line Regulation | $\Delta V_{FB}$ | $V_{CC}$ = 4.75 V to 5.25 V | | 0.05 | | % |
| $V_{DAC}$ Boot Voltage (Note 2) | $V_{BOOTFB}$ | Measured during boot delay period | | 1.200 | | V |
| Soft−Start Delay (Note 2) | $t_{DSS}$ | Measured from EN pos edge to FB = 50 mV | | 200 | | μs |
| Soft−Start Time | $t_{SS}$ | Measured from EN pos edge to FB settles to $V_{BOOT}$ = 1.2 V within −5% | | 1.7 | | ms |
| Boot Delay | $t_{BOOT}$ | Measured from FB settling to $V_{BOOT}$ = 1.2 V within −5% to $\overline{CLKEN}$ neg edge | | 150 | | μs |
| $V_{DAC}$ Slew Rate | | Soft−Start<br>Non−LSB VID step, DPRSLP = H, Slow C4 Entry/Exit<br>Non−LSB VID step, DPRSLP = L, Fast C4 Exit | | 0.0625<br>0.25<br><br>1.0 | | LSB/μs |
| FBRTN Current | $I_{FBRTN}$ | | | 90 | 200 | μA |
| **VOLTAGE MONITORING AND PROTECTION − Power Good** | | | | | | |
| CSREF Undervoltage Threshold | $V_{UVCSREF}$ | Relative to DAC Voltage:<br>= 0.5 V to 1.5 V<br>= 0.3 V to 0.4875 V | <br>−360<br>−360 | <br>−300<br>−300 | <br>−240<br>−160 | mV |
| CSREF Overvoltage Threshold | $V_{OVCSREF}$ | Relative to nominal DAC Voltage | 150 | 200 | 250 | mV |
| CSREF Crowbar Voltage Threshold | $V_{CBCSREF}$ | Relative to FBRTN | 1.57 | 1.7 | 1.78 | V |
| CSREF Reverse Voltage Threshold | $V_{RVCSREF}$ | Relative to FBRTN, Latchoff mode:<br>CSREF Falling<br>CSREF Rising | <br>−350 | <br>−300<br>−70 | <br><br>−5.0 | mV |

1. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).
2. Guaranteed by design or bench characterization, not production tested.
3. Timing is referenced to the 90% and 10% points, unless otherwise noted.

**ELECTRICAL CHARACTERISTICS** $V_{CC}$ = $P_{VCC1}$ = $P_{VCC2}$ = BST1 = BST2 = High = 5.0V, FBRTN = GND = SW1 = SW2 = PGND1 = PGND2 = Low = 0 V, EN = VATFREQ = High, DPRSLP = 0 V, $\overline{PSI}$ = 1.05 V, $V_{VID}$ = 1.2000 V, $T_A$ = −40°C to 100°C, unless otherwise noted (Note 1). Current entering a pin (sunk by the device) has a positive sign. $R_{REF}$ = 80 kΩ.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VOLTAGE MONITORING AND PROTECTION − Power Good** | | | | | | |
| PWRGD Low Voltage | $V_{PWRGD}$ | $I_{PWRGD(SINK)}$ = 4 mA | | 50 | 150 | mV |
| PWRGD High, Leakage Current | $I_{PWRGD}$ | $V_{PWRDG}$ = 5.0 V | | | 0.1 | μA |
| PWRGD Startup Delay | $T_{SSPWRGD}$ | Measured from CLKEN neg edge to PWRGD Pos Edge | | 8.0 | | ms |
| PWRGD Latchoff Delay | $T_{LOFFPWRGD}$ | Measured from Out−off−Good−Window event to Latchoff (switching stops) | | 8.0 | | ms |
| PWRGD Propagation Delay (Note 3) | $T_{PDPWRGD}$ | Measured from Out−off−Good−Window event to PWRGD neg edge | | 200 | | ns |
| Crowbar Latchoff Delay (Note 2) | $T_{LOFFCB}$ | Measured from Crowbar event to Latchoff (switching stops) | | 200 | | ns |
| PWRGD Masking Time | | Triggered by any VID change or OCP event | | 100 | | μs |
| CSREF Soft−Stop Resistance | | EN = L or Latchoff condition | | 70 | | Ω |
| **CURRENT CONTROL − Current Sense Amplifier (CSAMP)** | | | | | | |
| CSSUM, CSREF Common−Mode Range (Note 2) | | Voltage range of interest | 0 | | 2.0 | V |
| CSSUM, CSREF Offset Voltage | $V_{OSCSA}$ | $T_A$ = 25°C<br>CSREF − CSSUM, $T_A$ = −10°C to 85°C<br>CSREF − CSSUM, $T_A$ = −40°C to 85°C | −0.5<br>−1.7<br>−1.8 | | +0.5<br>+1.7<br>+1.8 | mV |
| CSSUM Bias Current | $I_{BCSSUM}$ | | −50 | | +50 | nA |
| CSREF Bias Current | $I_{BCSREF}$ | | −120 | | +120 | nA |
| CSCOMP Voltage Range (Note 2) | | Operating Range | 0.05 | | 2.0 | V |
| CSCOMP Current | $I_{CSCOMPsource}$<br>$I_{CSCOMPsink}$ | CSCOMP = 2.0 V<br>CSSUM forced 200 mV below CSREF<br>CSSUM forced 200 mV above CSREF | | −750<br>1.0 | | μA<br>mA |
| CSCOMP Slew Rate | | $C_{CSCOMP}$ = 10 pF, Open Loop Configuration<br>CSSUM forced 200 mV below CSREF<br>CSSUM forced 200 mV above CSREF | | <br>10<br>−10 | | V/μs |
| Gain Bandwidth (Note 2) | $GBW_{CSA}$ | Non−inverting unit gain configuration<br>$R_{FB}$ = 1 kΩ | | 20 | | MHz |
| **CURRENT MONITORING AND PROTECTION** | | | | | | |
| Current Reference $I_{REF}$ Voltage | $V_{REF}$ | $R_{REF}$ = 80 kΩ to set $I_{REF}$ = 20 μA | 1.55 | 1.6 | 1.65 | V |
| Current Limiter (OCP) Current Limit Threshold | $V_{LIMTH}$ | Measured from CSCOMP to CSREF,<br>$R_{LIM}$ = 4.5 kΩ,<br>2−ph configuration, $\overline{PSI}$ = H<br>2−ph configuration, $\overline{PSI}$ = L<br>1−ph configuration<br>Measured from CSCOMP to CSREF,<br>$R_{LIM}$ = 4.5 kΩ,<br>3−ph configuration, $\overline{PSI}$ = H<br>3−ph configuration, $\overline{PSI}$ = L<br>1−ph configuration | <br><br>−70<br>−32<br>−70<br><br><br>−70<br>−15<br>−70 | <br><br>−95<br>−47.5<br>−95<br><br><br>−90<br>−30<br>−90 | <br><br>−115<br>−65<br>−115<br><br><br>−115<br>−50<br>−115 | mV |
| Current Limit Latchoff Delay | | Measured from OCP event to PWRGD deassertion | | 8.0 | | ms |

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| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **CURRENT MONITOR** | | | | | | |
| Current Gain Accuracy | $I_{MON}/I_{LIM}$ | Measured from $I_{LIMP}$ to $I_{MON}$<br>$I_{LIM}$ = −20 μA<br>$I_{LIM}$ = −10 μA<br>$I_{LIM}$ = −5 μA | <br>9.5<br>9.3<br>9.0 | <br>10<br>10<br>10 | <br>10.5<br>10.7<br>11.0 | |
| $I_{MON}$ Clamp Voltage | $V_{MAXMON}$ | Relative to FBRTN, $I_{LIMP}$ = −30 μA | 1.0 | | 1.05 | V |
| **PULSE WIDTH MODULATOR – Clock Oscillator** | | | | | | |
| $R_T$ Voltage | $V_{RT}$ | VARFREQ = High, $R_T$ = 125 kΩ,<br>$V_{VID}$ = 1.5000 V<br>VARFREQ = Low, See also $V_{RT}(V_{VID})$ formula | 1.22<br><br>0.98 | 1.25<br><br>1.0 | 1.27<br><br>1.02 | V |
| PWM Clock Frequency Range (Note 2) | $f_{CLK}$ | Operating Range | 0.3 | | 3.0 | MHz |
| PWM Clock Frequency | $f_{CLK}$ | $T_A$ = 25°C, $V_{VID}$ = 1.2000 V<br>$R_T$ = 73 kΩ<br>$R_T$ = 125 kΩ<br>$R_T$ = 180 kΩ | <br>1200<br>680<br>400 | <br>1470<br>920<br>640 | <br>1720<br>1120<br>840 | kHz |
| **RAMP GENERATOR** | | | | | | |
| RAMP Voltage | $V_{RAMP}$ | EN = high, $I_{RAMP}$ = 30 μA<br>EN = low | 0.9 | 1.0<br>$V_{IN}$ | 1.1 | V |
| RAMP Current Range (Note 2) | $I_{RAMP}$ | EN = high<br>EN = low, RAMP = 19 V | 1.0<br>−0.5 | | 100<br>+0.5 | μA |
| **PWM COMPARATOR** | | | | | | |
| PWM Comparator Offset (Note 2) | $V_{OSRPM}$ | $V_{RAMP}$ − $V_{COMP}$ | −3.0 | | 3.0 | mV |
| **RPM COMPARATOR** | | | | | | |
| RPM Current | $I_{RPM}$ | $V_{VID}$ = 1.2 V, $R_T$ = 125 kΩ,<br>VARFREQ = High, See also $I_{RPM}(R_T)$ formula | | −8.8 | | μA |
| RPM Comparator Offset (Note 2) | $V_{OSRPM}$ | $V_{COMP}$ − (1 +$V_{RPM}$) | −3.0 | | 3.0 | mV |
| **EPWM CLOCK SYNC** | | | | | | |
| Trigger Threshold (Note 2) | | Relative to COMP sampled $T_{CLK}$ earlier<br>2−phase configuration<br>1−phase configuration | | <br>400<br>450 | | mV |
| **SWITCH AMPLIFIER** | | | | | | |
| SW Common Mode Range (Note 2) | $V_{SW(X)CM}$ | Operating Range for current sensing | −600 | | +200 | mV |
| SW Resistance | $R_{SW_PGND(X)}$ | Measured from SW to PGND | | 3.0 | | kΩ |
| **ZERO CURRENT SWITCHING COMPARATOR** | | | | | | |
| SW ZCS Threshold | $V_{DCM(SW1)}$ | DCM mode, DPRSLP = 3.3 V | | −6.0 | | mV |
| Masked Off Time | $t_{OFFMSKD}$ | Measured from DRVH neg edge to DRVH pos edge at max frequency of operation | | 700 | | ns |
| **SYSTEM I/O BUFFERS VID[6:0], $\overline{PSI}$ INPUTS** | | | | | | |
| Input Voltage | | Refers to driving signal level<br>Logic low, $I_{sink} \geq$ 1 μA<br>Logic high, $I_{source} \leq$ −5 μA | <br><br>0.7 | | <br>0.3 | V |
| Input Current | | V = 0.2 V<br>VID[6:0], DPRSLP (active pulldown to GND)<br>$\overline{PSI}$ (active pullup to $V_{CC}$) | | <br>−1.0<br>+1.0 | | μA |
| VID Delay Time (Note 2) | | Any VID edge to FB change 10% | 200 | | | ns |

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2. Guaranteed by design or bench characterization, not production tested.
3. Timing is referenced to the 90% and 10% points, unless otherwise noted.

**ELECTRICAL CHARACTERISTICS** $V_{CC}$ = $P_{VCC1}$ = $P_{VCC2}$ = BST1 = BST2 = High = 5.0V, FBRTN = GND = SW1 = SW2 = PGND1 = PGND2 = Low = 0 V, EN = VATFREQ = High, DPRSLP = 0 V, $\overline{PSI}$ = 1.05 V, $V_{VID}$ = 1.2000 V, $T_A$ = −40°C to 100°C, unless otherwise noted (Note 1). Current entering a pin (sunk by the device) has a positive sign. $R_{REF}$ = 80 kΩ.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DPRSLP** | | | | | | |
| Input Voltage | | Refers to driving signal level<br>Logic low, $I_{sink} \geq 1$ μA<br>Logic high, $I_{source} \leq -5$ μA | <br><br>2.3 | | <br><br>1.0 | V |
| Input Current | | DPRSLP = low<br>DPRSLP = high | | −1.0<br>+2.0 | | μA |
| **$\overline{\text{DPRSTP}}$** | | | | | | |
| Input Voltage | | Refers to driving signal level<br>Logic low, $I_{sink} \geq 1$ μA<br>Logic high, $I_{source} \leq -5$ μA | <br><br>0.7 | | <br><br>0.3 | V |
| Input Current | | | | 1.0 | | μA |
| **VARFREQ, SP** | | | | | | |
| Input Voltage | | Refers to driving signal level<br>Logic low, $I_{sink} \geq 1$ μA<br>Logic high, $I_{source} \leq -5$ μA | <br><br>4.0 | | <br><br>0.7 | V |
| Input Current | | | | 1.0 | | μA |
| **EN INPUT** | | | | | | |
| Input Voltage | | Refers to driving signal level<br>Logic low, $I_{sink} \geq 1$ μA<br>Logic high, $I_{source} \leq -5$ μA | <br><br>2.3 | | <br><br>1.0 | V |
| Input Current | | EN = L or EN = H (Static)<br>0.8 V < EN < 1.6 V (During Transition) | | 10<br>70 | | nA<br>μA |
| **$\overline{\text{CLKEN}}$ OUTPUT** | | | | | | |
| Output Low Voltage | | Logic low, $I_{sink}$ = 4 mA | | 50 | 100 | mV |
| Output High, Leakage Current | | Logic high, $V_{CLKEN} = V_{CC}$ | | | 1.0 | μA |
| **THERMAL MONITORING AND PROTECTION** | | | | | | |
| TTSNS Voltage Range (Note 2) | | | 0 | | 5.0 | V |
| TTSNS Threshold | | $V_{CC}$ = 5.0 V, TTSNS is falling | 2.45 | 2.5 | 2.55 | V |
| TTSNS Hysteresis | | | 50 | 110 | | mV |
| TTSNS Bias Current | | TTSNS = 2.6 V | −2.0 | | 2.0 | μA |
| VRTT Output Voltage | $V_{VRTT}$ | Logic low, $I_{VRTT(SINK)}$ = 400 μA<br>Logic high, $I_{VRTT(SOURCE)}$ = −400 μA | <br>4.0 | 10<br>5.0 | 100 | mV<br>V |
| **SUPPLY** | | | | | | |
| Supply Voltage Range | $V_{CC}$ | | 4.5 | | 5.5 | V |
| Supply Current | | EN = H<br>EN = 0 V | | 6.0<br>15 | 10<br>50 | mA<br>μA |
| $V_{CC}$ OK Threshold | $V_{CCOK}$ | $V_{CC}$ is Rising | | 4.3 | 4.5 | V |
| $V_{CC}$ UVLO Threshold | $V_{CCUVLO}$ | $V_{CC}$ is Falling | 4.0 | 4.1 | | V |
| $V_{CC}$ Hysteresis (Note 2) | | | | 210 | | mV |
| **HIGH−SIDE MOSFET DRIVER** | | | | | | |
| Pullup Resistance, Sourcing Current | | BST = PVCC | | 1.8 | 3.3 | Ω |
| Pulldown Resistance, Sinking Current | | BST = PVCC | | 1.0 | 3.0 | Ω |

1. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).
2. Guaranteed by design or bench characterization, not production tested.
3. Timing is referenced to the 90% and 10% points, unless otherwise noted.

**ELECTRICAL CHARACTERISTICS** $V_{CC}$ = $P_{VCC1}$ = $P_{VCC2}$ = BST1 = BST2 = High = 5.0V, FBRTN = GND = SW1 = SW2 = PGND1 = PGND2 = Low = 0 V, EN = VATFREQ = High, DPRSLP = 0 V, $\overline{PSI}$ = 1.05 V, $V_{VID}$ = 1.2000 V, $T_A$ = −40°C to 100°C, unless otherwise noted (Note 1). Current entering a pin (sunk by the device) has a positive sign. $R_{REF}$ = 80 kΩ.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **HIGH−SIDE MOSFET DRIVER** | | | | | | |
| Transition Times | $tr_{DRVH}$<br>$tf_{DRVH}$ | BST = PVCC, $C_L$ = 3 nF, Figure 6<br>BST = PVCC, $C_L$ = 3 nF, Figure 6 | | 15<br>13 | 35<br>31 | ns |
| Dead Delay Times | $tpdh_{DRVH}$ | BST = PVCC, Figure 6 | | 39 | 50 | ns |
| BST Quiescent Current | | EN = L (Shutdown)<br>EN = H, no switching | | 0.6<br>15 | 5.0 | μA |
| **LOW−SIDE MOSFET DRIVER** | | | | | | |
| Pullup Resistance, Sourcing Current | | BST = PVCC | | 1.6 | 3.3 | Ω |
| Pulldown Resistance, Sinking Current | | BST = PVCC | | 0.8 | 2.5 | Ω |
| Transition Times | $tr_{DRVL}$<br>$tf_{DRVL}$ | $C_L$ = 3 nF, Figure 6<br>$C_L$ = 3 nF, Figure 6 | | 15<br>14 | 35<br>35 | ns |
| Progation Delay Times | $tpdh_{DRVL}$ | $C_L$ = 3 nF, Figure 6 | | 10 | 45 | ns |
| SW Transition Times | $t_{TOSW}$ | DRVH = L, SW = 2.5 V | 210 | 250 | 450 | ns |
| SW Off Threshold | $V_{OFFSW}$ | | | 1.6 | | V |
| PVCC Quiescent Current | | EN = L (Shutdown)<br>EN = H, no switching | | 1.0<br>240 | 15 | μA |
| **BOOTSTRAP RECTIFIER SWITCH** | | | | | | |
| On Resistance | | EN = L or EN = H and DRVL = H | 3.0 | 6.0 | 1.0 | Ω |

1. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).
2. Guaranteed by design or bench characterization, not production tested.
3. Timing is referenced to the 90% and 10% points, unless otherwise noted.

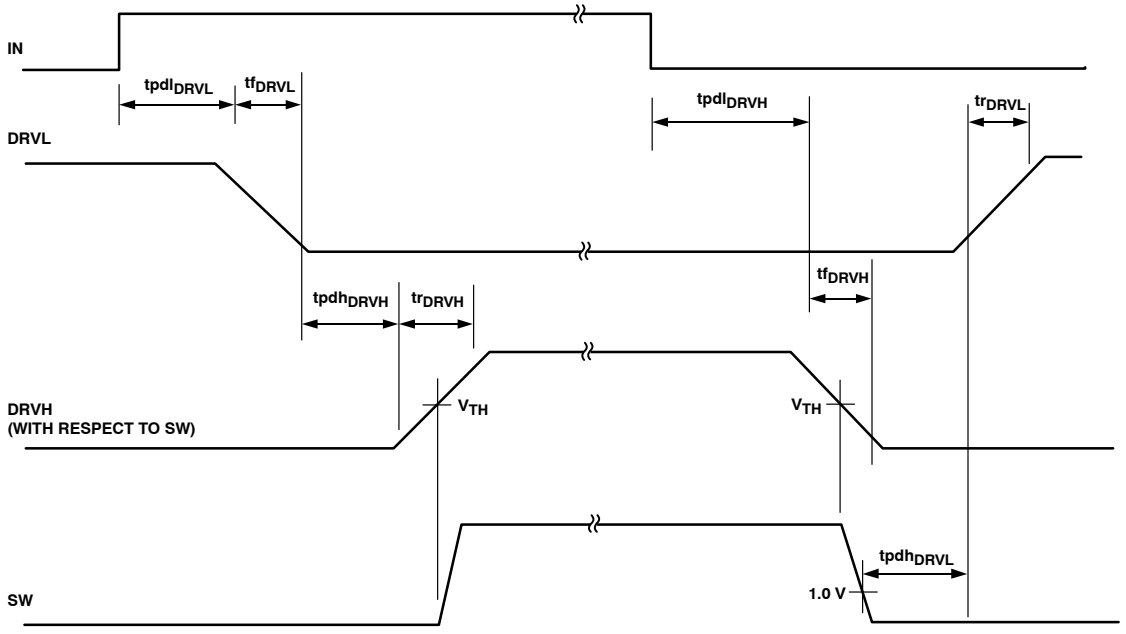



**Figure 6. Timing Diagram** (Note 3)

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{VID}$ = 1.5 V, $T_A$ = 20°C to 100°C, unless otherwise noted.

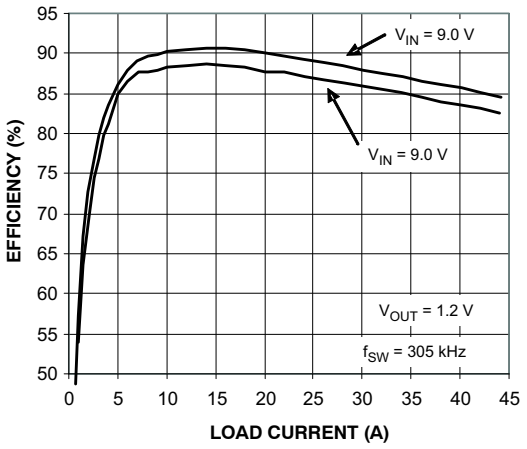



Figure 7. PWM Mode Efficiency vs. Load Current

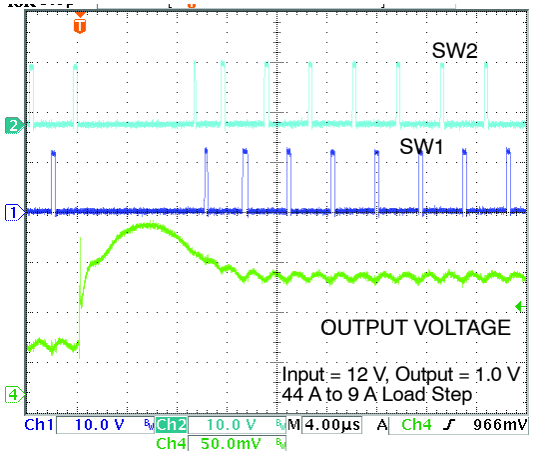



Figure 8. Load Transient with 2−Phases

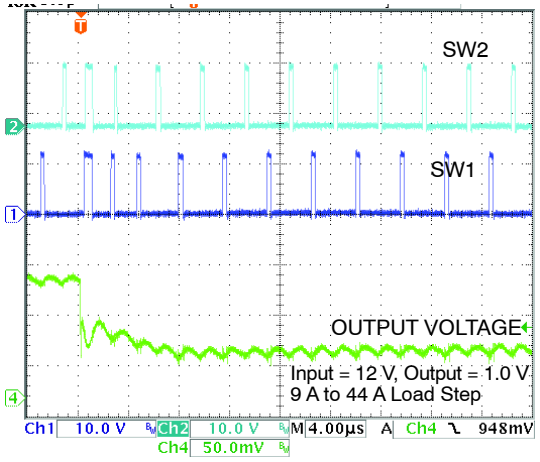



Figure 9. Load Transient with 2 Phases

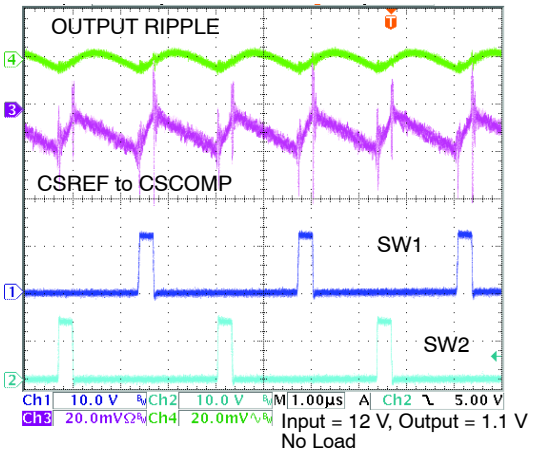



Figure 10. Switching Waveforms in 2 Phase

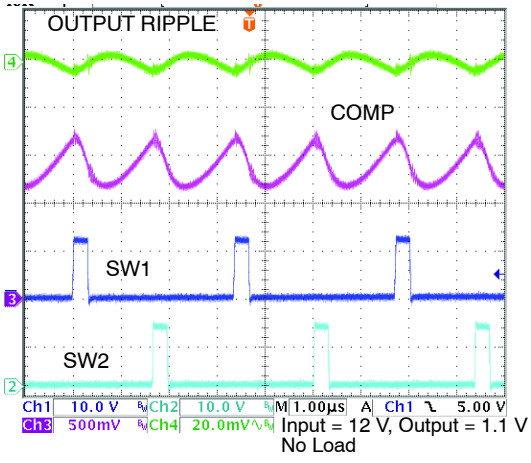



Figure 11. Switching Waveforms in 2−Phase

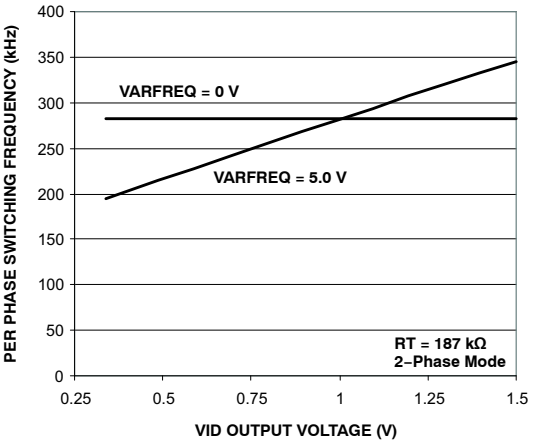



Figure 12. Switching Frequency vs. VID Output Voltage in PWM Mode

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{VID}$ = 1.5 V, $T_A$ = 20°C to 100°C, unless otherwise noted.

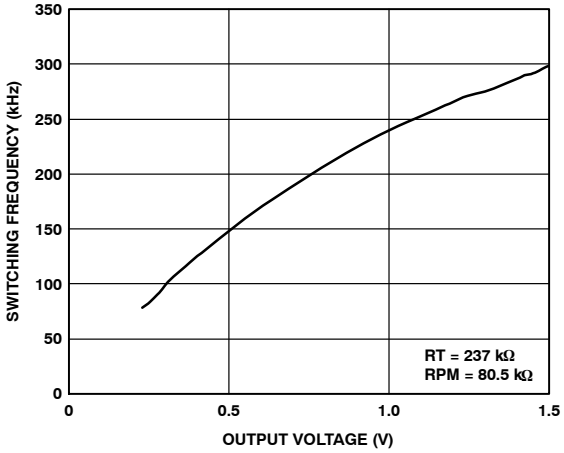



**Figure 13. Switching Frequency vs. Output Voltage in RPM Mode**

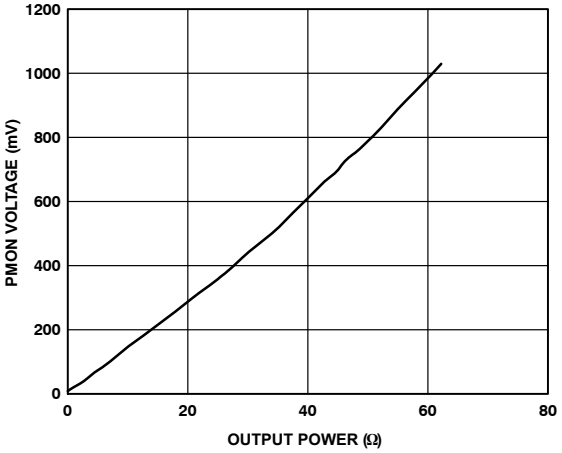



**Figure 14. IMON Voltage vs. Output Current**

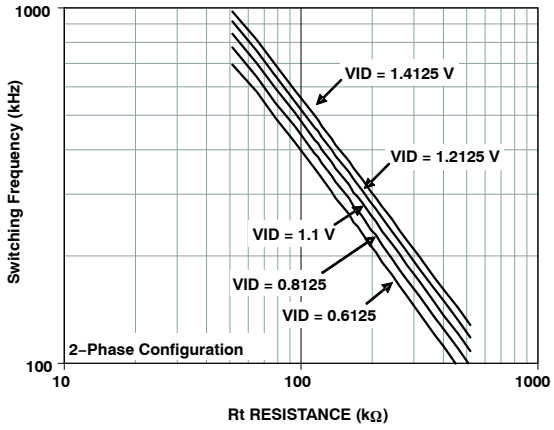



**Figure 15. Per Phase Switching Frequency vs. RT Resistance**

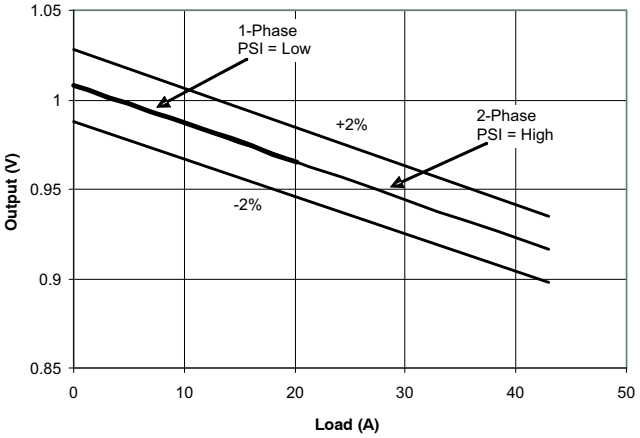



**Figure 16. Load Line Accuracy**

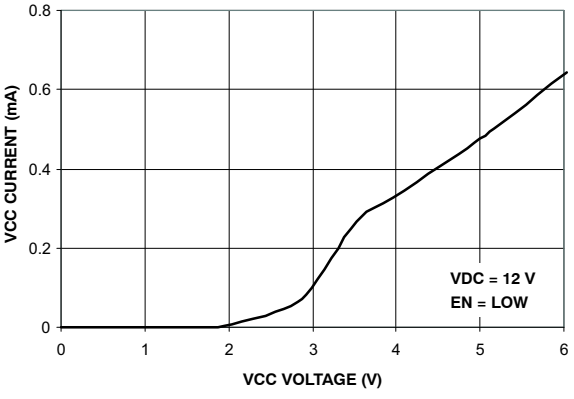



**Figure 17. VCC Current vs. VCC Voltage with Enable Low**

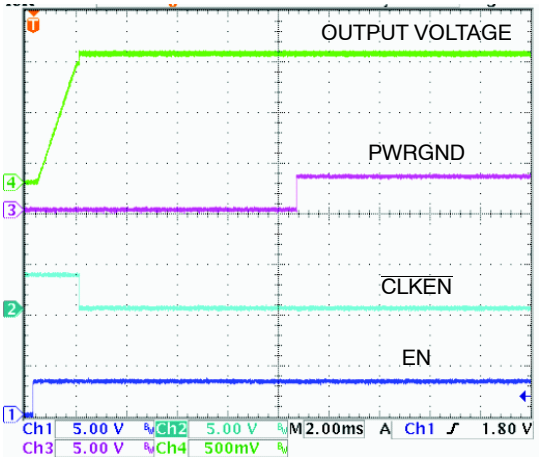



**Figure 18. Startup Waveforms**

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{VID}$ = 1.5 V, $T_A$ = 20°C to 100°C, unless otherwise noted.

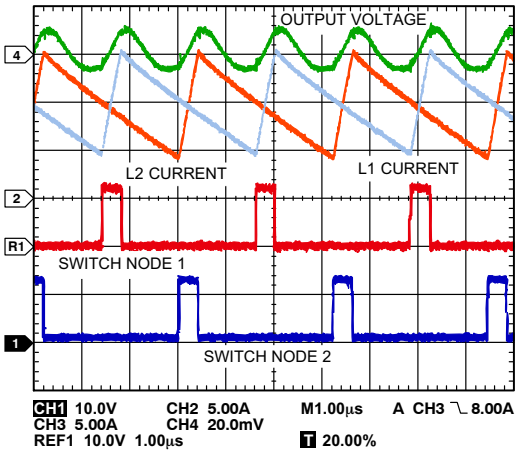



**Figure 19. Dual−Phase, Interleaved PWM Waveform, 20 A Load**

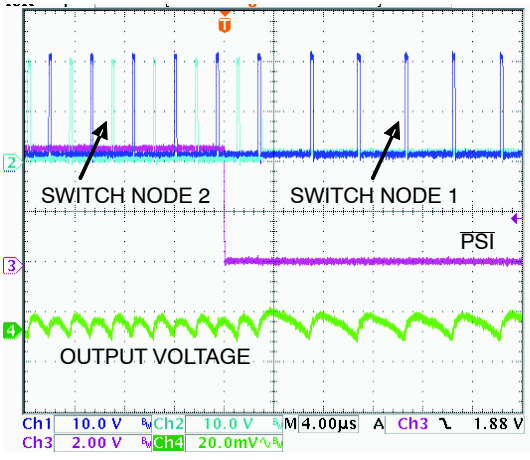



**Figure 20. $\overline{\text{PSI}}$ Transition**

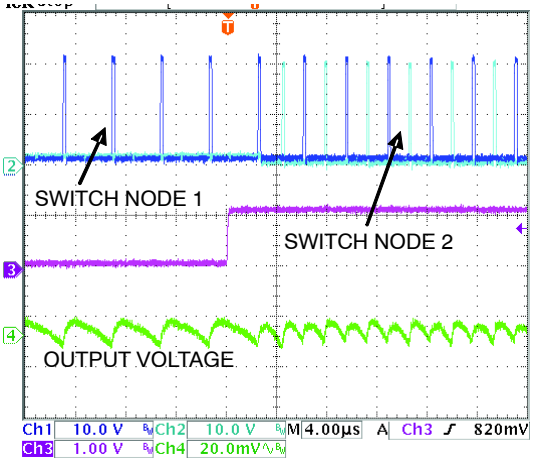



**Figure 21. $\overline{\text{PSI}}$ Transition**

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{VID}$ = 1.5 V, $T_A$ = 20°C to 100°C, unless otherwise noted.

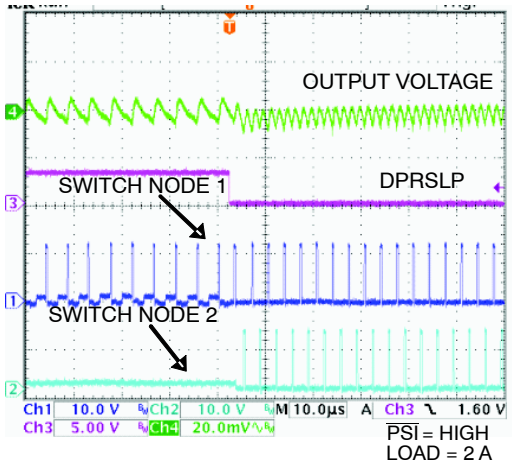



**Figure 22. DPRSLP Transition**

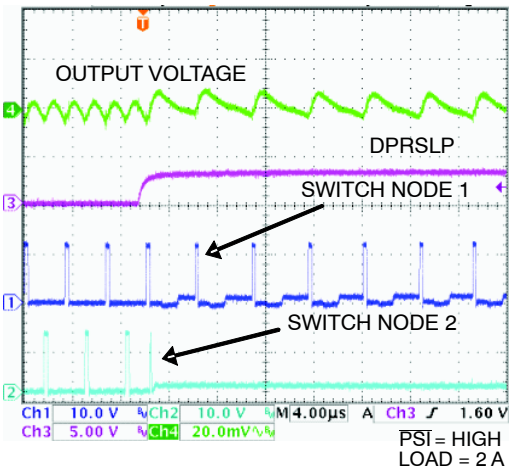



**Figure 23. DPRSLP Transition**

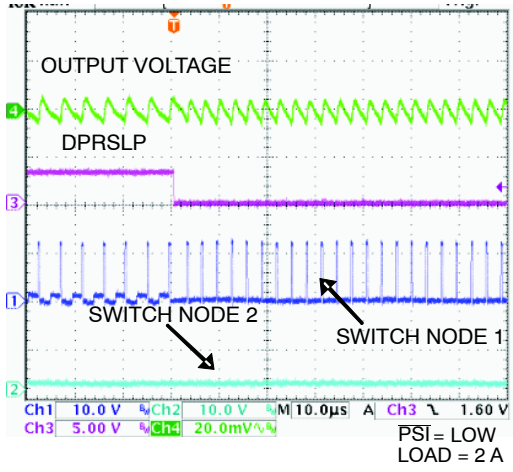



**Figure 24. DPRSLP Transition**

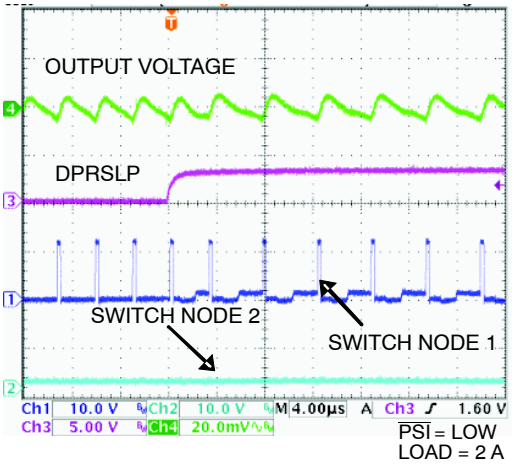



**Figure 25. DPRSLP Transition**

### Theory of Operation

The ADP3208D combines multi−mode Pulse Width Modulated (PWM) control and Ramp Pulse Modulated (RPM) control with multi−phase logic outputs for use in single− and dual−phase synchronous buck CPU core supply power converters. The internal 7−bit VID DAC conforms to the Intel IMVP−6+ specifications.

Multiphase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling high currents in a single−phase converter would put too high of a thermal stress on system components such as the inductors and MOSFETs.

The multi−mode control of the ADP3208D is a stable, high performance architecture that includes

- Current and thermal balance between phases
- High speed response at the lowest possible switching frequency and minimal count of output decoupling capacitors
- Minimized thermal switching losses due to lower frequency operation
- High accuracy load line regulation
- High current output by supporting 2−phase operation
- Reduced output ripple due to multiphase ripple cancellation
- High power conversion efficiency with heavy and light loads
- Increased immunity from noise introduced by PC board layout constraints
- Ease of use due to independent component selection
- Flexibility in design by allowing optimization for either low cost or high performance

### Number of Phases

The number of operational phases can be set by the user. Tying the SP pin to the VCC pin forces the chip into single−phase operation. Otherwise, dual−phase operation is automatically selected, and the chip switches between single− and dual−phase modes as the load changes to optimize power conversion efficiency.

In dual−phase configuration, SP is low and the timing relationship between the two phases is determined by internal circuitry that monitors the PWM outputs. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one output can be active at a time, permitting overlapping phases.

### Operation Modes

The number of phases can be static (see the Number of Phases section) or dynamically controlled by system signals to optimize the power conversion efficiency with heavy and light loads.

If SP is set low (user−selected dual−phase mode) during a VID transient or with a heavy load condition (indicated by DPRSLP being low and $\overline{\text{PSI}}$ being high), the ADP3208D runs in 2−phase, interleaved PWM mode to achieve minimal $V_{CORE}$ output voltage ripple and the best transient performance possible. If the load becomes light (indicated by $\overline{\text{PSI}}$ being low or DPRSLP being high), ADP3208D switches to single−phase mode to maximize the power conversion efficiency.

In addition to changing the number of phases, the ADP3208D is also capable of dynamically changing the control method. In dual−phase operation, the ADP3208D runs in PWM mode, where the switching frequency is controlled by the master clock. In single−phase operation (commanded by the $\overline{\text{PSI}}$ low state), the ADP3208D runs in RPM mode, where the switching frequency is controlled by the ripple voltage appearing on the COMP pin. In RPM mode, the DRVH1 pin is driven high each time the COMP pin voltage rises to a voltage limit set by the VID voltage and an external resistor connected from the RPM to GND. If the device is in single−phase mode and the system signal DPRSLP is asserted high during the deeper sleep mode of CPU operation, the ADP3208D continues running in RPM mode but offers the option of turning off the low−side (synchronous rectifier) MOSFET when the inductor current drops to 0. Turning off the low−side MOSFETs at the zero current crossing prevents reversed inductor current build up and breaks synchronous operation of high− and low−side switches. Due to the asynchronous operation, the switching frequency becomes slower as the load current decreases, resulting in good power conversion efficiency with very light loads.

Table 1 summarizes how the ADP3208D dynamically changes the number of active phases and transitions the operation mode based on system signals and operating conditions.

**Table 1. Phase Number and Operation Modes**

| $\overline{\text{PSI}}$ | DPRSLP | VID Transient (Note 1) | Current Limit | No. of Phases Selected by User | No. of Phases in Operation | Operation Mode (Note 2) |
|---|---|---|---|---|---|---|
| * | * | Yes | * | N [2 or 1] | N | PWM, CCM only |
| 1 | 0 | No | * | N [2 or 1] | N | PWM, CCM only |
| 0 | 0 | No | No | * | 1 | RPM, CCM only |
| 0 | 0 | No | Yes | * | 1 | PWM, CCM only |
| * | 1 | No | No | * | 1 | RPM, automatic CCM/DCM |
| * | 1 | No | Yes | * | 1 | PWM, CCM only |

* = Don't Care

1. VID transient period is the time following any VID change, including entry into and exit from deeper sleep mode. The duration of VID transient period is the same as that of PWRGD masking time.
2. CCM stands for continuous current mode, and DCM stands for discontinuous current mode.

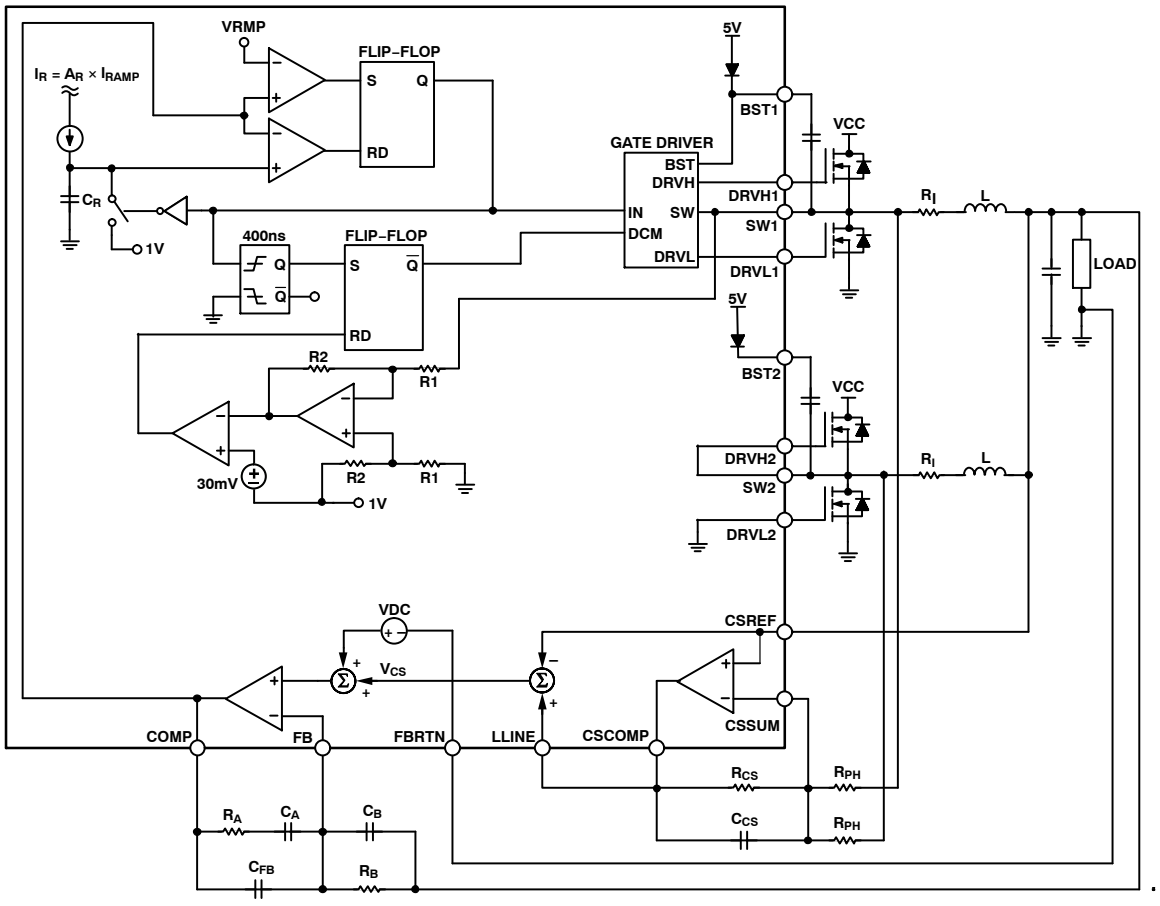



**Figure 26. Single−Phase RPM Mode Operation**

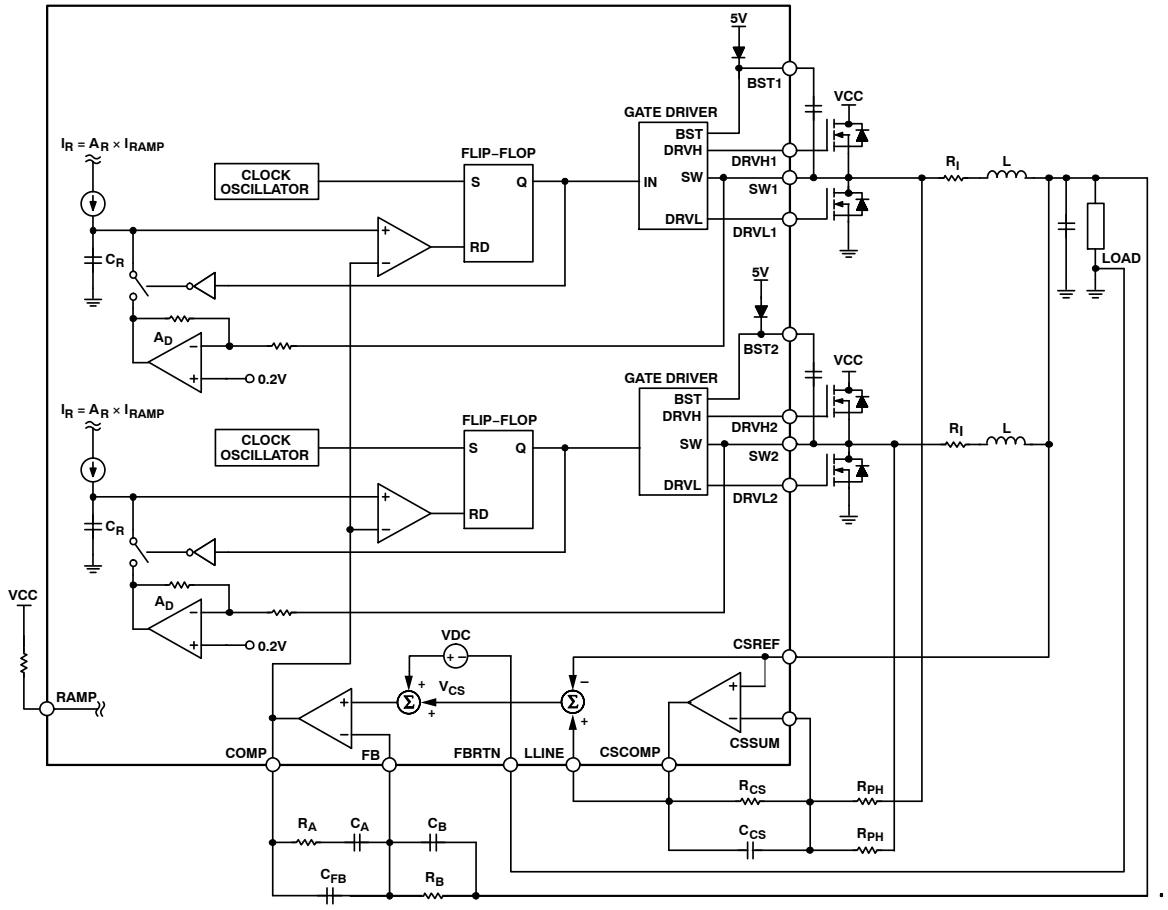



**Figure 27. Dual−Phase PWM Mode Operation**

## Setting Switch Frequency

### Master Clock Frequency in PWM Mode

When the ADP3208D runs in PWM, an external resistor connected from the RT pin to GND sets the clock frequency. The frequency is constant at a given VID code but varies with the VID voltage: the lower the VID voltage, the lower the clock frequency. The variation of clock frequency with VID voltage maintains constant $V_{CORE}$ ripple and improves power conversion efficiency at lower VID voltages. Figure 15 shows the relationship between clock frequency and VID voltage, parametrized by RT resistance.

To determine the switching frequency per phase, divide the clock by the number of phases in use.

### Switching Frequency in RPM Mode — Single−Phase Operation

In single−phase RPM mode, the switching frequency is controlled by the ripple voltage on the COMP pin, rather than by the master clock. Each time the COMP pin voltage exceeds the RPM pin voltage threshold level determined by the VID voltage and the external resistor connected from RPM to GND, an internal ramp signal is started and DRVH1 is driven high. The slew rate of the internal ramp is programmed by the current entering the RAMP pin. One−third of the RAMP current charges an internal ramp capacitor (5 pF typical) and creates a ramp. When the internal ramp signal intercepts the COMP voltage, the DRVH1 pin is reset low.

In continuous current mode, the switching frequency of RPM operation is almost constant. While in discontinuous current conduction mode, the switching frequency is reduced as a function of the load current.

### Differential Sensing of Output Voltage

The ADP3208D combines differential sensing with a high accuracy VID DAC, referenced by a precision band gap source and a low offset error amplifier, to meet the rigorous accuracy requirement of the Intel IMVP−6+ specification. In steady−state mode, the combination of the VID DAC and error amplifier maintain the output voltage for a worst−case scenario within ±8 mV of the full operating output voltage and temperature range.

The CPU core output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the positive regulation point; the VCC remote sensing pin of the microprocessor. FBRTN should be connected directly to the negative remote sensing point; the $V_{SS}$ sensing point of the CPU. The internal VID DAC and precision voltage reference are referenced to FBRTN and have a maximum current of 200 μA for guaranteed accurate remote sensing.

### Output Current Sensing

The ADP3208D includes a dedicated Current Sense Amplifier (CSA) to monitor the total output current of the converter for proper voltage positioning vs. load current and for over current detection. Sensing the current delivered to the load is an inherently more accurate method than detecting peak current or sampling the current across a sense element, such as the low−side MOSFET. The CSA can be configured several ways, depending on system optimization objectives, and the current information can be obtained by:

- Output inductor ESR sensing without the use of a thermistor for the lowest cost
- Output inductor ESR sensing with the use of a thermistor that tracks inductor temperature to improve accuracy
- Discrete resistor sensing for the highest accuracy

At the positive input of the CSA, the CSREF pin is connected to the output voltage. At the negative input (that is, the CSSUM pin of the CSA), signals from the sensing element (in the case of inductor DCR sensing, signals from the switch node side of the output inductors) are summed together by series summing resistors. The feedback resistor between the CSCOMP and CSSUM pins sets the gain of the CSA, and a filter capacitor is placed in parallel with this resistor. The current information is then given as the voltage difference between the CSCOMP and CSREF pins. This signal is used internally as a differential input for the current limit comparator.

An additional resistor divider connected between the CSCOMP and CSREF pins with the midpoint connected to the LLINE pin can be used to set the load line required by the microprocessor specification. The current information to set the load line is then given as the voltage difference between the LLINE and CSREF pins. This configuration allows the load line slope to be set independent from the current limit threshold. If the current limit threshold and load line do not have to be set independently, the resistor divider between the CSCOMP and CSREF pins can be omitted and the CSCOMP pin can be connected directly to LLINE. To disable voltage positioning entirely (that is, to set no load line), LLINE should be tied to CSREF.

To provide the best accuracy for current sensing, the CSA has a low offset input voltage and the sensing gain is set by an external resistor ratio.

### Active Impedance Control Mode

To control the dynamic output voltage droop as a function of the output current, the signal that is proportional to the total output current, converted from the voltage difference between LLINE and CSREF, can be scaled to be equal to the required droop voltage. This droop voltage is calculated by multiplying the droop impedance of the regulator by the output current. This value is used as the control voltage of the PWM regulator. The droop voltage is subtracted from the DAC reference output voltage, and the resulting voltage is used as the voltage positioning setpoint. The arrangement results in an enhanced feed−forward response.

### Current Control Mode and Thermal Balance

The ADP3208D has individual inputs for monitoring the current of each phase. The phase current information is combined with an internal ramp to create a current−balancing feedback system that is optimized for initial current accuracy and dynamic thermal balance. The current balance information is independent from the total inductor current information used for voltage positioning described in the Active Impedance Control Mode section.

The magnitude of the internal ramp can be set so that the transient response of the system is optimal. The ADP3208D monitors the supply voltage to achieve feed forward control whenever the supply voltage changes. A resistor connected from the power input voltage rail to the RAMP pin determines the slope of the internal PWM ramp. More detail about programming the ramp is provided in the Application Information section.

The ADP3208D should not require external thermal balance circuitry if a good layout is used. However, if mismatch is desired due to uneven cooling in phase, external resistors can be added to individually control phase currents as long as the phase currents are mismatched by less than 30%. If unwanted mismatch exceeds 30%, a new layout that improves phase symmetry should be considered.

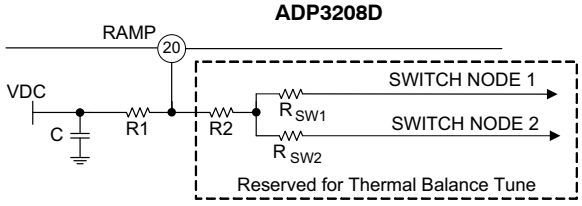



**Figure 28. Optional Current Balance Resistors**

In 2−phase operation, alternate cycles of the internal ramp control the duty cycle of the separate phases. Figure 28 shows the addition of two resistors from each switch node to the RAMP pin; this modifies the ramp−charging current individually for each phase. During Phase 1, SW Node 1 is high (practically at the input voltage potential) and SW Node 2 is low (practically at the ground potential). As a consequence, the RAMP pin, through the R2 resistor, sees the tap point of a divider connected to the input voltage, where $R_{SW1}$ is the upper element and $R_{SW2}$ is the lower element of the divider. During Phase 2, the voltages on SW Node 1 and SW Node 2 switch and the resistors swap functions. Tuning $R_{SW1}$ and $R_{SW2}$ allows the current to be optimally set for each phase. To increase the current for a given phase, decrease $R_{SW}$ for that phase.

### Voltage Control Mode

A high−gain bandwidth error amplifier is used for the voltage mode control loop. The noninverting input voltage

is set via the 7−bit VID DAC. The VID codes are listed in the VID Code table. The noninverting input voltage is offset by the droop voltage as a function of current, commonly known as active voltage positioning. The output of the error amplifier is the COMP pin, which sets the termination voltage of the internal PWM ramps.

At the negative input, the FB pin is tied to the output sense location using $R_B$, a resistor for sensing and controlling the output voltage at the remote sensing point. The main loop compensation is incorporated in the feedback network connected between the FB and COMP pins.

### Power−Good Monitoring

The power−good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open−drain output that can be pulled up through an external resistor to a voltage rail, not necessarily the same VCC voltage rail that is running the controller. A logic high level indicates that the output voltage is within the voltage limits defined by a range around the VID voltage setting. PWRGD goes low when the output voltage is outside of this range.

Following the IMVP−6+ specification, the PWRGD range is defined to be 300 mV less than and 200 mV greater than the actual VID DAC output voltage. For any DAC voltage less than 300 mV, only the upper limit of the PWRGD range is monitored. To prevent a false alarm, the power−good circuit is masked during various system transitions, including a VID change and entrance into or exit out of deeper sleep. The duration of the PWRGD mask is set to approximately 130 μs by an internal timer. If the voltage drop is greater than 200 mV during deeper sleep entry or slow deeper sleep exit, the duration of PWRGD masking is extended by the internal logic circuit.

### Powerup Sequence and Soft−Start

The power−on ramp−up time of the output voltage is set internally. The powerup sequence, including the soft−start is illustrated in Figure 29.

After EN is asserted high, the soft−start sequence starts. The core voltage ramps up linearly to the boot voltage. The ADP3208D regulates at the boot voltage for 100 μs. After the boot time is completed, $\overline{\text{CLKEN}}$ is asserted low. After $\overline{\text{CLKEN}}$ is asserted low for 9ms, PWRGD is asserted high.

In VCC UVLO or in shutdown, a small MOSFET turns on connecting the CSREF to GND. The MOSFET on the CSREF pin has a resistance of approximately 100Ω. When VCC ramps above the upper UVLO threshold and EN is asserted high, the ADP3208D enables internal bias and starts a reset cycle that lasts about 50 μs to 60 μs. Next, when initial reset is over, the chip detects the number of phases set by the user, and gives a go signal to start soft−start. The ADP3208D reads the VID codes provided by the CPU on VID0 to VID6 input pins after $\overline{\text{CLKEN}}$ is asserted low. The PWRGD signal is asserted after a $t_{CPU_PWRGD}$ delay of about 9 ms, as specified by IMVP−6+. The power−good delay is programmed internally.

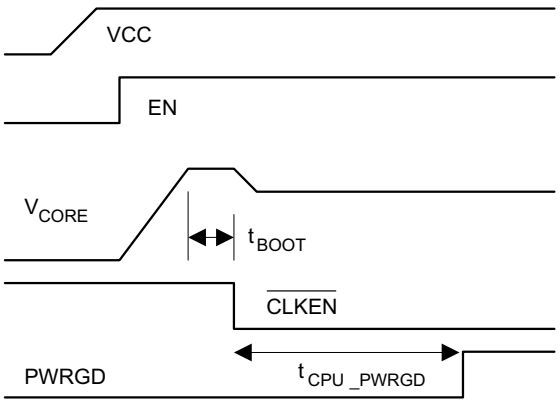



**Figure 29. Powerup Sequence of ADP3208D**

If EN is taken low or VCC drops below the VCC UVLO threshold, both the SS capacitor and the PGDELAY capacitor are reset to ground to prepare the chip for a subsequent soft−start cycle.

### Soft Transient

When a VID input changes, the ADP3208D detects the change but ignores new code for a minimum of 400 ns. This delay is required to prevent the device from reacting to digital signal skew while the 7−bit VID input code is in transition. Additionally, the VID change triggers a PWRGD masking timer to prevent a PWRGD failure. Each VID change resets and retriggers the internal PWRGD masking timer.

The ADP3208D provides a soft transient function to reduce inrush current during VID transitions. Reducing the inrush current helps decrease the acoustic noise generated by the MLCC input capacitors and inductors.

The soft transient feature is implemented internally. When a new VID code is detected, the ADP3208D steps sequentially through each VID voltage to the final VID voltage. There is a PWRGD masking time of 100μs after the last VID code is changed internally. Table 2 lists the soft transient slew rate.

**Table 2. Soft Transient Slew Rate**

| VID Transient | DPRSLP | Slew Rate |
|---|---|---|
| Entrance to Deeper Sleep | HIGH | −3.125mV/μs |
| Fast Exit from Deeper Sleep | LOW | +12.5mV/μs |
| Slow Exit from Deeper Sleep | HIGH | +3.125mV/μs |
| Transient from $V_{BOOT}$ to VID | DNC[1] | ±3.125mV/μs |

1. DNC = Do Not Care.

### Current Limit

The ADP3208D compares the differential output of a current sense amplifier to a programmable current limit setpoint to provide current limiting function. The current limit set point is set with a resistor connected from $I_{LIM}$ pin to CSCOMP pin. This is the $R_{lim}$ resistor. During normal

operation, the voltage on the $I_{LIM}$ pin is equal to the CSREF pin. The voltage across $R_{LIM}$ is equal to the voltage across the CSA (from CSREF pin to CSCOMP pin). This voltage is proportional to output current. The current through $R_{LIM}$ is proportional to the output inductor current. The current through $R_{LIM}$ is compared with an internal reference current. When the $R_{LIM}$ current goes above the internal reference current, the ADP3208D goes into current limit. The current limit circuit is shown in Figure 30.

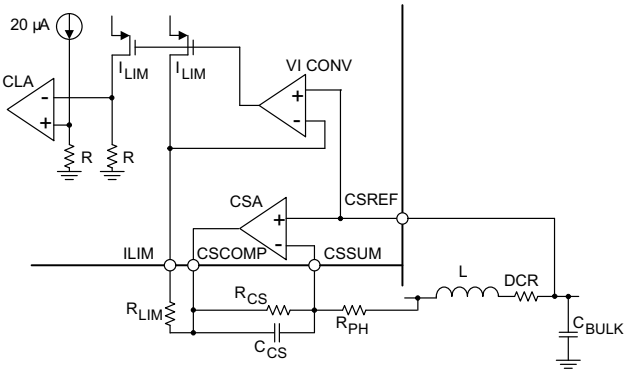



**Figure 30. Current Limit Circuit**

During startup when the output voltage is below 200 mV, a secondary current limit is activated. This is necessary because the voltage swing on CSCOMP cannot extend below ground. The secondary current limit circuit clamps the internal COMP voltage and sets the internal compensation ramp termination voltage at 1.5 V level. The clamp actually limits voltage drop across the low side MOSFETs through the current balance circuitry.

An inherent per phase current limit protects individual phases in case one or more phases stop functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage.

After 9 ms in current limit, the ADP3208D will latchoff. The latchoff can be reset by removing and reapplying VCC, or by recycling the EN pin low and high for a short time.

The latchoff can be reset by removing and reapplying VCC, or by recycling the EN pin low and high for a short time.

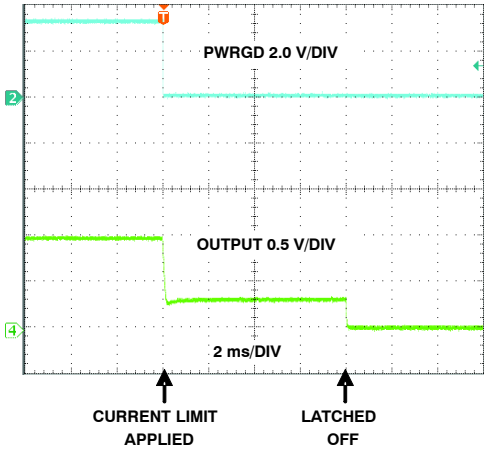



**Figure 31. Current Overload**

### Changing VID OTF

The ADP3208D is designed to track dynamically changing VID code. As a consequence, the CPU VCC voltage can change without the need to reset the controller or the CPU. This concept is commonly referred to as VID OTF transient. A VID OTF can occur with either light or heavy load conditions. The processor alerts the controller that a VID change is occurring by changing the VID inputs in LSB incremental steps from the start code to the finish code. The change can be either upwards or downwards steps.

When a VID input changes, the ADP3208D detects the change but ignores new code for a minimum of 400 ns. This delay is required to prevent the device from reacting to digital signal skew while the 7−bit VID input code is in transition. Additionally, the VID change triggers a PWRGD masking timer to prevent a PWRGD failure. Each VID change resets and retriggers the internal PWRGD masking timer.

As listed in Table 3, during a VID transient, the ADP3208D forces PWM mode regardless of the state of the system input signals. For example, this means that if the chip is configured as a dual−phase controller but is running in single−phase mode due to a light load condition, a current overload event causes the chip to switch to dual−phase mode to share the excessive load until the delayed current limit latchoff cycle terminates.

In user−set single−phase mode, the ADP3208D usually runs in RPM mode. When a VID transition occurs, however, the ADP3208D switches to dual−phase PWM mode.

### Light Load RPM DCM Operation

In single−phase normal mode, DPRSLP is pulled low and the APD3208 operates in Continuous Conduction Mode (CCM) over the entire load range. The upper and lower MOSFETs run synchronously and in complementary phase. See Figure 32 for the typical waveforms of the ADP3208D running in CCM with a 7 A load current.

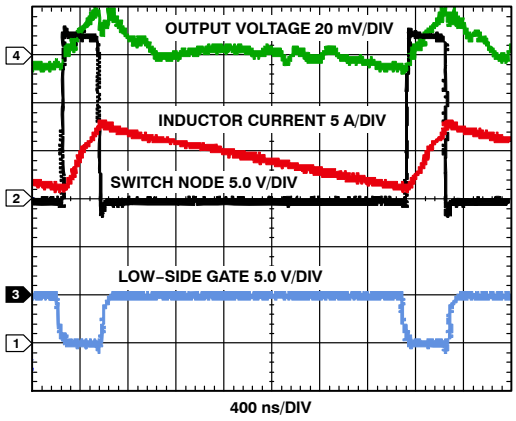



**Figure 32. Single−Phase Waveforms in CCM**

If DPRSLP is pulled high, the ADP3208D operates in RPM mode. If the load condition is light, the chip enters Discontinuous Conduction Mode (DCM). Figure 33 shows a typical single−phase buck with one upper FET, one lower FET, an output inductor, an output capacitor, and a load resistor. Figure 34 shows the path of the inductor current with the upper FET on and the lower FET off. In Figure 35 the high−side FET is off and the low−side FET is on. In CCM, if one FET is on, its complementary FET must be off; however, in DCM, both high− and low−side FETs are off and no current flows into the inductor (see Figure 36). Figure 37 shows the inductor current and switch node voltage in DCM.

In DCM with a light load, the ADP3208D monitors the switch node voltage to determine when to turn off the low−side FET. Figure 38 shows a typical waveform in DCM with a 1 A load current. Between $t_1$ and $t_2$, the inductor current ramps down. The current flows through the source drain of the low−side FET and creates a voltage drop across the FET with a slightly negative switch node. As the inductor current ramps down to 0 A, the switch voltage approaches 0 V, as seen just before $t_2$. When the switch voltage is approximately −6 mV, the low−side FET is turned off.

Figure 37 shows a small, dampened ringing at $t_2$. This is caused by the LC created from capacitance on the switch node, including the $C_{DS}$ of the FETs and the output inductor. This ringing is normal.

The ADP3208D automatically goes into DCM with a light load. Figure 38 shows the typical DCM waveform of the ADP3208D. As the load increases, the ADP3208D enters into CCM. In DCM, frequency decreases with load current. Figure 39 shows switching frequency vs. load current for a typical design. In DCM, switching frequency is a function of the inductor, load current, input voltage, and output voltage.

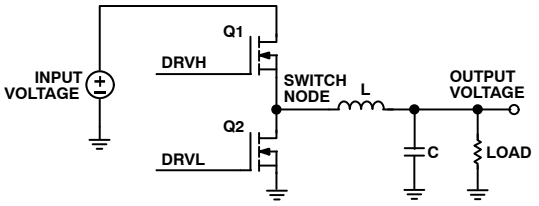



**Figure 33. Buck Topology**

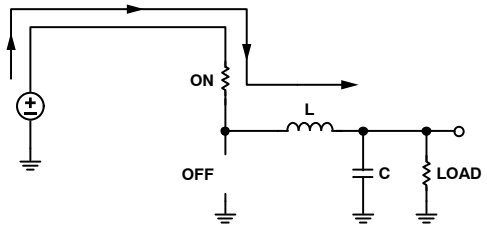



**Figure 34. Buck Topology Inductor Current During $t_0$ and $t_1$**

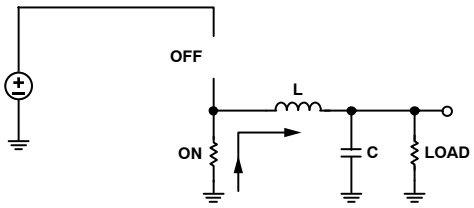



**Figure 35. Buck Topology Inductor Current During $t_1$ and $t_2$**

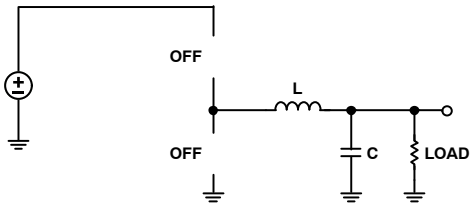



**Figure 36. Buck Topology Inductor Current During $t_2$ and $t_3$**

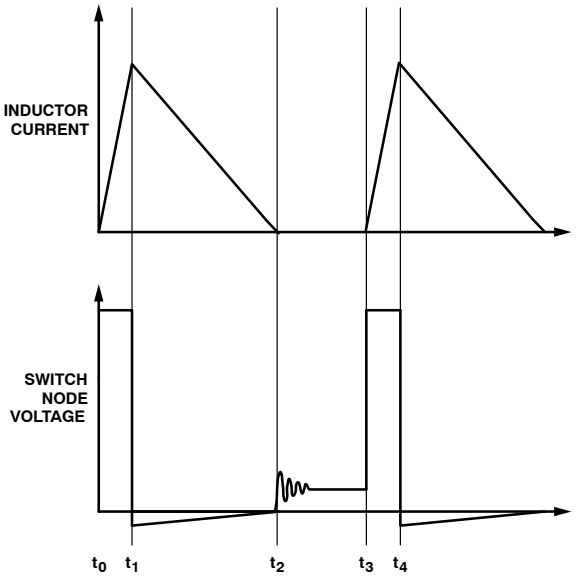



**Figure 37. Inductor Current and Switch Node in DCM**

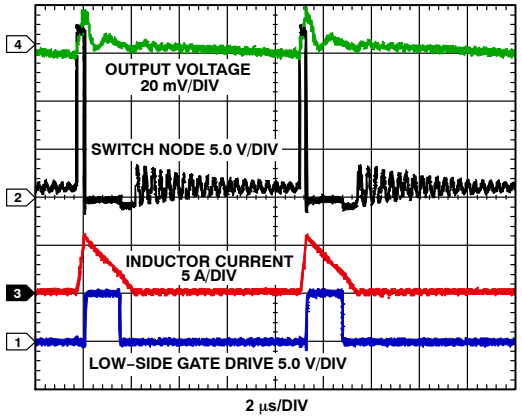



**Figure 38. Single−Phase Waveforms in DCM with 1 A Load Current**

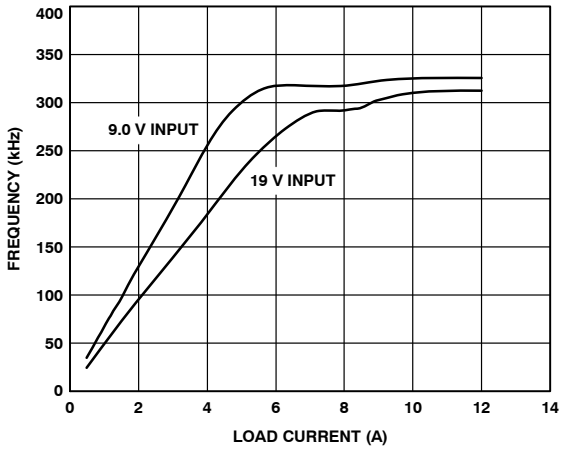



**Figure 39. Single−Phase CCM/DCM Frequency vs. Load Current**

### Output Crowbar

To prevent the CPU and other external components from damage due to overvoltage, the ADP3208D turns off the DRVH1 and DRVH2 outputs and turns on the DRVL1 and DRVL2 outputs when the output voltage exceeds the OVP threshold (1.7 V typical).

Turning on the low−side MOSFETs forces the output capacitor to discharge and the current to reverse due to current build up in the inductors. If the output overvoltage is due to a drain−source short of the high−side MOSFET, turning on the low−side MOSFET results in a crowbar across the input voltage rail. The crowbar action blows the fuse of the input rail, breaking the circuit and thus protecting the microprocessor from destruction.

When the OVP feature is triggered, the ADP3208D is latched off. The latchoff function can be reset by removing and reapplying VCC to the ADP3208D or by briefly pulling the EN pin low.

Pulling TTSNS to less than 1.0 V disables the overvoltage protection function. In this configuration, VRTT should be tied to ground.

### Reverse Voltage Protection

Very large reverse current in inductors can cause negative $V_{CORE}$ voltage, which is harmful to the CPU and other output components. The ADP3208D provides a reverse voltage protection (RVP) function without additional system cost. The $V_{CORE}$ voltage is monitored through the CSREF pin. When the CSREF pin voltage drops to less than −300 mV, the ADP3208D triggers the RVP function by disabling all PWM outputs and driving DRVL1 and DRVL2 low, thus turning off all MOSFETs. The reverse inductor currents can be quickly reset to 0 by discharging the built−up energy in the inductor into the input dc voltage source via the forward−biased body diode of the high−side MOSFETs. The RVP function is terminated when the CSREF pin voltage returns to greater than −100 mV.

Sometimes the crowbar feature inadvertently causes output reverse voltage because turning on the low−side MOSFETs results in a very large reverse inductor current. To prevent damage to the CPU caused from negative voltage, the ADP3208D maintains its RVP monitoring function even after OVP latchoff. During OVP latchoff, if the CSREF pin voltage drops to less than −300 mV, the low−side MOSFETs is turned off. DRVL outputs are allowed to turn back on when the CSREF voltage recovers to greater than −100 mV.

Figure 40 shows a typical OVP test. FB pin is shorted to ground causing the control to command a large duty cycle. The output voltage climbs up. When the output voltage is climbs 200 mV above the DAC voltage, the PWRGD signal de−asserts. When the output voltage climbs to 1.7V, OVP is enabled. In OVP, the phase 1 and phase 2 low side drive turns on the low side power MOSFETs. The low side MOSFETs pull the output voltage low through the power inductor. When the output voltage falls below −300 mV, Reverse Voltage Protection is enabled. In Reverse Voltage Protection, all power MOSFETs are turned off. This protects the CPU from seeing a large negative voltage.

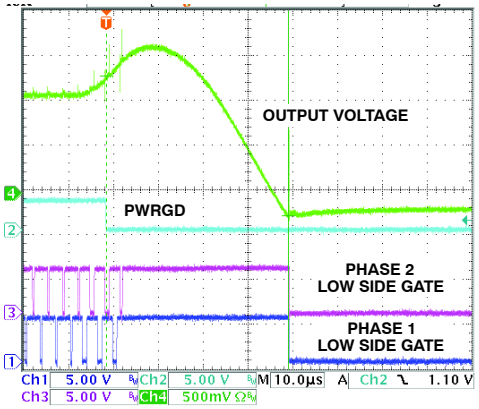



**Figure 40. Overvoltage Protection and Reverse Voltage Protection**

### Output Enable and UVLO

For the ADP3208D to begin switching the VCC supply voltage to the controller must be greater than the $V_{CCO}$ threshold and the EN pin must be driven high. If the VCC voltage is less than the $V_{CCUVLO}$ threshold or the EN pin is a logic low, the ADP3208D shuts off. In shutdown mode, the controller holds the PWM outputs low, shorts the capacitors of the SS and PGDELAY pins to ground, and drives the DRVH and DRVL outputs low.

The user must adhere to proper power supply sequencing during startup and shutdown of the ADP3208D. All input pins must be at ground prior to removing or applying VCC, and all output pins should be left in high impedance state while VCC is off.

### Thermal Throttling Control

The ADP3208D includes a thermal monitoring circuit to detect whether the temperature of the VR has exceeded a user−defined thermal throttling threshold. The thermal monitoring circuit requires an external resistor divider connected between the VCC pin and GND. The divider consists of an NTC thermistor and a resistor. To generate a

voltage that is proportional to temperature, the midpoint of the divider is connected to the TTSNS pin. An internal comparator circuit compares the TTSNS voltage to half the VCC threshold and outputs a logic level signal at the VRTT output when the temperature trips the user−set alarm threshold. The VRTT output is designed to drive an external transistor that in turn provides the high current, open−drain VRTT signal required by the IMVP−6+ specification. The internal VRTT comparator has a hysteresis of approximately 100 mV to prevent high frequency oscillation of VRTT when the temperature approaches the set alarm point.

### Current Monitor Function

The ADP3208D has an output current monitor. The IMON pin sources a current proportional to the inductor current. A resistor from IMON pin to FBRTN sets the gain. A 0.1 μF is added in parallel with $R_{MON}$ to filter the inductor ripple. The IMON pin is clamped to prevent it from going above 1.15V

**Table 3. VID Code Table**

| VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Output (V) |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1.5000 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1.4875 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1.4750 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1.4625 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1.4500 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1.4375 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1.4250 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1.4125 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1.4000 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1.3875 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1.3750 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1.3625 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1.3500 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1.3375 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1.3250 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1.3125 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1.3000 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1.2875 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1.2750 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1.2625 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1.2500 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1.2375 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1.2250 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1.2125 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1.2000 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1.1875 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1.1750 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1.1625 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1.1500 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1.1375 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1.1250 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1.1125 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1.1000 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1.0875 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1.0750 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1.0625 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1.0500 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1.0375 |

**Table 3. VID Code Table**

| VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Output (V) |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1.0250 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1.0125 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1.0000 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0.9875 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0.9750 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0.9625 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0.9500 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0.9375 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0.9250 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0.9125 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0.9000 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0.8875 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0.8750 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0.8625 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0.8500 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0.8375 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0.8250 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0.8125 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0.8000 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0.7875 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0.7750 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0.7625 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0.7500 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0.7375 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0.7250 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0.7125 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0.7000 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0.6875 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0.6750 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0.6625 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0.6500 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0.6375 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0.6250 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0.6125 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0.6000 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0.5875 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0.5750 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0.5625 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0.5500 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0.5375 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0.5250 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0.5125 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0.5000 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0.4875 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0.4750 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0.4625 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0.4500 |

**Table 3. VID Code Table**

| VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Output (V) |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0.4375 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0.4250 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0.4125 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0.4000 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0.3875 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0.3750 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0.3625 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0.3500 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0.3375 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0.3250 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0.3125 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0.3000 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0.2875 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0.2750 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0.2625 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0.2500 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0.2375 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0.2250 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0.2125 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0.2000 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0.1875 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0.1750 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0.1625 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0.1500 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0.1375 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0.1250 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0.1125 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0.1000 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0.0875 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0.0750 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0.0625 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0.0500 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0.0375 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0.0250 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0.0125 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0.0000 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0.0000 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0.0000 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0.0000 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0.0000 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0.0000 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0.0000 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.0000 |

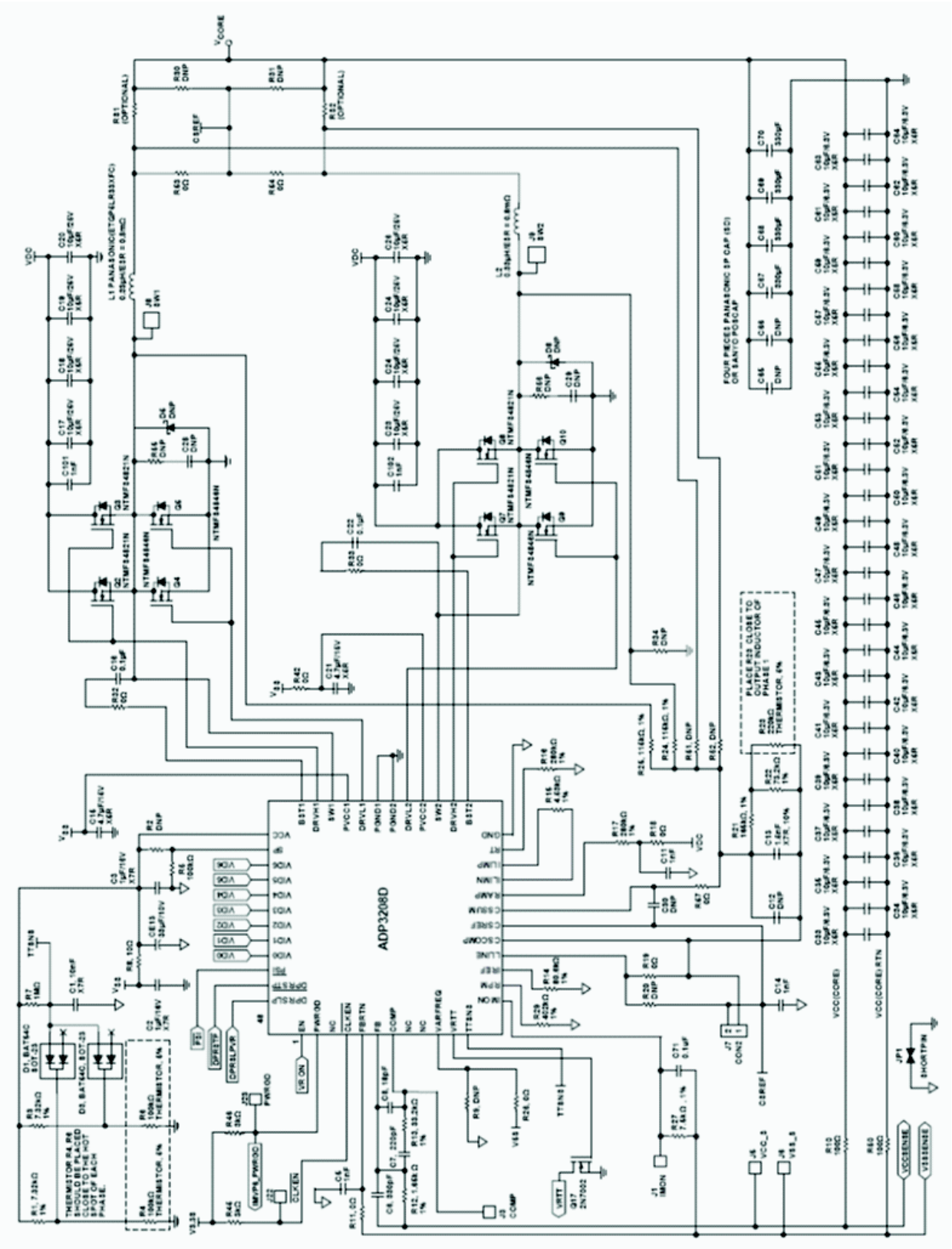



Figure 41. Typical 2−Phase Application Circuit

### Application Information

The design parameters for a typical IMVP−6+ compliant CPU core VR application are as follows:

- Maximum input voltage ($V_{INMAX}$) = 19 V
- Minimum input voltage ($V_{INMIN}$) = 8.0 V
- Output voltage by VID setting ($V_{VID}$) = 1.4375 V
- Maximum output current ($I_O$) = 40 A
- Droop resistance ($R_O$) = 2.1 mΩ
- Nominal output voltage at 40 A load ($V_{OFL}$) = 1.3535 V
- Static output voltage drop from no load to full load ($\Delta V$) = $V_{ONL} - V_{OFL}$ = 1.4375 V − 1.3535 V = 84 mV
- Maximum output current step ($\Delta I_O$) = 27.9 A
- Number of phases (n) = 2
- Switching frequency per phase ($f_{SW}$) = 300 kHz
- Duty cycle at maximum input voltage ($D_{MAX}$) = 0.18 V
- Duty cycle at minimum input voltage ($D_{MIN}$) = 0.076 V

### Setting the Clock Frequency for PWM

In PWM operation, the ADP3208D uses a fixed−frequency control architecture. The frequency is set by an external timing resistor (RT). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to the switching losses and the sizes of the inductors and input and output capacitors. For a dual−phase design, a clock frequency of 600 kHz sets the switching frequency to 300 kHz per phase. This selection represents the trade−off between the switching losses and the minimum sizes of the output filter components. To achieve a 600 kHz oscillator frequency at a VID voltage of 1.2 V, RT must be 187 kΩ. Alternatively, the value for RT can be calculated by using the following equation:

$$R_T = \frac{V_{VID} + 1.0\ V}{2 \times n \times f_{SW} \times 9\ pF} - 16\ k\Omega \qquad \text{(eq. 1)}$$

where:
9 pF and 16 kΩ are internal IC component values.
$V_{VID}$ is the VID voltage in volts.
n is the number of phases.
$f_{SW}$ is the switching frequency in hertz for each phase.

For good initial accuracy and frequency stability, it is recommended to use a 1% resistor.

When VARFREQ pin is connected to ground, the switching frequency does not change with VID. The value for RT can be calculated by using the following equation.

$$R_T = \frac{1.0\ V}{n \times f_{SW} \times 9\ pF} - 16\ k\Omega \qquad \text{(eq. 2)}$$

For good initial accuracy and frequency stability, it is recommended to use a 1% resistor.

### Setting the Switching Frequency for RPM Operation of Phase 1

During the RPM mode operation of Phase 1, the ADP3208D runs in pseudo constant frequency, given that the load current is high enough for continuous current mode. While in discontinuous current mode, the switching frequency is reduced with the load current in a linear manner. When considering power conversion efficiency in light load, lower switching frequency is usually preferred for RPM mode. However, the $V_{CORE}$ ripple specification in the IMVP−6 sets the limitation for lowest switching frequency. Therefore, depending on the inductor and output capacitors, the switching frequency in RPM mode can be equal, larger, or smaller than its counterpart in PWM mode.

A resistor from RPM to GND sets the pseudo constant frequency as following:

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{CC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{ISS} \qquad \text{(eq. 3)}$$

where:
$A_R$ is the internal ramp amplifier gain.
$C_R$ is the internal ramp capacitor value.
$R_R$ is an external resistor on the RAMPADJ pin to set the internal ramp magnitude.

Because $R_R$ = 280 kΩ, the following resistance sets up 300 kHz switching frequency in RPM operation.

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{CC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{ISS} \qquad \text{(eq. 4)}$$

### Inductor Selection

The choice of inductance determines the ripple current of the inductor. Less inductance results in more ripple current, which increases the output ripple voltage and the conduction losses in the MOSFETs. However, this allows the use of smaller−size inductors, and for a specified peak−to−peak transient deviation, it allows less total output capacitance. Conversely, a higher inductance results in lower ripple current and reduced conduction losses, but it requires larger−size inductors and more output capacitance for the same peak−to−peak transient deviation. For a multiphase converter, the practical value for peak−to−peak inductor ripple current is less than 50% of the maximum dc current of that inductor. Equation 5 shows the relationship between the inductance, oscillator frequency, and peak−to−peak ripple current. Equation 6 can be used to determine the minimum inductance based on a given output ripple voltage.

$$I_R = \frac{V_{VID} \times \left(1 - D_{MIN}\right)}{f_{SW} \times L} \qquad \text{(eq. 5)}$$

$$L \geq \frac{V_{VID} \times R_O \times (1 - (n \times D_{MIN}))}{f_{SW} \times V_{RIPPLE}} \qquad \text{(eq. 6)}$$

Solving Equation 6 for a 16 mV peak−to−peak output ripple voltage yields

$$L \geq \frac{1.4375\ V \times 2.1\ m\Omega \times (1 - (2 \times 0.076)}{300\ kHz \times 16\ mV} = 533\ nH \qquad \text{(eq. 7)}$$

If the resultant ripple voltage is less than the initially selected value, the inductor can be changed to a smaller value until the ripple value is met. This iteration allows optimal transient response and minimum output decoupling.

The smallest possible inductor should be used to minimize the number of output capacitors. Choosing a 490 nH inductor is a good choice for a starting point, and it provides

a calculated ripple current of 9.0 A. The inductor should not saturate at the peak current of 24.5 A, and it should be able to handle the sum of the power dissipation caused by the winding's average current (20 A) plus the ac core loss. In this example, 330 nH is used.

Another important factor in the inductor design is the DCR, which is used for measuring the phase currents. Too large of a DCR causes excessive power losses, whereas too small of a value leads to increased measurement error. For this example, an inductor with a DCR of 0.8 mΩ is used.

### Selecting a Standard Inductor

After the inductance and DCR are known, select a standard inductor that best meets the overall design goals. It is also important to specify the inductance and DCR tolerance to maintain the accuracy of the system. Using 20% tolerance for the inductance and 15% for the DCR at room temperature are reasonable values that most manufacturers can meet.

### Power Inductor Manufacturers

The following companies provide surface−mount power inductors optimized for high power applications upon request:

- Vishay Dale Electronics, Inc.
- Panasonic
- Sumida Corporation
- NEC Tokin Corporation

### Output Droop Resistance

The design requires that the regulator output voltage measured at the CPU pins decreases when the output current increases. The specified voltage drop corresponds to the droop resistance ($R_O$).

The output current is measured by summing the currents of the resistors monitoring the voltage across each inductor and by passing the signal through a low−pass filter. The summing is implemented by the CS amplifier that is configured with resistor $R_{PH(x)}$ (summer) and resistors $R_{CS}$ and $C_{CS}$ (filters). The output resistance of the regulator is set by the following equations:

$$R_O = \frac{R_{CS}}{R_{PH(x)}} \times R_{SENSE} \quad \text{(eq. 8)}$$

$$C_{CS} = \frac{L}{R_{SENSE} \times R_{CS}} \quad \text{(eq. 9)}$$

where $R_{SENSE}$ is the DCR of the output inductors.

Either $R_{CS}$ or $R_{PH(x)}$ can be chosen for added flexibility. Due to the current drive ability of the CSCOMP pin, the $R_{CS}$ resistance should be greater than 100 kΩ. For example, initially select $R_{CS}$ to be equal to 200 kΩ, and then use Equation 9 to solve for $C_{CS}$:

$$C_{CS} = \frac{330\ \text{nH}}{0.8\ \text{m}\Omega \times 200\ \text{k}\Omega} = 2.1\ \text{nF} \quad \text{(eq. 10)}$$

If $C_{CS}$ is not a standard capacitance, $R_{CS}$ can be tuned. For example, if the optimal $C_{CS}$ capacitance is 1.5 nF, adjust $R_{CS}$ to 280 kΩ. For best accuracy, $C_{CS}$ should be a 5% NPO capacitor. In this example, a 220 kΩ is used for $R_{CS}$ to achieve optimal results.

Next, solve for $R_{PH(x)}$ by rearranging Equation 8 as follows:

$$R_{PH(X)} \geq \frac{0.8\ \text{m}\Omega}{2.1\ \text{m}\Omega} \cdot 220\ \text{k}\Omega = 83.8\ \text{k}\Omega \quad \text{(eq. 11)}$$

The standard 1% resistor for $R_{PH(x)}$ is 86.6 kΩ.

### Inductor DCR Temperature Correction

If the DCR of the inductor is used as a sense element and copper wire is the source of the DCR, the temperature changes associated with the inductor's winding must be compensated for. Fortunately, copper has a well−known temperature coefficient (TC) of 0.39%/°C.

If $R_{CS}$ is designed to have an opposite but equal percentage of change in resistance, it cancels the temperature variation of the inductor's DCR. Due to the nonlinear nature of NTC thermistors, series resistors $R_{CS1}$ and $R_{CS2}$ (see Figure 42) are needed to linearize the NTC and produce the desired temperature coefficient tracking.

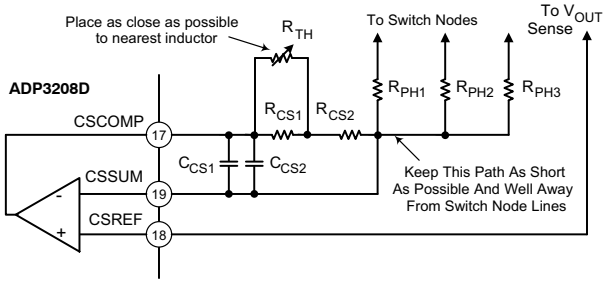



**Figure 42. Temperature−Compensation Circuit Values**

The following procedure and expressions yield values for $R_{CS1}$, $R_{CS2}$, and $R_{TH}$ (the thermistor value at 25°C) for a given $R_{CS}$ value.

1. Select an NTC to be used based on its type and value. Because the value needed is not yet determined, start with a thermistor with a value close to $R_{CS}$ and an NTC with an initial tolerance of better than 5%.
2. Find the relative resistance value of the NTC at two temperatures. The appropriate temperatures will depend on the type of NTC, but 50°C and 90°C have been shown to work well for most types of NTCs. The resistance values are called A (A is $R_{TH}(50°C)/R_{TH}(25°C)$) and B (B is $R_{TH}(90°C)/R_{TH}(25°C)$). Note that the relative value of the NTC is always 1 at 25°C.
3. Find the relative value of $R_{CS}$ required for each of the two temperatures. The relative value of $R_{CS}$ is based on the percentage of change needed, which is initially assumed to be 0.39%/°C in this example.
   The relative values are called $r_1$ ($r_1$ is $1/(1+ TC \times (T_1 - 25))$) and $r_2$ ($r_2$ is $1/(1 + TC \times (T_2 - 25))$), where TC is 0.0039,
   $T_1$ is 50°C, and $T_2$ is 90°C.

4. Compute the relative values for $r_{CS1}$, $r_{CS2}$, and $r_{TH}$ by using the following equations:

$$r_{CS2} = \frac{(A - B) \times r_1 \times r_2 - A \times (1 - B) \times r_2 + B \times (1 - A) \times r_1}{A \times (1 - B) \times r_1 - B \times (1 - A) \times r_2 - (A - B)}$$

$$r_{CS1} = \frac{(1 - A)}{\frac{1}{1 - r_{CS2}} - \frac{1}{r_1 - r_{CS2}}}$$

$$r_{TH} = \frac{1}{\frac{1}{1 - r_{CS2}} - \frac{1}{r_{CS1}}} \quad \text{(eq. 12)}$$

5. Calculate $R_{TH} = r_{TH} \times R_{CS}$, and then select a thermistor of the closest value available. In addition, compute a scaling factor k based on the ratio of the actual thermistor value used relative to the computed one:

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \quad \text{(eq. 13)}$$

6. Calculate values for $R_{CS1}$ and $R_{CS2}$ by using the following equations:

$$R_{CS1} = R_{CS} \times k \times r_{CS1}$$
$$R_{CS2} = R_{CS} \times ((1 - k) + (k \times r_{CS2})) \quad \text{(eq. 14)}$$

For example, if a thermistor value of 100 kΩ is selected in Step 1, an available 0603−size thermistor with a value close to $R_{CS}$ is the Vishay NTHS0603N04 NTC thermistor, which has resistance values of A = 0.3359 and B = 0.0771. Using the equations in Step 4, $r_{CS1}$ is 0.359, $r_{CS2}$ is 0.729, and $r_{TH}$ is 1.094. Solving for $r_{TH}$ yields 241 kΩ, so a thermistor of 220 kΩ would be a reasonable selection, making k equal to 0.913. Finally, $R_{CS1}$ and $R_{CS2}$ are found to be 72.1 kΩ and 166 kΩ. Choosing the closest 1% resistor for $R_{CS2}$ yields 165 kΩ. To correct for this approximation, 73.3 kΩ is used for $R_{CS1}$.

### $C_{OUT}$ Selection

The required output decoupling for processors and platforms is typically recommended by Intel. For systems containing both bulk and ceramic capacitors, however, the following guidelines can be a helpful supplement.

Select the number of ceramics and determine the total ceramic capacitance ($C_Z$). This is based on the number and type of capacitors used. Keep in mind that the best location to place ceramic capacitors is inside the socket; however, the physical limit is twenty 0805−size pieces inside the socket. Additional ceramic capacitors can be placed along the outer edge of the socket. A combined ceramic capacitor value of 200 μF to 300 μF is recommended and is usually composed of multiple 10 μF or 22 μF capacitors.

Ensure that the total amount of bulk capacitance ($C_X$) is within its limits. The upper limit is dependent on the VID OTF output voltage stepping (voltage step, $V_V$, in time, $t_V$, with error of $V_{ERR}$); the lower limit is based on meeting the critical capacitance for load release at a given maximum load step, $\Delta I_O$. The current version of the IMVP−6+ specification allows a maximum $V_{CORE}$ overshoot ($V_{OSMAX}$) of 10 mV more than the VID voltage for a step−off load current.

$$C_{x(MIN)} \geq \left[ \frac{L \times \Delta I_O}{n \times \left( R_O + \frac{V_{OSMAX}}{\Delta I_O} \right) \times V_{VID}} - C_z \right] \quad \text{(eq. 15)}$$

$$C_{X(MAX)} \leq \frac{L}{n \times k^2 \times R_O{}^2} \times \frac{V_v}{V_{VID}} \times \left[ \sqrt{1 + \left( t_v \frac{V_{VID}}{V_v} \times \frac{n \times k \times R_O}{L} \right)^2} - 1 \right] - C_z \quad \text{(eq. 16)}$$

where:

$$k = -1n \left( \frac{V_{ERR}}{V_V} \right) \quad \text{(eq. 17)}$$

To meet the conditions of these expressions and the transient response, the ESR of the bulk capacitor bank ($R_X$) should be less than two times the droop resistance, $R_O$. If the $C_{X(MIN)}$ is greater than $C_{X(MAX)}$, the system does not meet the VID OTF and/or the deeper sleep exit specifications and may require less inductance or more phases. In addition, the switching frequency may have to be increased to maintain the output ripple.

For example, if 30 pieces of 10 μF, 0805−size MLC capacitors ($C_Z$ = 300 μF) are used, the fastest VID voltage change is when the device exits deeper sleep, during which the $V_{CORE}$ change is 220 mV in 22 μs with a setting error of 10 mV. If k = 3.1, solving for the bulk capacitance yields:

$$C_{X(MIN)} \geq \left[ \frac{330\ nH \cdot 27.9\ A}{2 \times \left( 2.1\ m\Omega + \frac{10\ mV}{27.9\ A} \right) \times 1.4375\ V} - 300\ \mu F \right] = 1.0\ mF$$

$$C_{X(MAX)} \leq \frac{330\ nH \times 220\ mV}{2 \times 3.1^2 \times (2.1\ m\Omega)^2 \times 1.4375\ V} \left[ \sqrt{1 + \left( \frac{22\ \mu s \times 1.4375\ V \times 2 \times 3.1 \times 2.1\ m\Omega}{220\ mV \times 490\ nH} \right)^2} - 1 \right] - 300\ \mu F = 21\ mF$$

Using six 330 μF Panasonic SP capacitors with a typical ESR of 7 mΩ each yields $C_X$ = 1.98 mF and $R_X$ = 1.2 mΩ.

Ensure that the ESL of the bulk capacitors ($L_X$) is low enough to limit the high frequency ringing during a load change. This is tested using:

$$L_X \leq C_Z \times R_O{}^2 \times Q^2$$
$$L_X \leq 300\ \mu F \times (2.1\ m\Omega)^2 \times 2 = 2\ nH \quad \text{(eq. 18)}$$

where:
Q is limited to the square root of 2 to ensure a critically damped system.

$L_X$ is about 150 pH for the six SP capacitors, which is low enough to avoid ringing during a load change. If the $L_X$ of the chosen bulk capacitor bank is too large, the number of ceramic capacitors may need to be increased to prevent excessive ringing.

For this multi−mode control technique, an all ceramic capacitor design can be used if the conditions of Equations 16, 17, and 18 are satisfied.

**Power MOSFETs**

For typical 20 A per phase applications, the N−channel power MOSFETs are selected for two high−side switches and two or three low−side switches per phase. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, $Q_G$, $C_{ISS}$, $C_{RSS}$, and $R_{DS(ON)}$. Because the voltage of the gate driver is 5.0 V, logic−level threshold MOSFETs must be used.

The maximum output current, $I_O$, determines the $R_{DS(ON)}$ requirement for the low−side (synchronous) MOSFETs. In the ADP3208D, currents are balanced between phases; the current in each low−side MOSFET is the output current divided by the total number of MOSFETs ($n_{SF}$). With conduction losses being dominant, the following expression shows the total power that is dissipated in each synchronous MOSFET in terms of the ripple current per phase ($I_R$) and the average total output current ($I_O$):

$$P_{SF} = (1 - D) \times \left[ \left( \frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \times \left( \frac{n \times I_R}{n_{SF}} \right)^2 \right] \times R_{DS(SF)} \quad \text{(eq. 19)}$$

where:

D is the duty cycle and is approximately the output voltage divided by the input voltage.

$I_R$ is the inductor peak−to−peak ripple current and is approximately:

$$I_R = \frac{(1 - D) \times V_{OUT}}{L \times f_{SW}} \quad \text{(eq. 20)}$$

Knowing the maximum output current and the maximum allowed power dissipation, the user can calculate the required $R_{DS(ON)}$ for the MOSFET. For 8−lead SOIC or 8−lead SOIC−compatible MOSFETs, the junction−to−ambient (PCB) thermal impedance is 50°C/W. In the worst case, the PCB temperature is 70°C to 80°C during heavy load operation of the notebook, and a safe limit for $P_{SF}$ is about 0.8 W to 1.0 W at 120°C junction temperature. Therefore, for this example (40 A maximum), the $R_{DS(SF)}$ per MOSFET is less than 8.5 mΩ for two pieces of low−side MOSFETs. This $R_{DS(SF)}$ is also at a junction temperature of about 120°C; therefore, the $R_{DS(SF)}$ per MOSFET should be less than 6 mΩ at room temperature, or 8.5 mΩ at high temperature.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of the feedback to input must be small (less than 10% is recommended) to prevent accidentally turning on the synchronous MOSFETs when the switch node goes high.

The high−side (main) MOSFET must be able to handle two main power dissipation components: conduction losses and switching losses. Switching loss is related to the time for the main MOSFET to turn on and off and to the current and voltage that are being switched. Basing the switching speed on the rise and fall times of the gate driver impedance and MOSFET input capacitance, the following expression provides an approximate value for the switching loss per main MOSFET:

$$R_{RPM} = \frac{2 \times R_T}{V_{VID} \times 1.0\ V} \times \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} - 0.5\ k\Omega \quad \text{(eq. 21)}$$

where:

$n_{MF}$ is the total number of main MOSFETs.

$R_G$ is the total gate resistance.

$C_{ISS}$ is the input capacitance of the main MOSFET.

The most effective way to reduce switching loss is to use lower gate capacitance devices.

The conduction loss of the main MOSFET is given by the following equation:

$$R_{RPM} = \frac{2 \times 280\ k\Omega}{1.150\ V + 1.0\ V} \times \frac{0.5 \times (1 - 0.061) \times 1.150}{462\ k\Omega \times 5\ pF \times 300\ kHz} - 500\ k\Omega = 202\ k\Omega \quad \text{(eq. 22)}$$

where $R_{DS(MF)}$ is the on resistance of the MOSFET.

Typically, a user wants the highest speed (low $C_{ISS}$) device for a main MOSFET, but such a device usually has higher on resistance. Therefore, the user must select a device that meets the total power dissipation (about 0.8 W to 1.0 W for an 8−lead SOIC) when combining the switching and conduction losses.

For example, an IRF7821 device can be selected as the main MOSFET (four in total; that is, $n_{MF}$ = 4), with approximately $C_{ISS}$ = 1010 pF (max) and $R_{DS(MF)}$ = 18 mΩ (max at $T_J$ = 120°C), and an IR7832 device can be selected as the synchronous MOSFET (four in total; that is, $n_{SF}$ = 4), with $R_{DS(SF)}$ = 6.7 mΩ (max at $T_J$ = 120°C). Solving for the power dissipation per MOSFET at $I_O$ = 40 A and $I_R$ = 9.0 A yields 630 mW for each synchronous MOSFET and 590 mW for each main MOSFET. A third synchronous MOSFET is an option to further increase the conversion efficiency and reduce thermal stress.

Finally, consider the power dissipation in the driver for each phase. This is best described in terms of the $Q_G$ for the MOSFETs and is given by the following equation:

$$P_{DRV} = \left[ \frac{f_{SW}}{2 \times n} \times \left( n_{MF} \times Q_{GMF} + n_{SF} \times Q_{QSF} \right) + I_{CC} \right] \times V_{CC} \quad \text{(eq. 23)}$$

where $Q_{GMF}$ is the total gate charge for each main MOSFET, and $Q_{GSF}$ is the total gate charge for each synchronous MOSFET.

The previous equation also shows the standby dissipation ($I_{CC}$ times the VCC) of the driver.

### Ramp Resistor Selection

The ramp resistor ($R_R$) is used to set the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. Use the following expression to determine a starting value:

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \quad \text{(eq. 24)}$$

$$R_R = \frac{0.5 \times 360\ \text{nH}}{3 \times 5 \times 5.2\ \text{m}\Omega \times 5\ \text{pF}} = 462\ \text{k}\Omega$$

where:
$A_R$ is the internal ramp amplifier gain.
$A_D$ is the current balancing amplifier gain.
$R_{DS}$ is the total low−side MOSFET ON−resistance;
$C_R$ is the internal ramp capacitor value.

Another consideration in the selection of $R_R$ is the size of the internal ramp voltage (see Equation 25). For stability and noise immunity, keep the ramp size larger than 0.5 V. Taking this into consideration, the value of $R_R$ in this example is selected as 280 kΩ.

The internal ramp voltage magnitude can be calculated as follows:

$$V_R = \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \quad \text{(eq. 25)}$$

$$V_R = \frac{0.5 \times (1 - 0.061) \times 1.150\ \text{V}}{462\ \text{k}\Omega \times 5\ \text{pF} \times 280\ \text{kHz}} = 0.83\ \text{V}$$

The size of the internal ramp can be increased or decreased. If it is increased, stability and transient response improves but thermal balance degrades. Conversely, if the ramp size is decreased, thermal balance improves but stability and transient response degrade. In the denominator of Equation 24, the factor of 3 sets the minimum ramp size that produces an optimal combination of good stability, transient response, and thermal balance.

### COMP Pin Ramp

In addition to the internal ramp, there is a ramp signal on the COMP pin due to the droop voltage and output voltage ramps. This ramp amplitude adds to the internal ramp to produce the following overall ramp signal at the PWM input:

$$V_{RT} = \frac{V_R}{\left(1 - \frac{2 \times (1 - n \times D)}{n \times f_{SW} \times C_X \times R_O}\right)} \quad \text{(eq. 26)}$$

where $C_X$ is the total bulk capacitance, and $R_O$ is the droop resistance of the regulator.

For this example, the overall ramp signal is 1.85 V.

### Current Limit Setpoint

To select the current limit setpoint, the resistor value for $R_{CLIM}$ must be determined. The current limit threshold for the ADP3208D is set with $R_{CLIM}$. $R_{CLIM}$ can be found using the following equation:

$$R_{LIM} = \frac{I_{LIM} \times R_O}{60\ \mu\text{A}} \quad \text{(eq. 27)}$$

where:
$R_{LIM}$ is the current limit resistor.
$R_O$ is the output load line.
$I_{LIM}$ is the current limit set point.

When the ADP3208D is configured for 2−phase operation, the equation above is used to set the current limit. When the ADP3208D switches from 2−phase to 1−phase operation by $\overline{PSI}$ or DPRSLP signal, the current is single−phase is one half of the current limit in 2−phase.

When the ADP3208D is configured for 1−phase operation, the equation above is used to set the current limit.

### Output Current Monitor

The ADP3208D has output current monitor. The IMON pin sources a current proportional to the total inductor current. A resistor, $R_{MON}$, from IMON to FBRTN sets the gain of the output current monitor. A 0.1 μF is placed in parallel with $R_{MON}$ to filter the inductor current ripple and high frequency load transients. Since the IMON pin is connected directly to the CPU, it is clamped to prevent it from going above 1.15V.

The IMON pin current is equal to the $R_{LIM}$ times a fixed gain of 10. $R_{MON}$ can be found using the following equation:

$$R_{MON} = \frac{1.15\ \text{V} \times R_{LIM}}{10 \times R_O \times I_{FS}} \quad \text{(eq. 28)}$$

where:
$R_{MON}$ is the current monitor resistor. $R_{MON}$ is connected from IMON pin to FBRTN.
$R_{LIM}$ is the current limit resistor.
$R_O$ is the output load line resistance.
$I_{FS}$ is the output current when the voltage on IMON is at full scale.

### Feedback Loop Compensation Design

Optimized compensation of the ADP3208D allows the best possible response of the regulator's output to a load change. The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output impedance that is entirely resistive over the widest possible frequency range, including dc, and that is equal to the droop resistance ($R_O$). With the resistive output impedance, the output voltage droops in proportion with the load current at any load current slew rate, ensuring the optimal position and allowing the minimization of the output decoupling.

With the multi−mode feedback structure of the ADP3208D, it is necessary to set the feedback compensation so that the converter's output impedance works in parallel with the output decoupling. In addition, it is necessary to compensate for the several poles and zeros created by the output inductor and decoupling capacitors (output filter).

A Type III compensator on the voltage feedback is adequate for proper compensation of the output filter. Figure 43 shows the Type III amplifier used in the ADP3208D. Figure 44 shows the locations of the two poles and two zeros created by this amplifier.

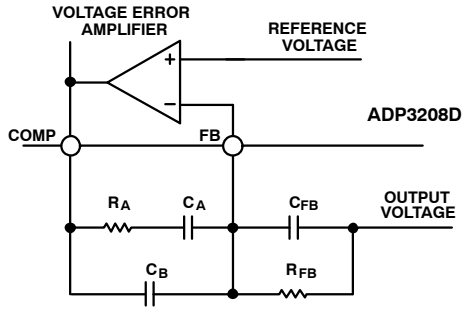



**Figure 43. Voltage Error Amplifier**

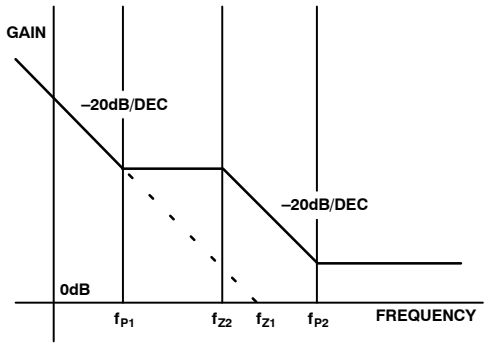



**Figure 44. Poles and Zeros of Voltage Error Amplifier**

The following equations give the locations of the poles and zeros shown in Figure 44:

$$f_{Z1} = \frac{1}{2\pi \times C_A \times R_A} \quad \text{(eq. 29)}$$

$$f_{Z2} = \frac{1}{2\pi \times C_{FB} \times R_{FB}} \quad \text{(eq. 30)}$$

$$f_{P1} = \frac{1}{2\pi\left(C_A + C_B\right) \times R_{FB}} \quad \text{(eq. 31)}$$

$$f_{P2} = \frac{C_A + C_B}{2\pi \times R_A \times C_B + C_A} \quad \text{(eq. 32)}$$

The expressions that follow compute the time constants for the poles and zeros in the system and are intended to yield an optimal starting point for the design; some adjustments may be necessary to account for PCB and component parasitic effects (see the Tuning Procedure for ADP3208D section):

$$R_E = n \times R_O + A_D \times R_{DS} + \frac{R_L \times V_{RT}}{V_{ID}} + \frac{2 \times L \times (1 - (n \times D)) \times V_{RT}}{n \times C_X \times R_O \times V_{VID}} \quad \text{(eq. 33)}$$

$$T_A = C_X \times (R_O - R') + \frac{L_X}{R_O} \times \frac{R_O - R'}{R_X} \quad \text{(eq. 34)}$$

$$T_B = (R_X + R' - R_O) \times C_X \quad \text{(eq. 35)}$$

$$T_C = \frac{V_{RT} \times \left(L - \frac{A_D \times R_{DS}}{2 \times f_{SW}}\right)}{V_{VID} \times R_E} \quad \text{(eq. 36)}$$

$$T_D = \frac{C_X \times C_Z \times R_O{}^2}{C_X \times (R_O - R') + C_Z \times R_O} \quad \text{(eq. 37)}$$

where:

R' is the PCB resistance from the bulk capacitors to the ceramics and is approximately 0.4 mΩ (assuming an 8−layer motherboard).

$R_{DS}$ is the total low−side MOSFET for on resistance per phase.

$A_D$ is 5.

$V_{RT}$ is 1.25 V.

$L_X$ is 150 pH for the six Panasonic SP capacitors.

The compensation values can be calculated as follows:

$$C_A = \frac{n \times R_O \times T_A}{R_E \times R_B} \quad \text{(eq. 38)}$$

$$R_A = \frac{T_C}{C_A} \quad \text{(eq. 39)}$$

$$C_B = \frac{T_B}{R_B} \quad \text{(eq. 40)}$$

$$C_{FB} = \frac{T_D}{R_A} \quad \text{(eq. 41)}$$

The standard values for these components are subject to the tuning procedure described in the Tuning Procedure for ADP3208D section.

### $C_{IN}$ Selection and Input Current DI/DT Reduction

In continuous inductor−current mode, the source current of the high−side MOSFET is approximately a square wave with a duty ratio equal to $n \times V_{OUT}/V_{IN}$ and amplitude that is one−$n^{th}$ of the maximum output current. To prevent large voltage transients, use a low ESR input capacitor sized for the maximum RMS current. The maximum RMS capacitor current occurs at the lowest input voltage and is given by:

$$I_{CRMS} = D \times I_O \times \sqrt{\frac{1}{n \times D} - 1} \quad \text{(eq. 42)}$$

$$I_{CRMS} = 0.18 \times 40\ A \times \sqrt{\frac{1}{2 \times 0.18} - 1} = 9.6\ A$$

where $I_O$ is the output current.

In a typical notebook system, the battery rail decoupling is achieved by using MLC capacitors or a mixture of MLC capacitors and bulk capacitors. In this example, the input capacitor bank is formed by eight pieces of 10 μF, 25 V MLC capacitors, with a ripple current rating of about 1.5 A each.

### Selecting Thermal Monitor Components

To monitor the temperature of a single−point hot spot, set $R_{TTSET1}$ equal to the NTC thermistor's resistance at the alarm temperature. For example, if the alarm temperature for VRTT is 100°C and a Vishey thermistor (NTHS−0603N011003J) with a resistance of 100 kΩ at 25°C, or 6.8 kΩ at 100°C, is used, the user can set $R_{TTSET1}$ equal to 6.8 kΩ (the $R_{TH1}$ at 100°C).

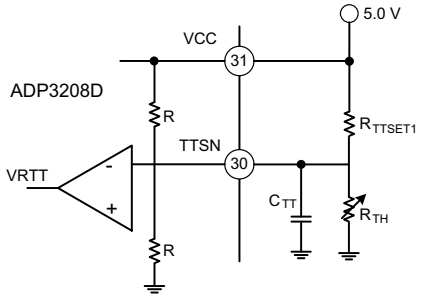



**Figure 45. Single−Point Thermal Monitoring**

To monitor the temperature of multiple−point hot spots, use the configuration shown in Figure 46. If any of the monitored hot spots reaches the alarm temperature, the VRTT signal is asserted. The following calculation sets the alarm temperature:

$$R_{TTSET1} = \frac{\frac{1}{2} + \frac{V_{FD}}{V_{REF}}}{\frac{1}{2} - \frac{V_{FD}}{V_{REF}}} R_{TH1ALARMTEMPERATURE} \quad \text{(eq. 43)}$$

where $V_{FD}$ is the forward drop voltage of the parallel diode.

Because the forward current is very small, the forward drop voltage is very low, that is, less than 100 mV. Assuming the same conditions used for the single−point thermal monitoring example, that is, an alarm temperature of 100°C and use of an NTHS−0603N011003J Vishay thermistor; solving Equation 43 gives a $R_{TTSET}$ of 7.37 kΩ, and the closest standard resistor is 7.32 kΩ (1%).

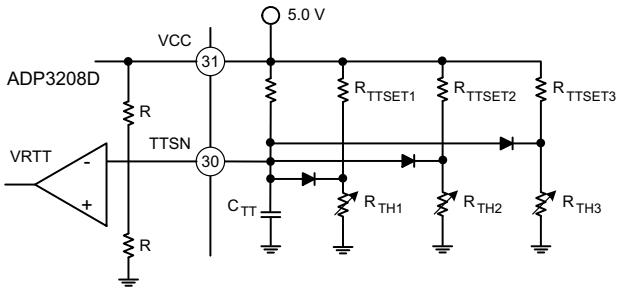



**Figure 46. Multiple−Point Thermal Monitoring**

The number of hot spots monitored is not limited. The alarm temperature of each hot spot can be individually set by using different values for $R_{TTSET1}$, $R_{TTSET2}$, ... $R_{TTSETn}$.

## Tuning Procedure for ADP3208D

### Set Up and Test the Circuit

1. Build a circuit based on the compensation values computed from the design spreadsheet.
2. Connect a dc load to the circuit.
3. Turn on the ADP3208D and verify that it operates properly.
4. Check for jitter with no load and full load conditions.

### Set the DC Load Line

1. Measure the output voltage with no load ($V_{NL}$) and verify that this voltage is within the specified tolerance range.
2. Measure the output voltage with a full load when the device is cold ($V_{FLCOLD}$). Allow the board to run for ~10 minutes with a full load and then measure the output when the device is hot ($V_{FLHOT}$). If the difference between the two measured voltages is more than a few millivolts, adjust $R_{CS2}$ using Equation 44.

$$R_{CS2(NEW)} = R_{CS2(OLD)} \times \frac{V_{NL} - V_{FLCOLD}}{V_{NL} - V_{FLHOT}} \quad \text{(eq. 44)}$$

3. Repeat Step 2 until no adjustment of $R_{CS2}$ is needed.
4. Compare the output voltage with no load to that with a full load using 5 A steps. Compute the load line slope for each change and then find the average to determine the overall load line slope ($R_{OMEAS}$).
5. If the difference between $R_{OMEAS}$ and $R_O$ is more than 0.05 mΩ, use the following equation to adjust the $R_{PH}$ values:

$$R_{PH(NEW)} = R_{PH(OLD)} \times \frac{R_{OMEAS}}{R_O} \quad \text{(eq. 45)}$$

6. Repeat Steps 4 and 5 until no adjustment of $R_{PH}$ is needed. Once this is achieved, do not change $R_{PH}$, $R_{CS1}$, $R_{CS2}$, or $R_{TH}$ for the rest of the procedure.
7. Measure the output ripple with no load and with a full load with scope, making sure both are within the specifications.

### Set the AC Load Line

1. Remove the dc load from the circuit and connect a dynamic load.
2. Connect the scope to the output voltage and set it to dc coupling mode with a time scale of 100 μs/div.
3. Set the dynamic load for a transient step of about 40 A at 1 kHz with 50% duty cycle.
4. Measure the output waveform (note that use of a dc offset on the scope may be necessary to see the waveform). Try to use a vertical scale of 100 mV/div or finer.

5. The resulting waveform will be similar to that shown in Figure 47. Use the horizontal cursors to measure $V_{ACDRP}$ and $V_{DCDRP}$, as shown in Figure 47. Do not measure the undershoot or overshoot that occurs immediately after the step.

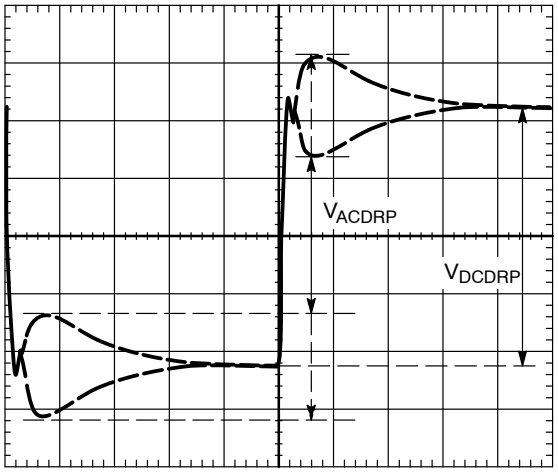



**Figure 47. AC Loadline Waveform**

6. If the difference between $V_{ACDRP}$ and $V_{DCDRP}$ is more than a couple of millivolts, use Equation 46 to adjust $C_{CS}$. It may be necessary to try several parallel values to obtain an adequate one because there are limited standard capacitor values available (it is a good idea to have locations for two capacitors in the layout for this reason).

$$C_{CS(NEW)} = C_{CS(OLD)} \times \frac{V_{ACDRP}}{V_{DCDRP}} \quad \text{(eq. 46)}$$

7. Repeat Steps 5 and 6 until no adjustment of $C_{CS}$ is needed. Once this is achieved, do not change $C_{CS}$ for the rest of the procedure.
8. Set the dynamic load step to its maximum step size (but do not use a step size that is larger than needed) and verify that the output waveform is square, meaning $V_{ACDRP}$ and $V_{DCDRP}$ are equal.
9. Ensure that the load step slew rate and the powerup slew rate are set to ~150 A/μs to 250 A/μs (for example, a load step of 50 A should take 200 ns to 300 ns) with no overshoot. Some dynamic loads have an excessive overshoot at powerup if a minimum current is incorrectly set (this is an issue if a VTT tool is in use).

### Set the Initial Transient

1. With the dynamic load set at its maximum step size, expand the scope time scale to 2 μs/div to 5 μs/div. This results in a waveform that may have two overshoots and one minor undershoot before achieving the final desired value after $V_{DROOP}$ (see Figure 48).

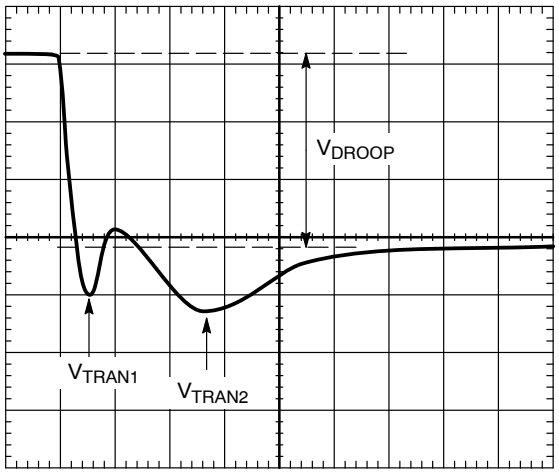



**Figure 48. Transient Setting Waveform, Load Step**

2. If both overshoots are larger than desired, try the following adjustments in the order shown.
   a. Increase the resistance of the ramp resistor ($R_{RAMP}$) by 25%.
   b. For $V_{TRAN1}$, increase $C_B$ or increase the switching frequency.
   c. For $V_{TRAN2}$, increase $R_A$ by 25% and decrease $C_A$ by 25%.
   If these adjustments do not change the response, it is because the system is limited by the output decoupling. Check the output response and the switching nodes each time a change is made to ensure that the output decoupling is stable.
3. For load release (see Figure 49), if $V_{TRANREL}$ is larger than the value specified by IMVP−6+, a greater percentage of output capacitance is needed. Either increase the capacitance directly or decrease the inductor values. (If inductors are changed, however, it will be necessary to redesign the circuit using the information from the spreadsheet and to repeat all tuning guide procedures).

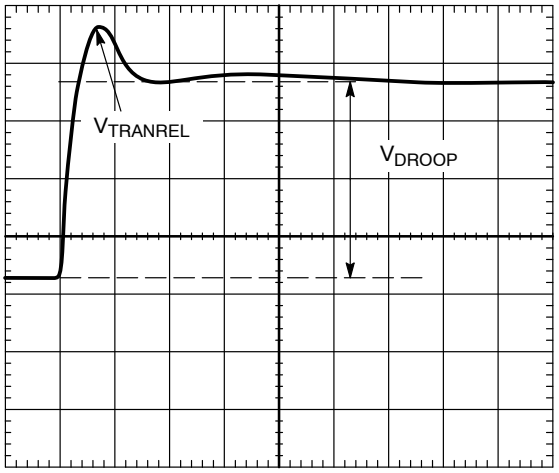



**Figure 49. Transient Setting Waveform, Load Release**

## Layout and Component Placement

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

### General Recommendations

1. 1. For best results, use a PCB of four or more layers. This should provide the needed versatility for control circuitry interconnections with optimal placement; power planes for ground, input, and output; and wide interconnection traces in the rest of the power delivery current paths. Keep in mind that each square unit of 1 oz copper trace has a resistance of ~0.53 mΩ at room temperature.
2. When high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.
3. If critical signal lines (including the output voltage sense lines of the ADP3208D) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of increasing signal ground noise.
4. An analog ground plane should be used around and under the ADP3208D for referencing the components associated with the controller. This plane should be tied to the nearest ground of the output decoupling capacitor, but should not be tied to any other power circuitry to prevent power currents from flowing into the plane.
5. The components around the ADP3208D should be located close to the controller with short traces. The most important traces to keep short and away from other traces are those to the FB and CSSUM pins. Refer to Figure 42 for more details on the layout for the CSSUM node.
6. The output capacitors should be connected as close as possible to the load (or connector) that receives the power (for example, a microprocessor core). If the load is distributed, the capacitors should also be distributed and generally placed in greater proportion where the load is more dynamic.
7. Avoid crossing signal lines over the switching power path loop, as described in the Power Circuitry section.

### Power Circuitry

1. The switching power path on the PCB should be routed to encompass the shortest possible length to minimize radiated switching noise energy (that is, EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system as well as noise−related operational problems in the power−converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs, including all interconnecting PCB traces and planes. The use of short, wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high energy ringing, and it accommodates the high current demand with minimal voltage loss.
2. When a power−dissipating component (for example, a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are improved current rating through the vias and improved thermal performance from vias extended to the opposite side of the PCB, where a plane can more readily transfer heat to the surrounding air. To achieve optimal thermal dissipation, mirror the pad configurations used to heat sink the MOSFETs on the opposite side of the PCB. In addition, improvements in thermal performance can be obtained using the largest possible pad area.
3. The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.
4. For best EMI containment, a solid power ground plane should be used as one of the inner layers and extended under all power components.

### Signal Circuitry

1. The output voltage is sensed and regulated between the FB and FBRTN pins, and the traces of these pins should be connected to the signal ground of the load. To avoid differential mode noise pickup in the sensed signal, the loop area should be as small as possible. Therefore, the FB and FBRTN traces should be routed adjacent to each other, atop the power ground plane, and back to the controller.
2. The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be Kelvin connected to the center point of the copper bar, which is the $V_{CORE}$ common node for the inductors of all the phases.
3. On the back of the ADP3208D package, there is a metal pad that can be used to heat sink the device. Therefore, running vias under the ADP3208D is not recommended because the metal pad may cause shorting between vias.

## ORDERING INFORMATION

| Device | Temperature Range | Package | Package Option | Shipping† |
|---|---|---|---|---|
| ADP3208DJCPZ−RL | −10°C to 100°C | 48−Lead Frame Chip Scale Package [LFCSP_VQ] | CP−48−1 | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*The “Z” suffix indicates Pb−Free part.

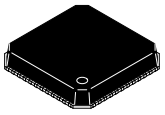
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# MECHANICAL CASE OUTLINE
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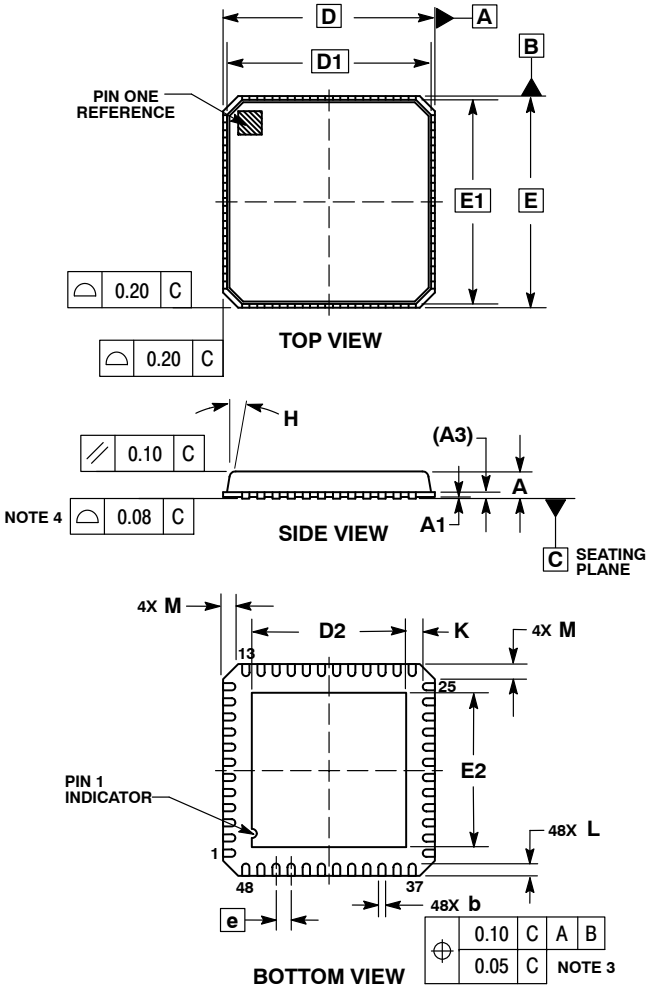
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CASE 932AD−01
ISSUE A

DATE 23 JAN 2009



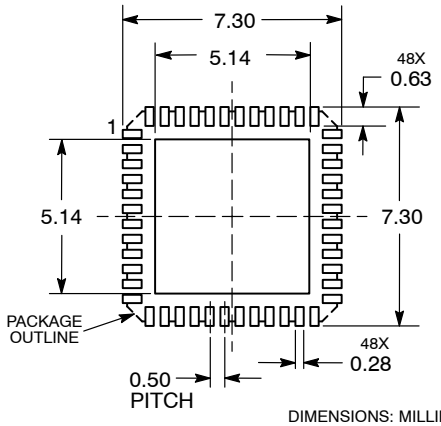
**SCALE 2:1**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 7.00 BSC | |
| D1 | 6.75 BSC | |
| D2 | 4.95 | 5.25 |
| E | 7.00 BSC | |
| E1 | 6.75 BSC | |
| E2 | 4.95 | 5.25 |
| e | 0.50 BSC | |
| H | --- | 12° |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |
| M | --- | 0.60 |

**SOLDERING FOOTPRINT***




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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