

钍地半导体
Tudi Semiconductor

Product Specification

TUDI-ADM3493

3.3 V Slew Rate Limited, Half Duplex RS-485/RS-422 Transceiver

网址 www.sztdbdt.com

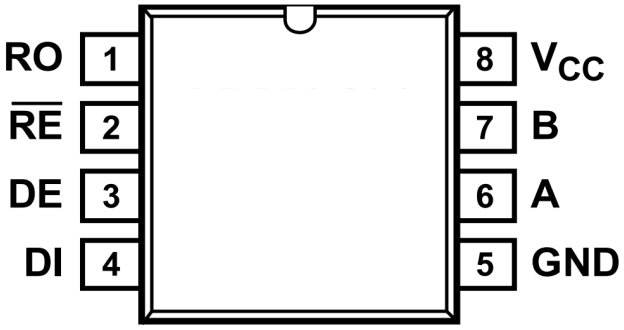
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

FEATURES

- Operates with 3.3 V supply
- Interoperable with 5 V logic
- EIA RS-422 and RS-485 compliant over full CM range
- Data rate: 250 kbps
- Half duplex transceiver
- Reduced slew rates for low EMI
- 2 nA supply current in shutdown mode
- Up to 256 transceivers on a bus
- -7 V to +12 V bus common-mode range
- Specified over -40°C to +85°C temperature range
- 8 ns skew
- Available in 8-lead SOIC



SOP8 Pin Configuration

APPLICATIONS

- Low power RS-485 applications
- EMI sensitive systems
- DTE-DCE interfaces
- Industrial control
- Packet switching
- Local area networks
- Level translators

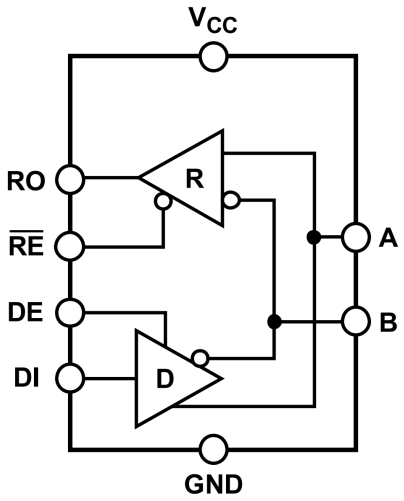
DESCRIPTION

The ADM3493 is a low power, differential line transceiver designed to operate using a single 3.3 V power supply. Low power consumption, coupled with a shutdown mode, makes it ideal for power-sensitive applications. The ADM3493 is suitable for communication on multipoint bus transmission lines.

The device contains one driver and one receiver. Designed for half-duplex communication, the ADM3493 features a slew rate limited driver that minimizes EMI and reduces reflections caused by improperly terminated cables, allowing error-free data transmission at data rates up to 250 kbps. The receiver input impedance is 96 kΩ, allowing up to 256 transceivers to be connected on the bus . A thermal shutdown circuit prevents excessive power dissipation caused by bus contention or by output shorting. If a significant temperature increase is detected in the internal driver circuitry during fault conditions then the thermal shutdown circuit forces the driver output into a high impedance state. The receiver contains a fai-safe feature that results in a logic high output state, if the inputs are unconnected (floating).

The ADM3493 is fully specified over the commercial and industrial temperature ranges and is available in an 8-lead SOIC.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

T_A= 25°C, unless otherwise noted.

Table 1.

Parameter	Rating
V_{CC} to GND	7V
Digital /O Voltage(DE,RE,DI)	-0.3V to V_{CC}+0.3V
Digital I/O Voltage(Rout)	V_{CC}-0.5V to V_{CC}+0.5V
Driver Output/Receiver Input Voltage	-7.5V to +12.5V
Operating Temperature Range	-40℃ to+85℃
Storage Temperature Range	-65℃ to +125℃
θ_{JA} Thermal Impedance	
8-Lead SOIC	121℃/W
Lead Temperature	
Soldering(10 seconds)	300℃
Vapor Phase(60 seconds)	215℃
Infrared(15 seconds)	220℃

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges.
Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

FUNCTION DESCRIPTIONS

Table 2 . Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RO	Receiver Output.When enabled,if A>B by 200 mV,then RO= high.If A<Bby 200 mV,then RO=low.
2	RE	Receiver Output Enable.A low level enables the receiver output,RO.A high levelplaces it in a high impedance state.If RE is high and DE is low,the device enters a lowpower shutdown mode.
3	DE	Driver Output Enable.A high level enables the driver differential Outputs A and B.A low level places it in a high impedance state.If RE is high and DE is low,the device enters a low power shutdown mode.
4 5	DIGND	Driver Input.When the driver is enabled,a logic low on DI forces A low and B high while a logic high on DI forces A high and B low.Ground.
6	A	Noninverting Receiver Input A and Noninverting Driver Output A.
7	B	Inverted Receiver Input B and Inverted Driver Output B.
8	V_{CC}	Power Supply,3.3V±0.3V.

SPECIFICATIONS

Table 3.

V_{CC} = 3.3 V ±0.3 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DRIVER					
Differential Output Voltage,V_{OD}	2.0			V	R_L=100Ω(RS-422),Vcc=3.3V±5%(see Figure 1)
	1.5			V	R_L=54Ω(RS-485) (see Figure 1)
	1.5			V	R_L=60Ω(RS-485),Vcc=3.3V (see Figure 2)
△|Vop|for Complementary Output States(1)			0.2	V	R_L=54Ωor 100Ω (see Figure 1)
Common-Mode Output Voltage,Voc			3	V	R_L=54Ωor 100Ω (see Figure 1)
△|Voc|for Common-Mode Output Voltage			0.2	V	R_L=54Ωor 100Ω (see Figure 1)
DRIVER INPUT LOGIC					
CMOSInput Logic Threshold Low,V_{IH}			0.8	V	DE,DI,RE
CMOSInput Logic Threshold High,V_{IL}	2.0			V	DE,DI,RE
CMOS Logic Input Current,I_{N1}			±2	μA	DE,DI,RE
Input Current(A,B),I_{N2}		60		μA	V_{IN}=12V; DE=0V, Vcc=0V or 3.6V
		-60		μA	V_{IN}=-7V; DE=0V, Vcc=0V or 3.6V
RECEIVER					
Differential Input Threshold Voltage, V_{TH}	-0.2		0.2	V	-7V<V_{CM}<+12V
Input Hysteresis,△V_{TH}		50		mV	V_{CM}=0V
CMOS Output Voltage High,V_{OH}	Vcc-0.4			V	I_{OUT}=-1.5 mA,V_{ID}=200 mV (see Figure 3)
CMOS Output Voltage Low,V_{OL}			0.4	V	I_{OUT}=2.5mA,V_{ID}=200mV(see Figure 3)
Three-State Output Leakage Current, I_{OZR}			± 1	μA	Vcc=3.6V,0V≤V_{OUT}≤Vcc
Input Resistance,R_{IN}		96		kΩ	-7V<V_{CM}<+12V

Table 3. (continued)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments	
POWER SUPPLY CURRENT						
Supply Current		1.1	2.2	mA	DE=Vcc RE=0VorVcc	No load,DI=0V or Vcc
		0.95	1.9	mA	DE=Vcc RE=0V	
Supply Current in Shutdown Mode, I_{SHDN}		0.002	1	μA	DE=0V,RE=Vcc,DI=Vcc or 0V	
Driver Short-Circuit Output Current, I_{OSD}			-250	mA	V_{OUT}=-7V	
			250	mA	V_{OUT}=12V	
Receiver Short-Circuit Output Current, I_{OSR}	±8		± 60	mA	0V<V_{RO}<Vcc	

(1) ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when DI input changes state.

TIMING SPECIFICATIONS

Table 4.

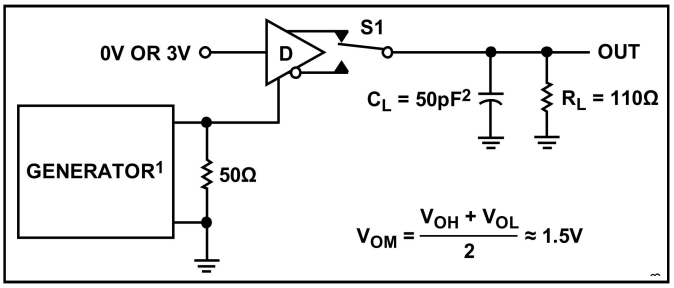
V_{CC} = 3.3 V, T_A = 25°C, unless otherwise noted.

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DRIVER					
Differential Output Delay, t_{DD}	600	900	1400	ns	R_L=60Ω(see Figure 4 and Figure 10)
Differential Output Transition Time, t_{TD}	400	700	1200	ns	R_L=60Ω(see Figure 4 and Figure 10)
Propagation Delay,Low-to-High Level, t_{PLH}	700	1000	1500	ns	R_L=27Ω(see Figure 5 and Figure 11)
Propagation Delay,High-to-Low Level, t_{PHL}	700	1000	1500	ns	R_L=27Ω(see Figure 5 and Figure 11)
tPLH-tPHL|Propagation Delay Skew(1), t_{PDS}		100		ns	R_L=27Ω(see Figure 5 and Figure 11)
DRIVER OUTPUT ENABLE/DISABLE TIMES					
Output Enable Time to Low Level, t_{PZL}		900	1300	ns	R_L=110Ω(see Figure 7 and Figure 13)
Output Enable Time to High Level, t_{PZH}		600	800	ns	R_L=110Ω(see Figure 6 and Figure 12)
Output Disable Time from High Level, t_{PHZ}		50	80	ns	R_L=110Ω(see Figure 6 and Figure 12)
Output Disable Time from Low Level, t_{PLZ}		50	80	ns	R_L=110Ω(see Figure 7 and Figure 13)
Output Enable Time from Shutdown to Low Level, t_{PSL}		1.9	2.7	μs	R_L=110Ω(see Figure 7 and Figure 13)
Output Enable Time from Shutdown to High Level, t_{PSH}		2.2	3.0	μs	R_L=110Ω(see Figure 6 and Figure 12)
RECEIVER					
Time to Shutdown², t_{SHDN}	80	190	300	ns	
Propagation Delay,Low-to-High Level, t_{RPLH}	25	75	180	ns	V_{ID}=0V to 3.0V,CL=15pF(see Figure 8 and Figure 14)
Propagation Delay,High-to-Low Level, t_{RPHL}	25	75	180	ns	V_{ID}=0V to 3.0V,CL=15 pF(see Figure 8 and Figure 14)
|tPLH-tPHL|Propagation Delay Skew, t_{RPDS}			50	ns	V_{ID}=0V to 3.0V,CL=15pF(see Figure 8 and Figure 14)

Table 4. (continued)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
RECEIVER OUTPUT ENABLE/DISABLE TIMES					
Output Enable Time to Low Level, t_{PRZL}		25	50	ns	C_L=15 pF(see Figure 9 and Figure 15)
Output Enable Time to High Level, t_{PRZH}		25	50	ns	C_L=15 pF(see Figure 9 and Figure 15)
Output Disable Time from High Level, t_{PRHZ}		25	45	ns	C_L=15 pF(see Figure 9 and Figure 15)
Output Disable Time from Low Level, t_{PRLZ}		25	45	ns	C_L=15 pF(see Figure 9 and Figure 15)
Output Enable Time from Shutdown toLow Level, t_{PRSL}		720	1400	ns	C_L=15 pF(see Figure 9 and Figure 15)
Output Enable Time from Shutdown toHigh Level, t_{PRSH}		720	1400	ns	C_L=15 pF(see Figure 9 and Figure 15)

(1) Measured on $|t_{PLH}$ (A) - t_{PHL} (A)| and $|t_{PLH}$ (B) - t_{PHL} (B)|.
(2) The transceivers are put into shutdown by bringing RE high and DE low. If the inputs are in this state for less than 80 ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 300 ns, the parts are guaranteed to enter shutdown.



[1]PPR = 250kHz, 50% DUTY CYCLE, tR≤ 6.0ns, Z_O= 50Ω.
[2]C_L INCLUDES PROBE AND STRAY CAPACITANCE.

OC

Figure 6. Driver Enable and Disable Times (t_{PZH}, t_{PSH}, t_{PHZ})

TEST CIRCUITS

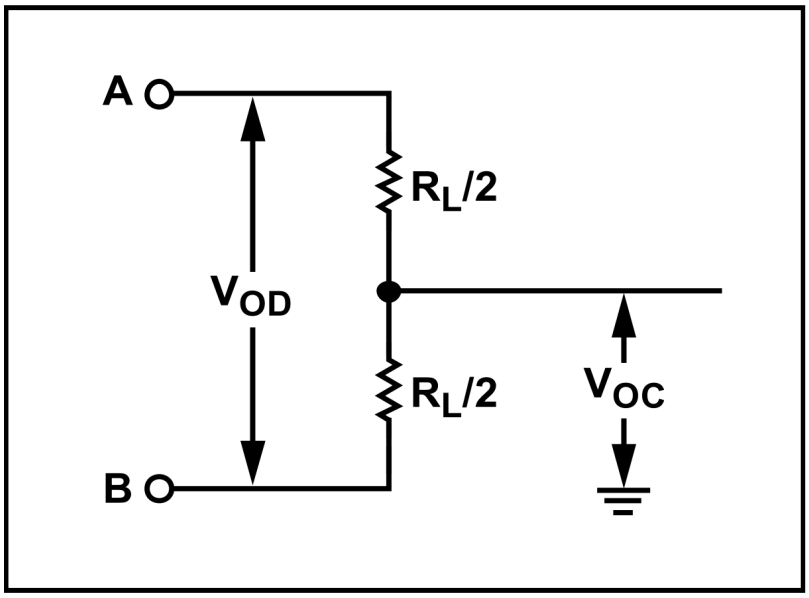


Figure 1. Driver V_{OD} and V_{OC}

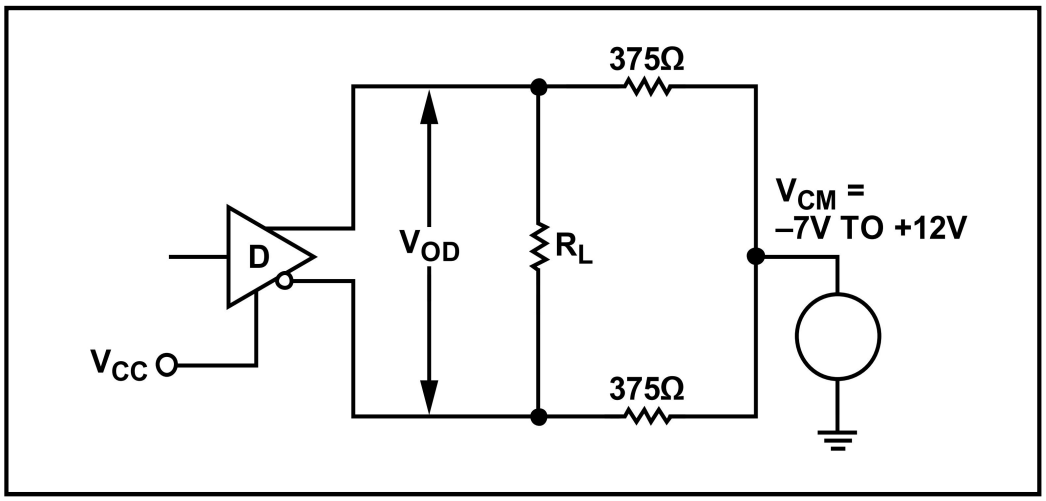


Figure 2. Driver VOD with Varying Common-Mode Voltage

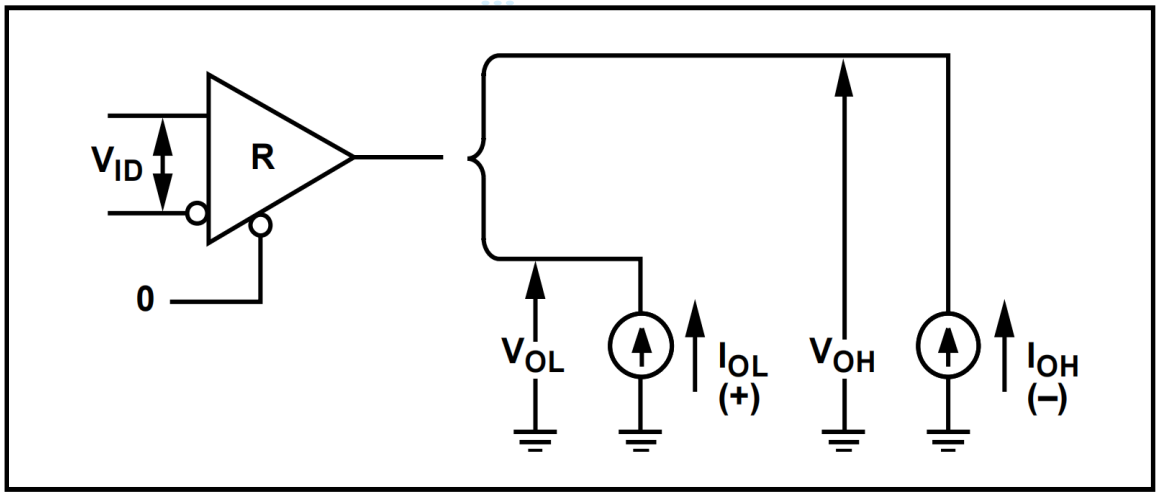
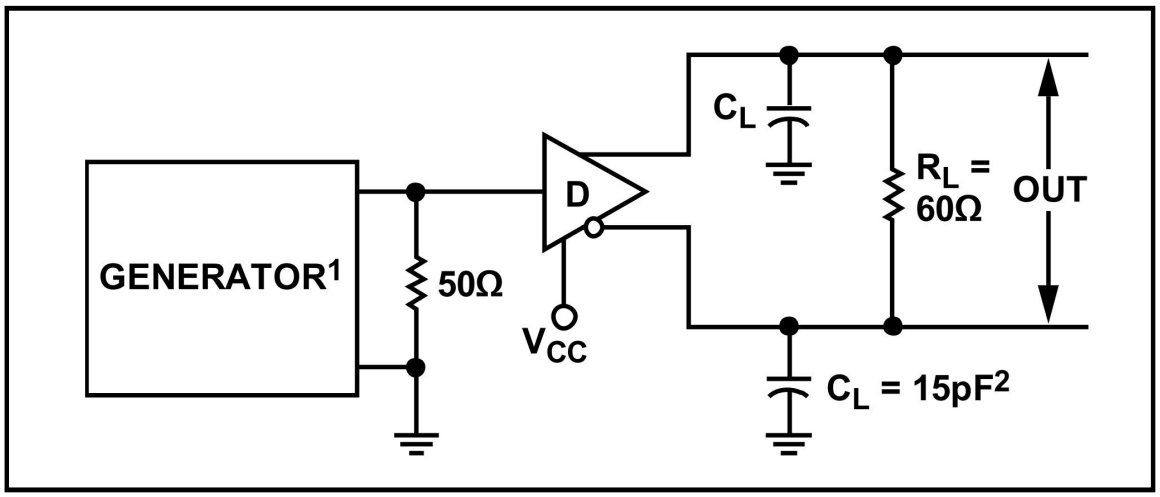
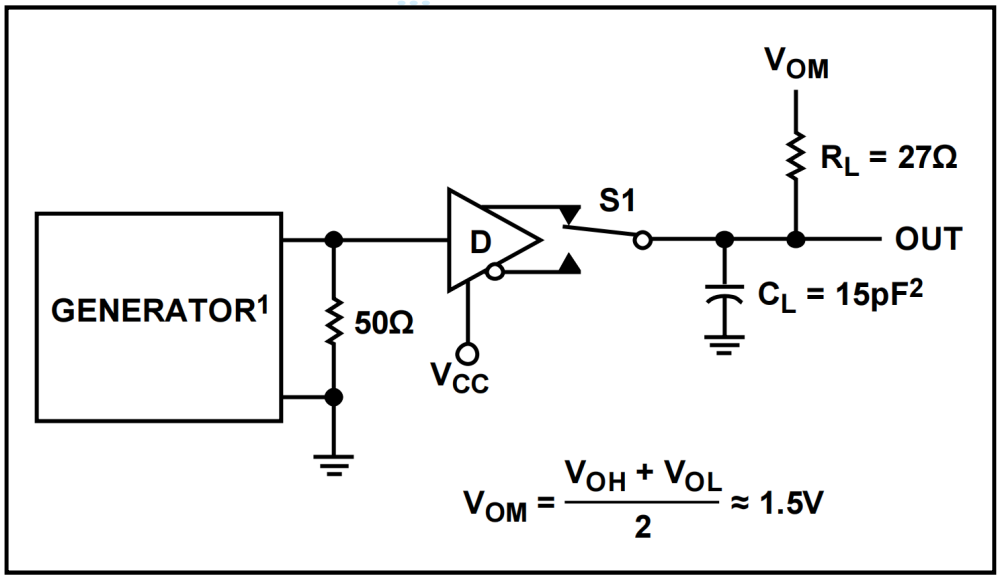


Figure 3. Receiver V_{OH} and V_{OL}



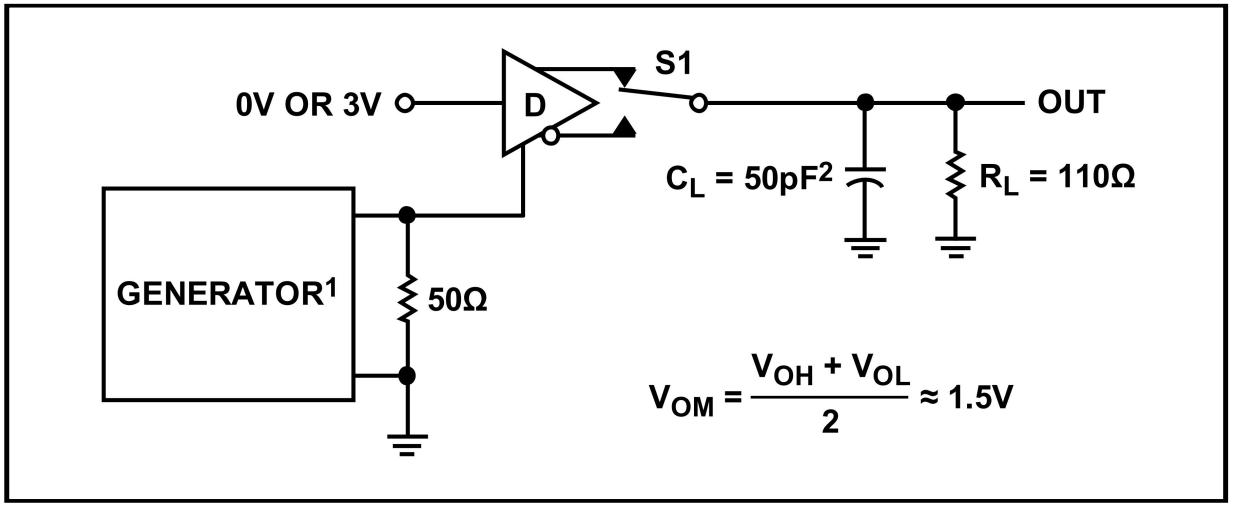
(1)PPR = 250kHz, 50% DUTY CYCLE, $t_R \leq$ 6.0ns, ZO = 50Ω.
(2)CL INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 4. Driver Differential Output Delay and Transition Times



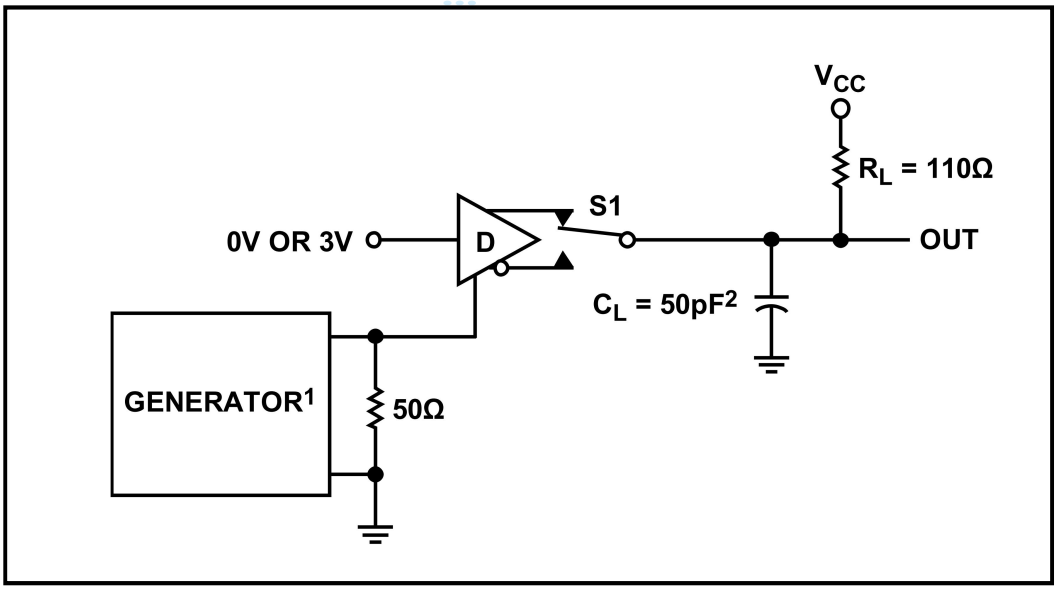
(1) PPR = 250kHz, 50% DUTY CYCLE, $t_R \leq$ 6.0ns, Z_O = 50Ω.
(2) CL INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 5. Driver Propagation Delays



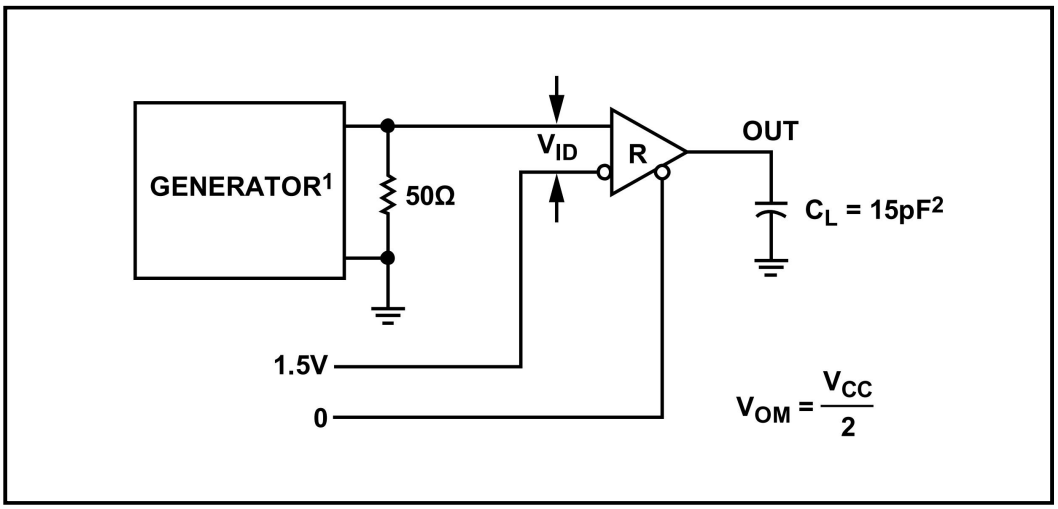
(1) PPR = 250kHz, 50% DUTY CYCLE, $t_R \leq$ 6.0ns, Z_O = 50Ω.
(2) CL INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 6. Driver Enable and Disable Times (t_{PZH}, t_{PSH}, t_{PHZ})



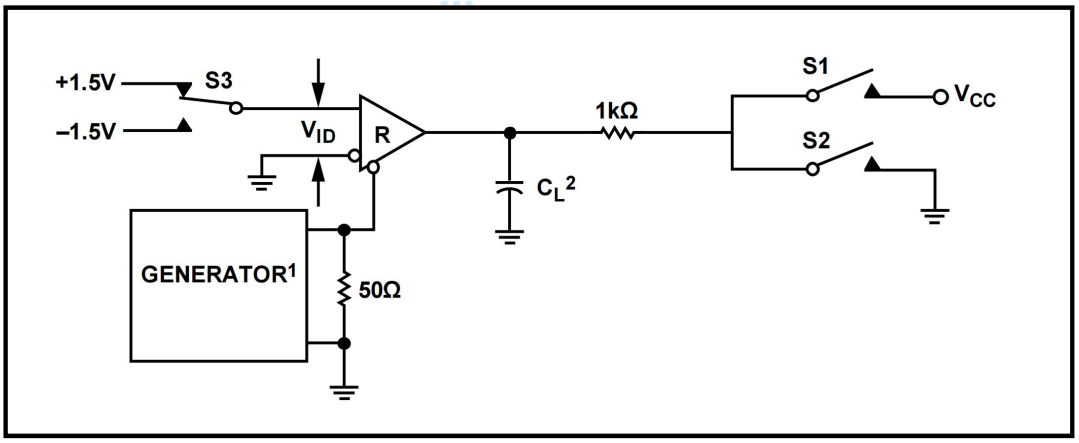
(1) PPR = 250kHz, 50% DUTY CYCLE, $t_R \leq$ 6.0ns, Z_O = 50Ω.
(2) CL INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 7. Driver Enable and Disable Times (t_{PZL}, t_{PSL}, t_{PLZ})



(1)PPR = 250kHz, 50% DUTY CYCLE, $t_R \leq$ 6.0ns, ZO = 50Ω.
(2) CL INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 8. Receiver Propagation Delay



(1) PPR = 250kHz, 50% DUTY CYCLE, tR ≤ 6.0ns, ZO = 50Ω.
(2) CL INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 9. Receiver Enable and Disable Times

SWITCHING CHARACTERISTICS

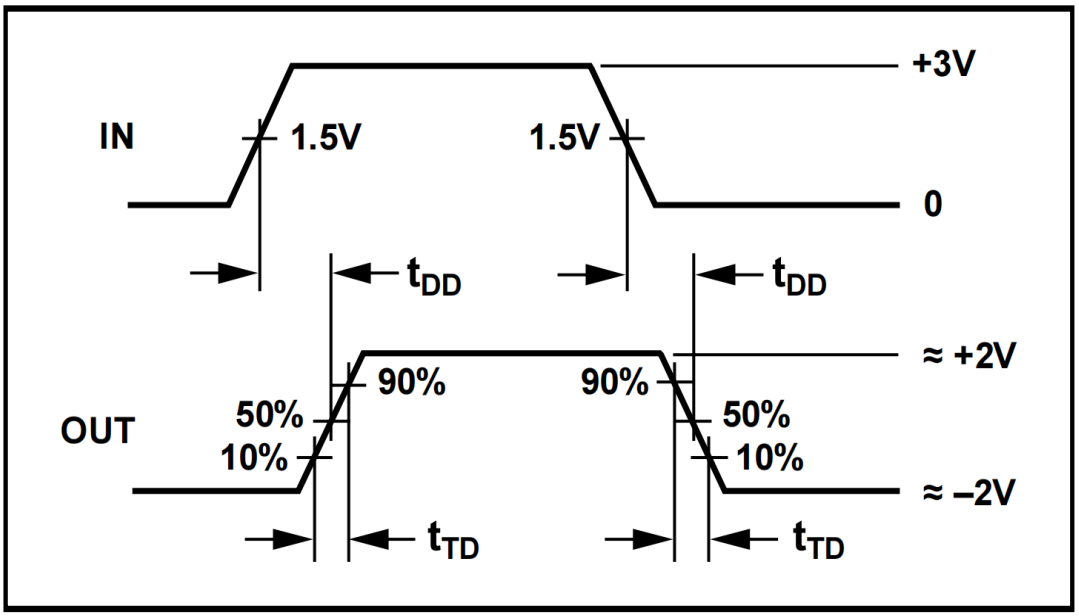


Figure 10. Driver Differential Output Delay and Transition Times

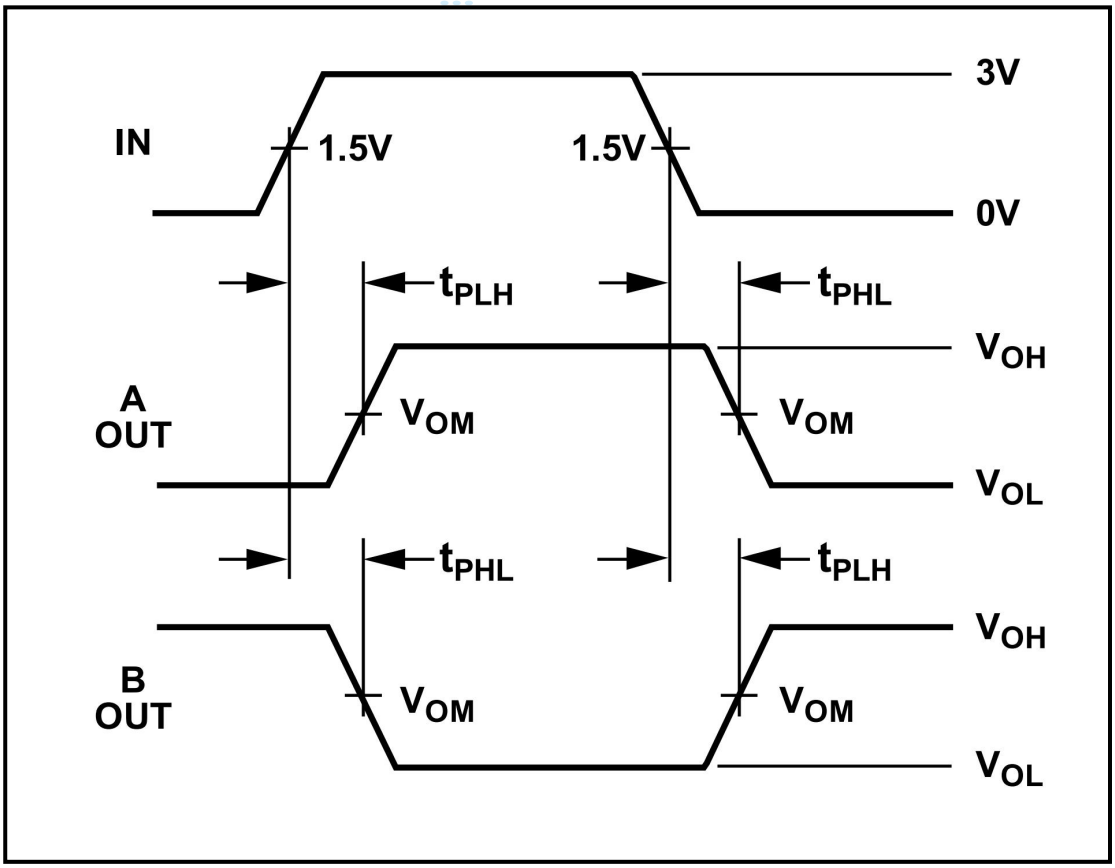


Figure 11. Driver Propagation Delays

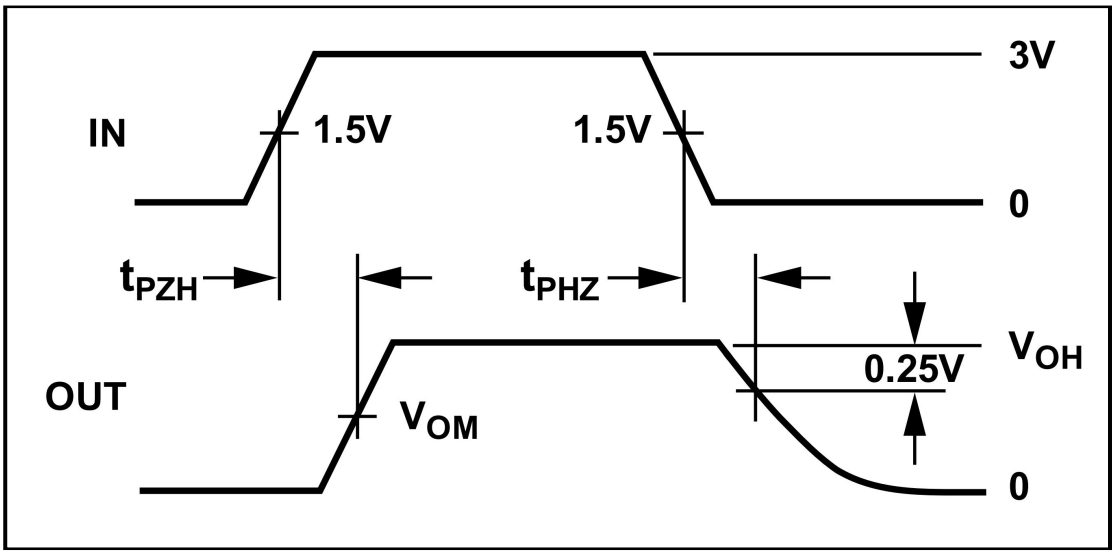


Figure 14. Driver Enable and Disable Times (t_{PZH},t_{PSH}, t_{PHZ})

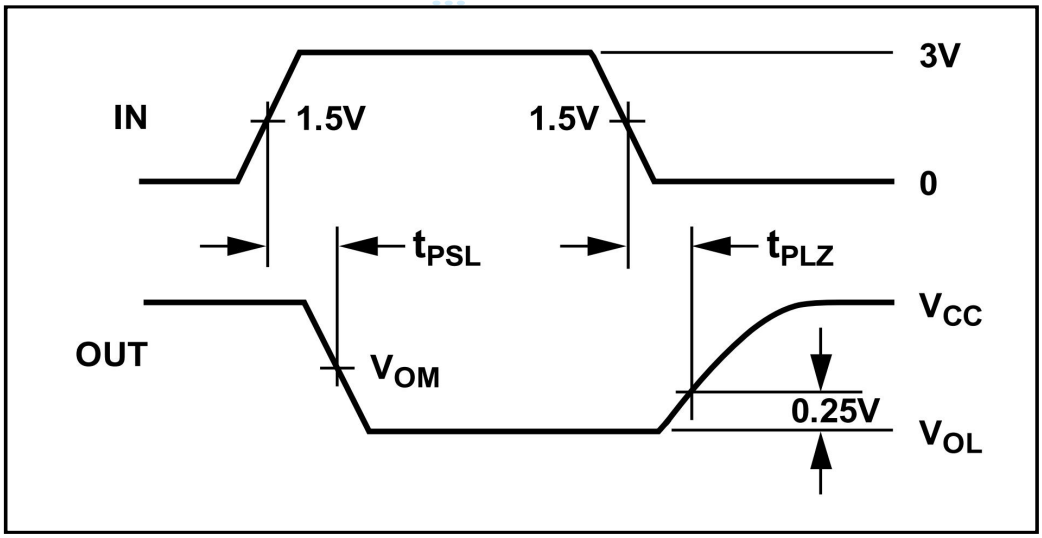


Figure 15. Driver Enable and Disable Times (t_{PZL}, t_{PSL}, t_{PLZ})

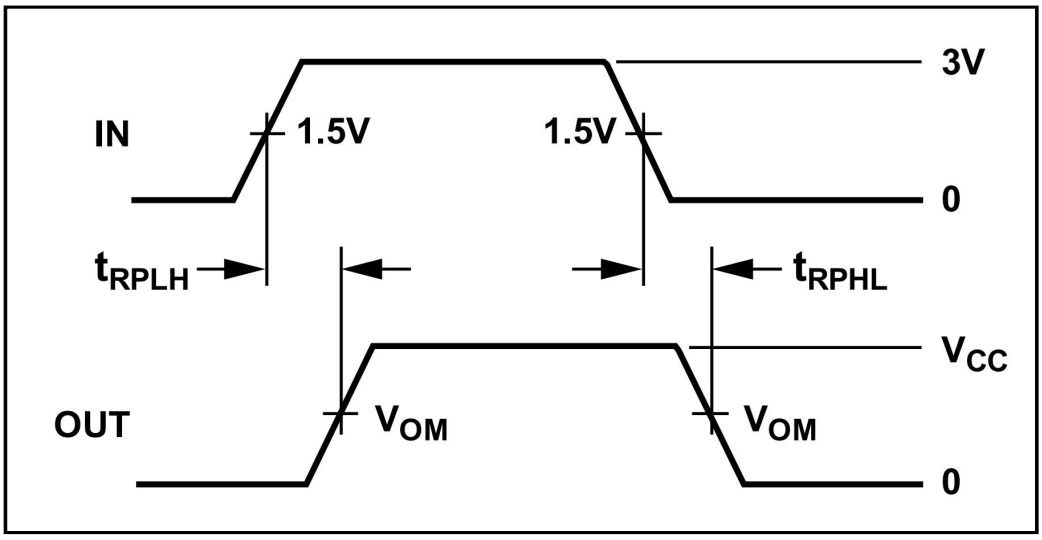


Figure 14. Receiver Propagation Delay

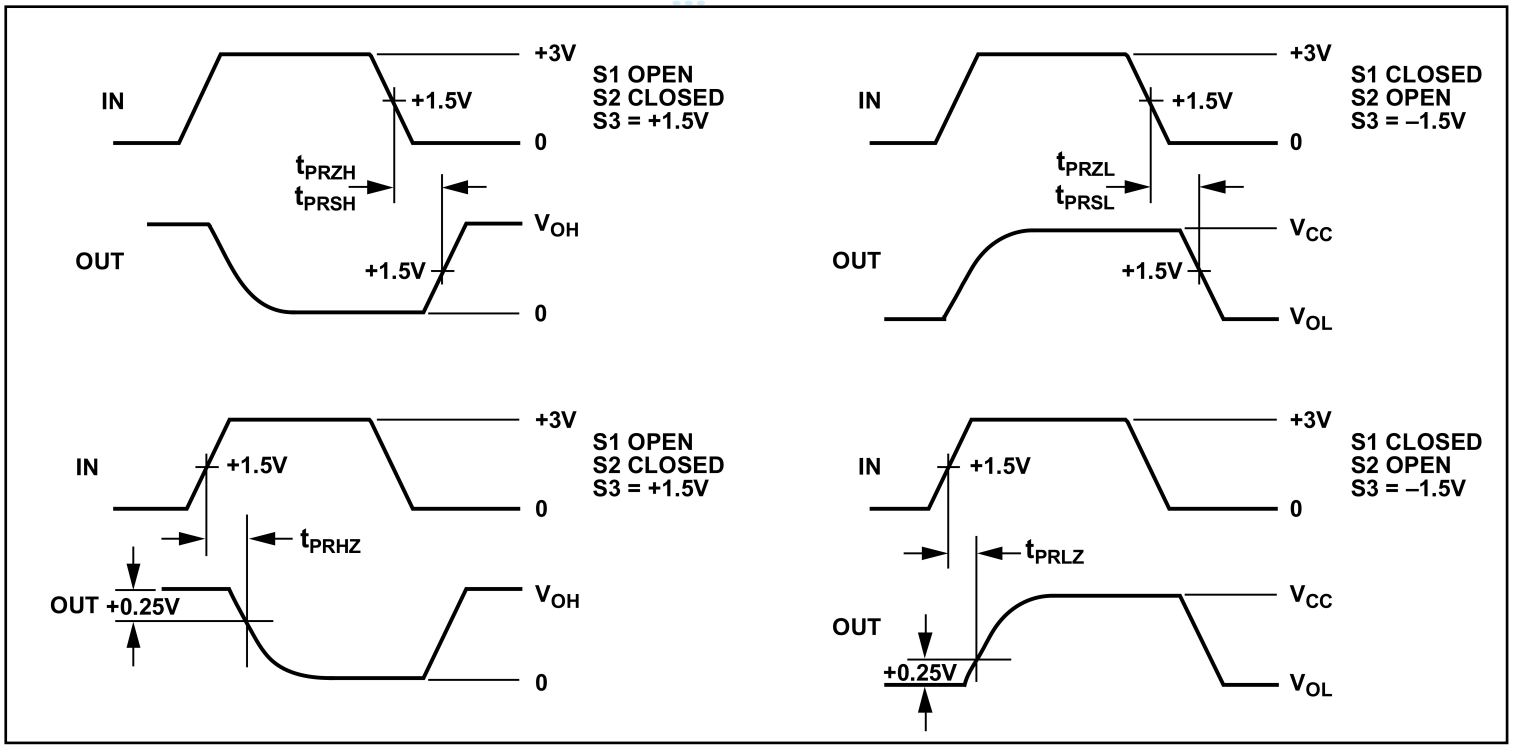


Figure 15. Receiver Enable and Disable Times

CIRCUIT DESCRIPTION

The ADM3493 is a low power transceiver for RS-485 and RS-422 communications. The ADM3493 can transmit and receive at data rates up to 250 kbps in a half duplex configuration. Driver Enable (DE) and Receiver Enable (RE) pins are included when disabled; the driver and receiver outputs are high impedance.

REDUCED EMI AND REFLECTIONS ：The ADM3493 is a slew rate limited transceiver, minimizing EMI and reducing reflections caused by improperly terminated cables.

LOW POWER SHUTDOWN MODE：A low power shutdown mode is initiated by bringing both RE high and DE low. The ADM3493 does not shut down unless both the driver and receiver are disabled (high impedance). In shutdown, the ADM3493 typically draws only 2 nA of supply current. For the ADM3493, the t_{PSH} and t_{PSL} enable times assume the part was in the low power shutdown mode; the t_{PZH} and t_{PZL} enable times assume the receiver or driver was disabled, but the part was not shut down.

DRIVER OUTPUT PROTECTION：Two methods are implemented to prevent excessive output current and power dissipation caused by faults or by bus contention. Current limit protection on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see Typical Performance Characteristics). In addition, a thermal shutdown circuit forces the driver outputs into a high impedance state if the die temperature rises excessively .

PROPAGATION DELAY：Skew time is simply the difference between the low-to-high and high-to-low propagation delay. Small driver/receiver skew times help maintain a symmetrical mark-space ratio (50% duty cycle). The receiver skew time, $|t_{PRLH} - t_{PRHL}|$, is 20 ns for the ADM3493. The driver skew time is typically under 100 ns.

TYPICAL APPLICATIONS：The ADM3493 transceiver is designed for bidirectional data communications on multipoint bus transmission lines. Figure 22 shows a typical network application ’ s circuits. To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew rate limited ADM3493 is tolerant of imperfect termination.

Table 5. Transmitting Truth Table

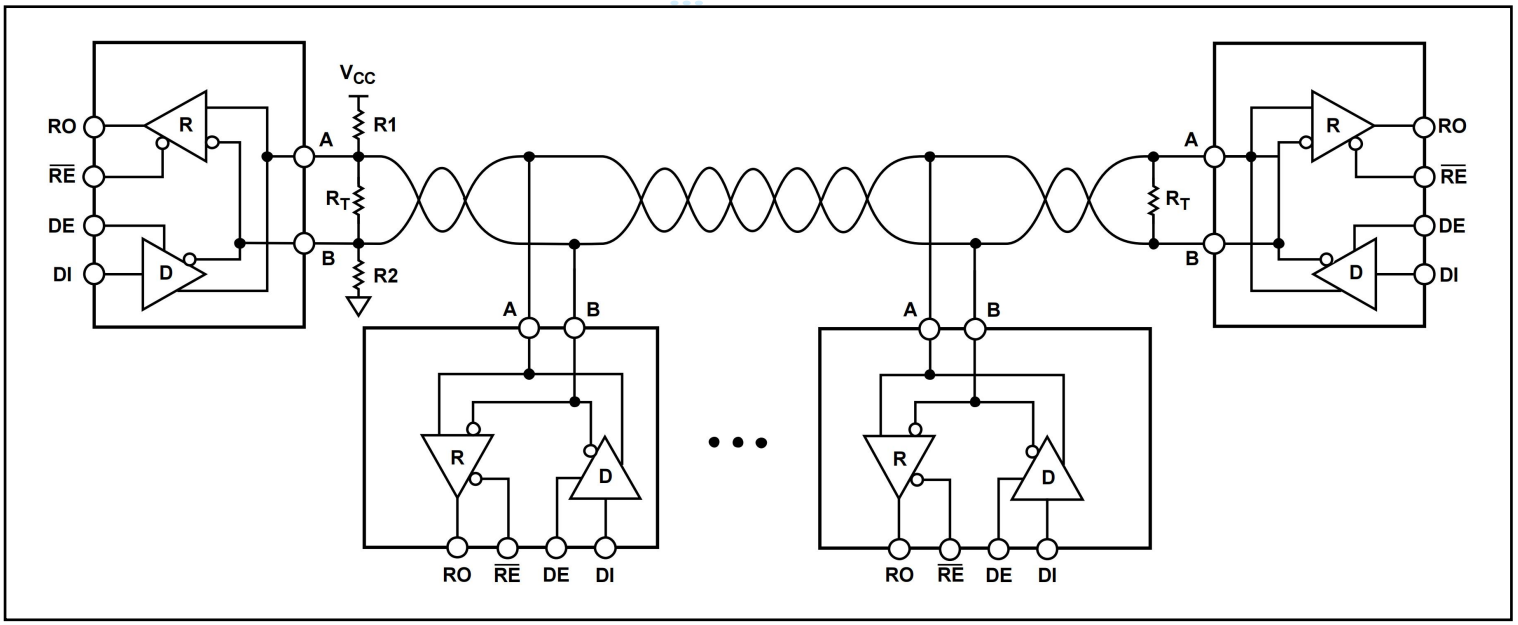
Transmitting Inputs			Transmitting Outputs		Mode
RE	DE	DI	B	A	
X（1）	1	1	0	1	Normal
X（1）	1	0	1	0	Normal
0	0	X（1）	High-Z（2）	High-Z（2）	Normal
1	0	X（1）	High-Z（2）	High-Z（2）	Shutdown

（1）X = Don ’ t care.
（2）High-Z = High Impedance.

Table 6. Receiving Truth Table

Receiving Inputs			Receiving Outputs	Mode
RE	DE	A-B	RO	
0	0	≥+0.2V	1	Normal
0	0	≤-0.2V	0	Normal
0	0	Inputs Open	1	Normal
1	0	X（1）	High-Z（2）	Shutdown

(1)X = Don ’ t care.
(2）High-Z = High Impedance



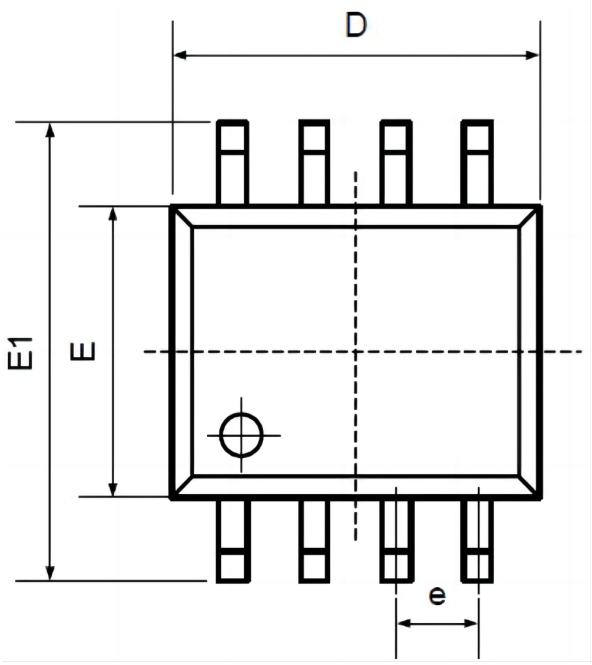
NOTES：1. RT IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE.

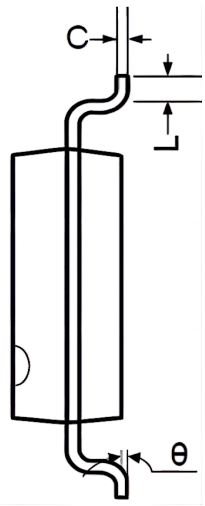
Figure 16. ADM3493 Typical Half Duplex RS-485 Network

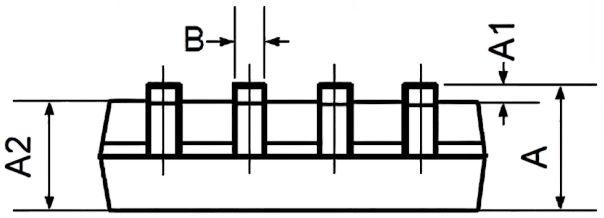
Order information

Order Number	Package	Package Quantity	Marking On The park	Temperature
ADM3493ARZ-REEL-TUDI	SOP8	Tape,Reel,4000	ADM3493ARZ	−40°C to +85°C

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Important statement:

●TUDI Semiconductor reserves the right to modify the product manual without prior notice! Before placing an order, customers need to confirm whether the obtained information is the latest version and verify the completeness of the relevant information.

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