MOSFET

Metal Oxide Semiconductor Field Effect Transistor

OptiMOS™

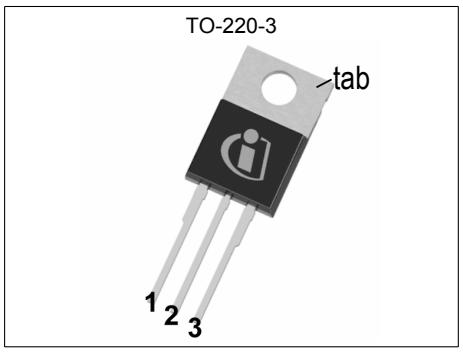
OptiMOS™ Power-Transistor, 60 V
IPP029N06N

Data Sheet

Rev. 2.6
Final

Power Management & Multimarket

1 Description



Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

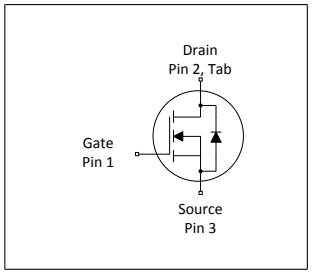


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	2.9	mΩ
I_D	100	A
Q_{OSS}	65	nC
Q_G(0V..10V)	56	nC

Type / Ordering Code	Package	Marking	Related Links
IPP029N06N	PG-TO220-3	029N06N	-

[1] J-STD20 and JESD22

Table of Contents

Description 2
Maximum ratings 4
Thermal characteristics 4
Electrical characteristics 5
Electrical characteristics diagrams 7
Package Outlines 11
Revision History 12
Disclaimer 12

2 Maximum ratings

at T_j = 25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - -	- - -	100 100 24	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_C=25 °C, R_{thJA} =50K/W
Pulsed drain current[1]	$I_{D,pulse}$	-	-	400	A	T_C=25 °C
Avalanche energy, single pulse[2]	E_{AS}	-	-	110	mJ	I_D=100 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	136 3.0	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 K/W
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.7	1.1	K/W	-
Device on PCB, minimal footprint	R_{thJA}	-	-	62	K/W	-
Device on PCB, 6 cm² cooling area[3]	R_{thJA}	-	-	40	K/W	-
Soldering temperature, wave and reflow soldering are allowed	T_{sold}	-	-	260	°C	Reflow MSL1

[1] See figure 3 for more detailed information
[2] See figure 13 for more detailed information
[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

4 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	V_{DS}=V_{GS}, I_D=75 µA
Zero gate voltage drain current	I_{DSS}	- -	0.5 10	1 100	µA	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	2.7 3.3	2.9 4.4	mΩ	V_{GS}=10 V, I_D=100 A V_{GS}=6 V, I_D=25 A
Gate resistance[1)]	R_G	0.65	1.3	1.95	Ω	-
Transconductance	g_{fs}	80	160	-	S	|V_{DS}|>2|I_D|$R_{DS(on)max}$, I_D=100 A

Table 5 Dynamic characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4100	5125	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Output capacitance	C_{oss}	-	980	1225	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	39	78	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	17	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$,ext=3 Ω
Rise time	t_r	-	15	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$,ext=3 Ω
Turn-off delay time	$t_{d(off)}$	-	30	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$,ext=3 Ω
Fall time	t_f	-	8	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$,ext=3 Ω

[1)] Defined by design. Not subject to production test

Table 6 Gate charge characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	20	-	nC	V_{DD}=30 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	11	-	nC	V_{DD}=30 V, I_D=100 A, V_{GS}=0 to 10 V
Gate to drain charge[2)]	Q_{gd}	-	11	15	nC	V_{DD}=30 V, I_D=100 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	19	-	nC	V_{DD}=30 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge total[2)]	Q_g	-	56	66	nC	V_{DD}=30 V, I_D=100 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.8	-	V	V_{DD}=30 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	49	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[2)]	Q_{oss}	-	65	82	nC	V_{DD}=30 V, V_{GS}=0 V

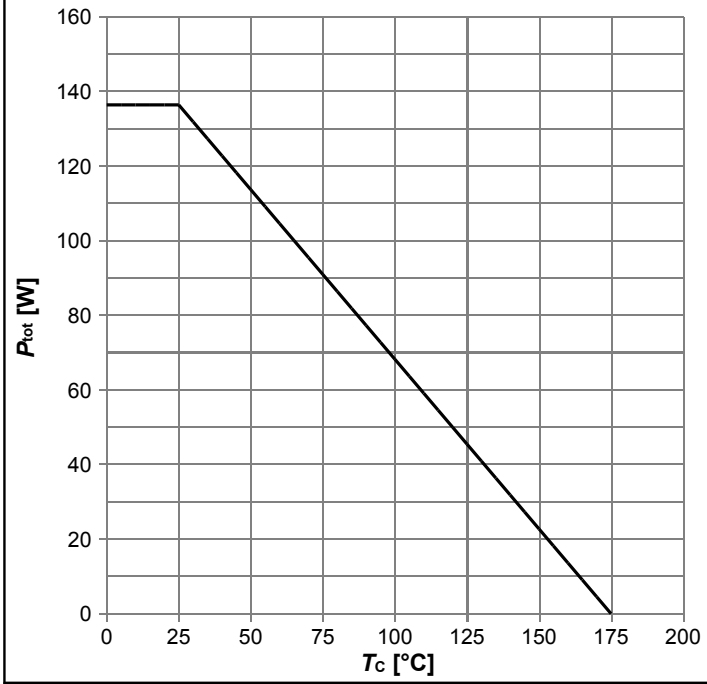
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	120	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	480	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	1.0	1.2	V	V_{GS}=0 V, I_F=100 A, T_j=25 °C
Reverse recovery time[2)]	t_{rr}	-	54	86	ns	V_R=30 V, I_F=100 A, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}	-	77	-	nC	V_R=30 V, I_F=100 A, di_F/dt=100 A/µs

[1)] See ″Gate charge waveforms″ for parameter definition
[2)] Defined by design. Not subject to production test

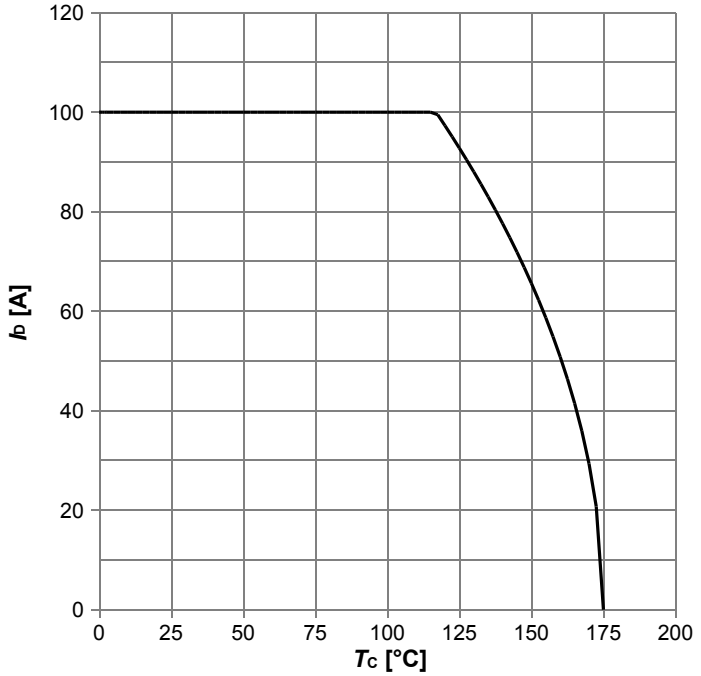
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



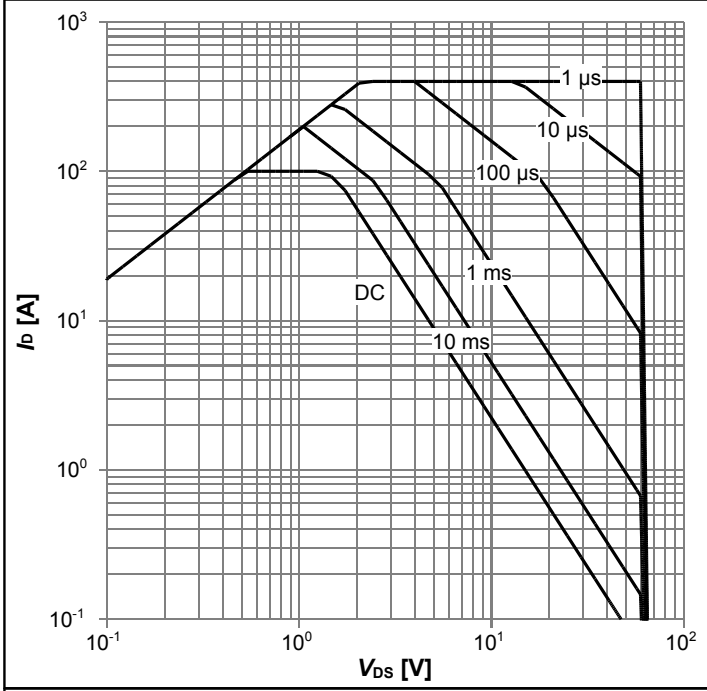
$P_{tot}=f(T_C)$

Diagram 2: Drain current



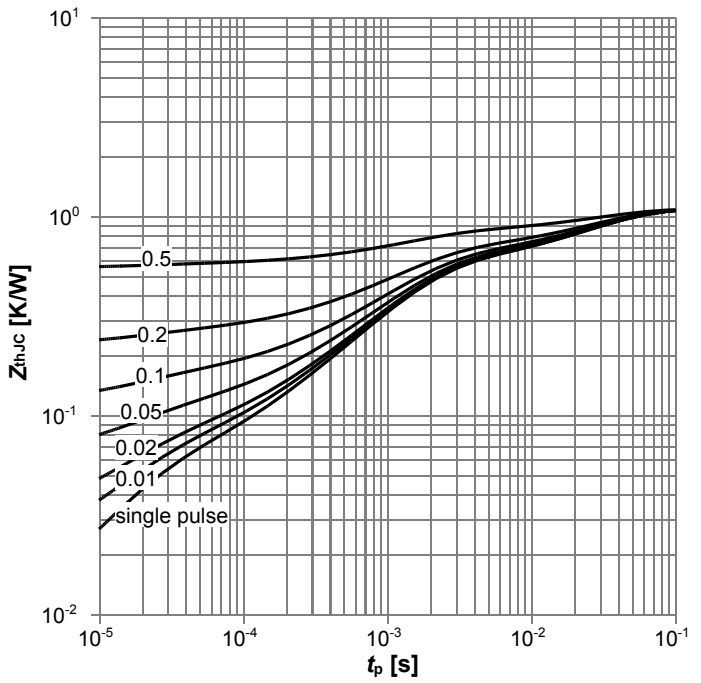
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



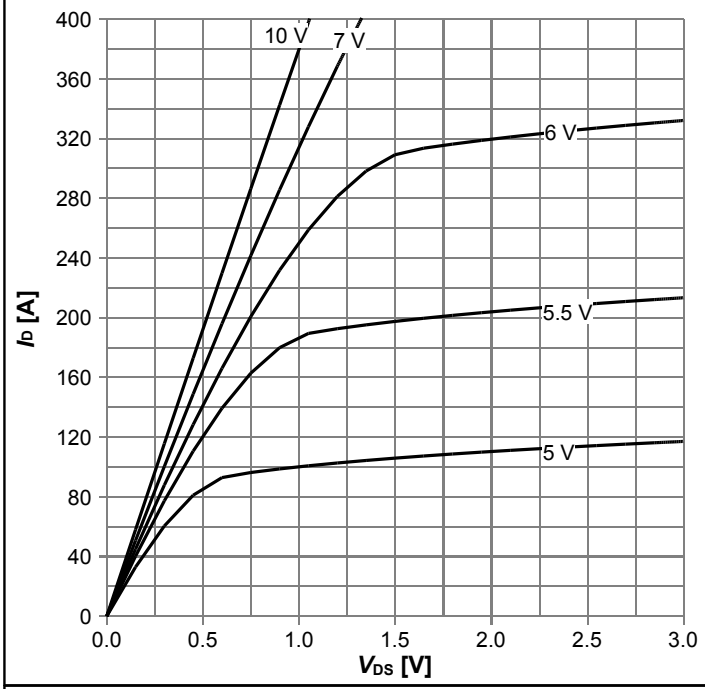
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



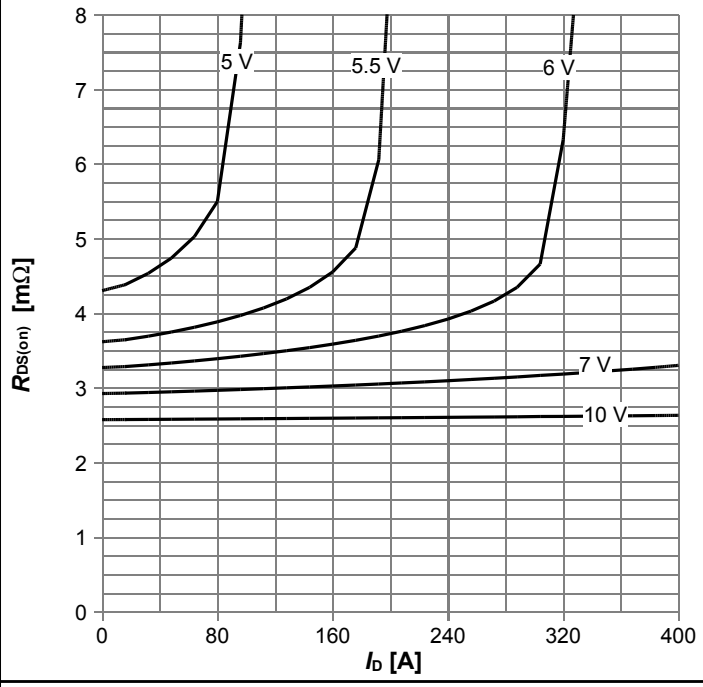
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



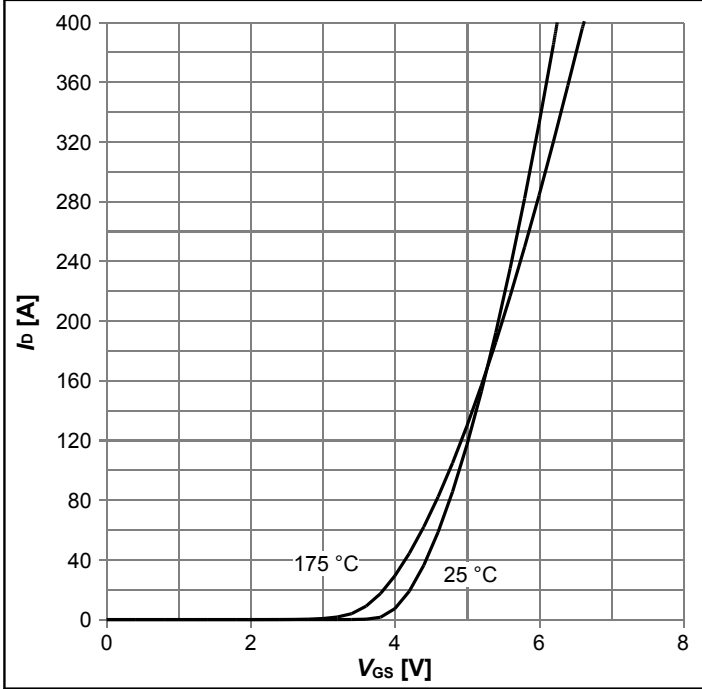
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



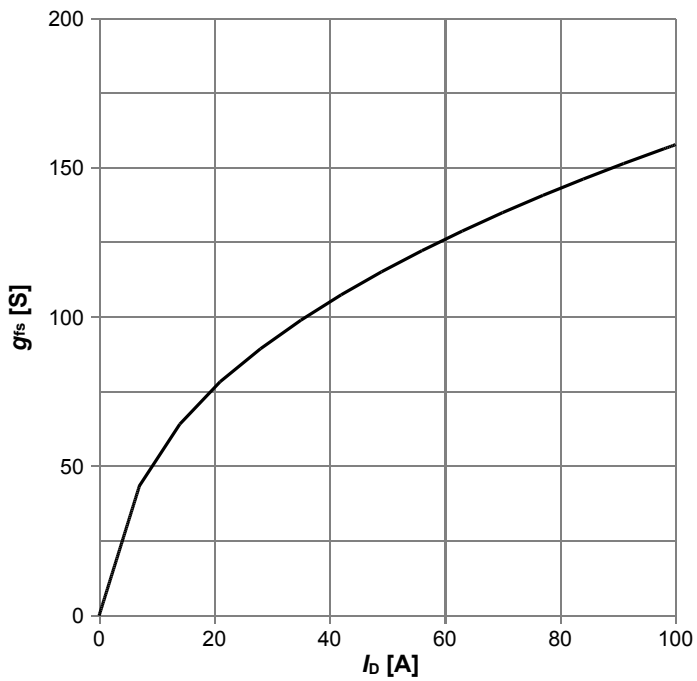
$R_{DS(on)}=f(I_D)$; $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



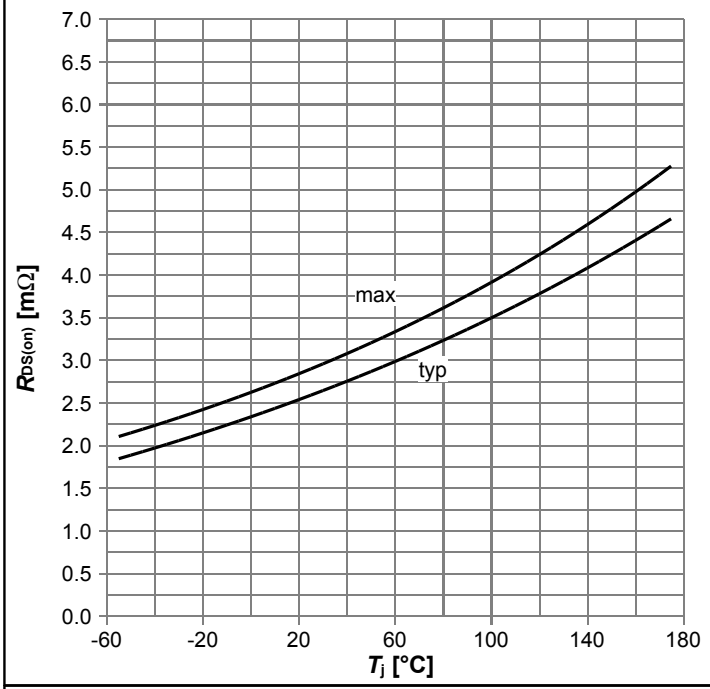
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



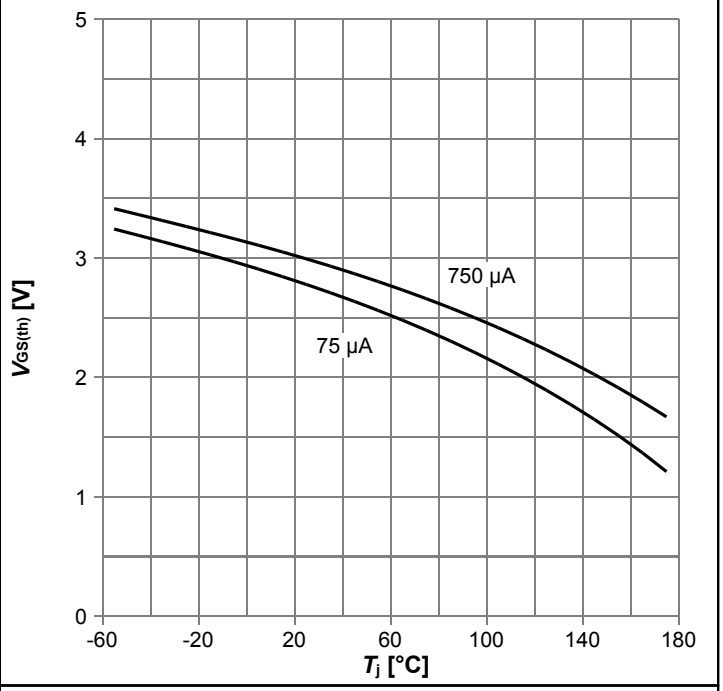
$g_{fs}=f(I_D)$; $T_j=25$ °C

Diagram 9: Drain-source on-state resistance



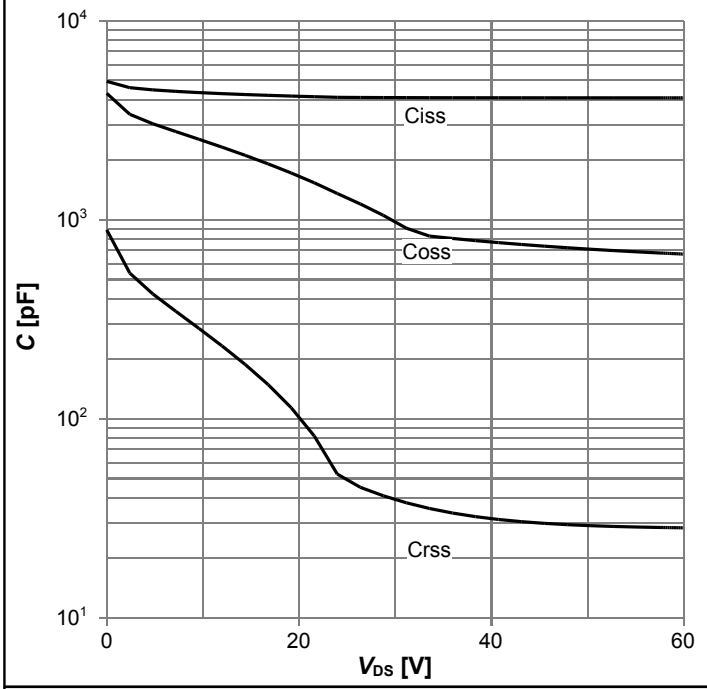
$R_{DS(on)}=f(T_j)$; $I_D=100$ A; $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



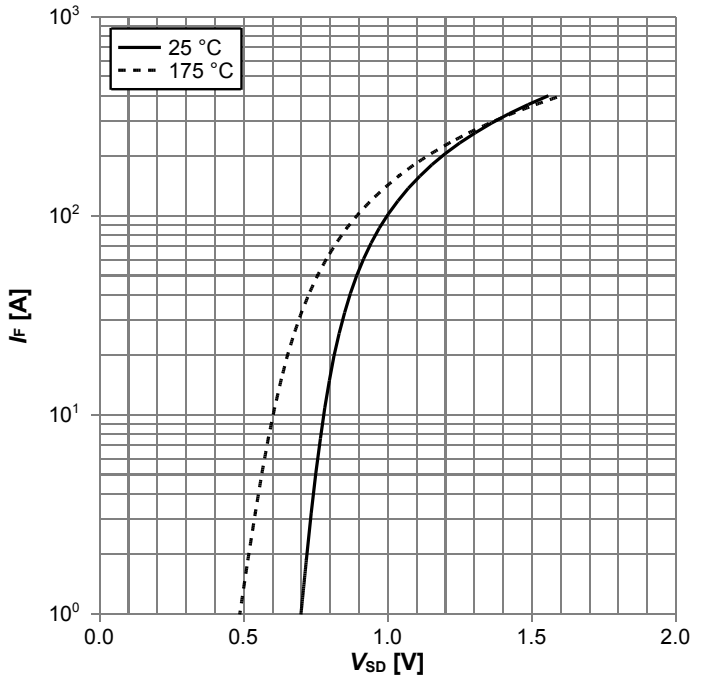
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



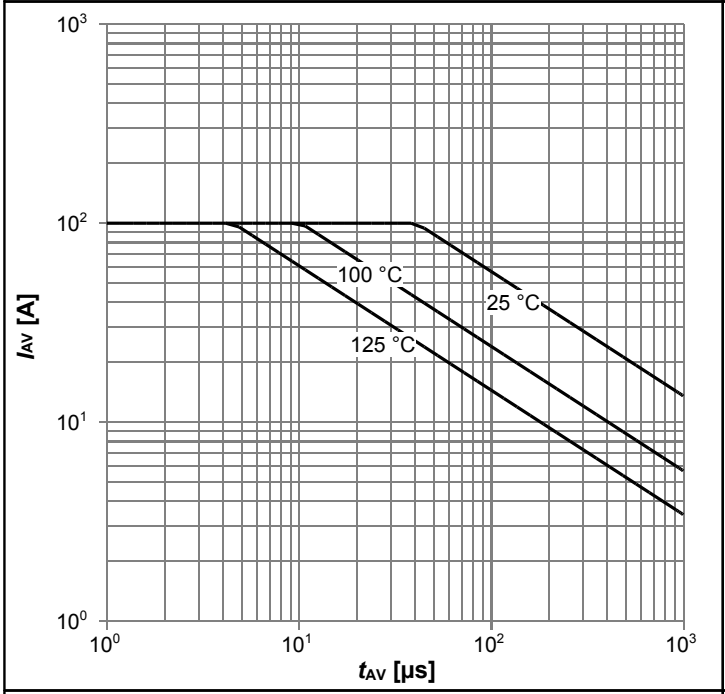
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



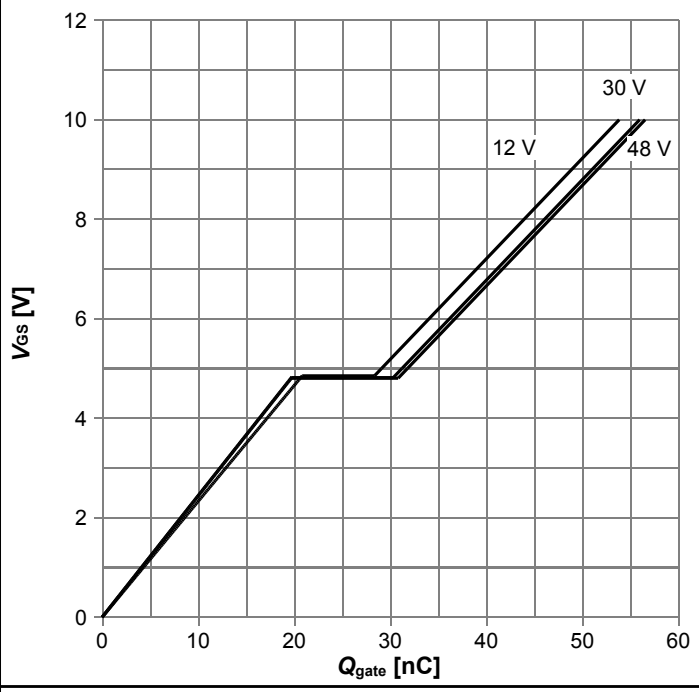
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



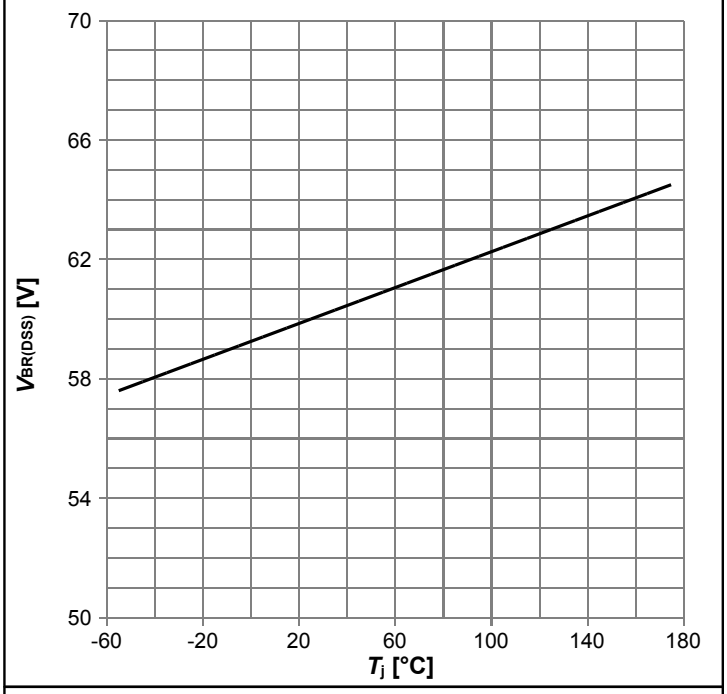
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



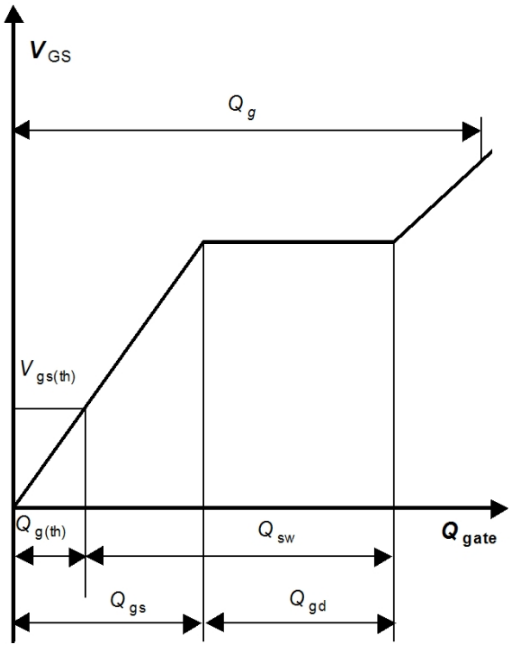
V_{GS}=f(Q_{gate}); I_D=100 A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

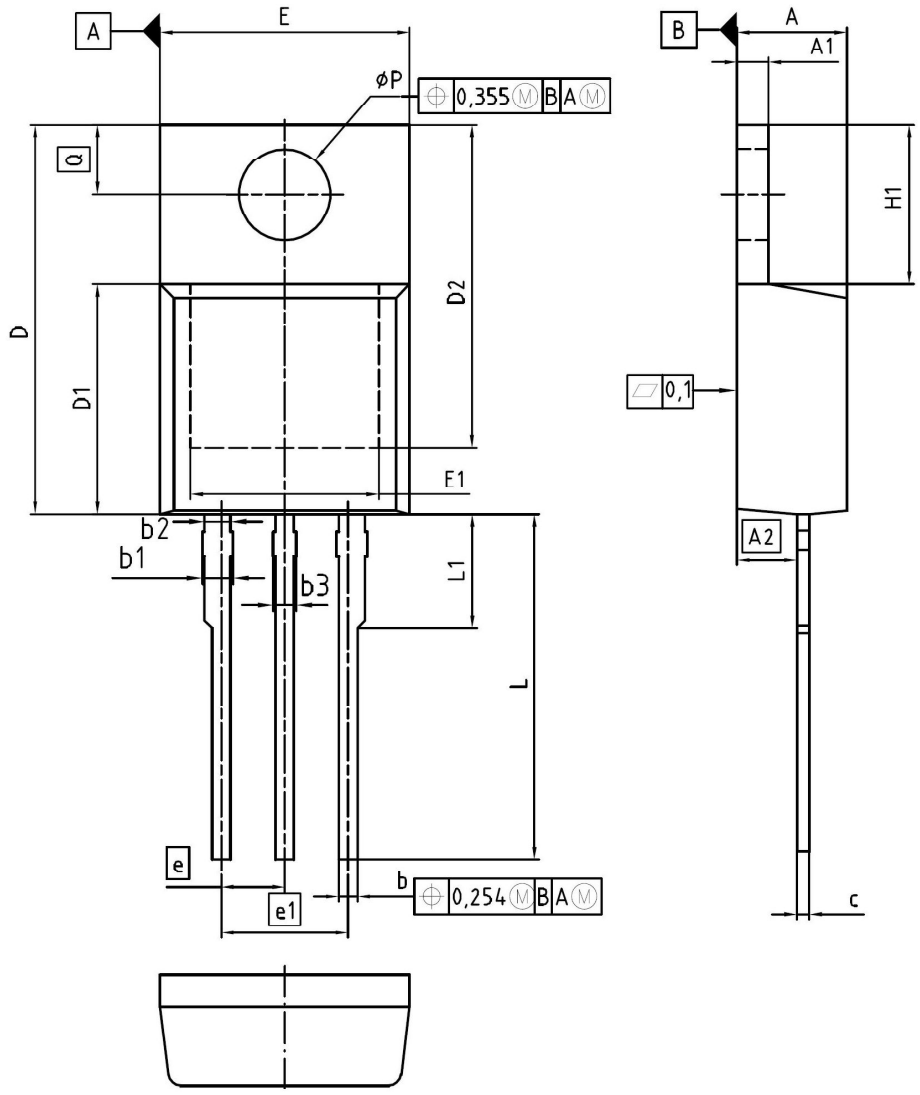


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Gate charge waveforms



6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

DOCUMENT NO.
Z8B00003318

SCALE 0 2.5 0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
30-07-2009

REVISION
06

Figure 1 Outline PG-TO220-3, dimensions in mm/inches

Revision History

IPP029N06N

Revision: 2015-02-10, Rev. 2.6

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.5	2014-07-25	Rev.2.5
2.6	2015-02-10	Insert Rg min value = 0.65 Ohm

We Listen to Your Comments
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:
erratum@infineon.com

Published by
Infineon Technologies AG
81726 München, Germany
© 2015 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information
For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

Warnings
Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.
The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Unikeyic Electronics

Global Electronic Components Distributor

Click to view pricing, inventory, delivery, and lifecycle information:

Infineon Technologies:

TLE4971A120N5E0001XUMA1 BAT5405WH6327XTSA1 FS100R12KT4GPBPSA1 IPB320P10LMATMA1 BSC320N20NS3 G BTS 5210 G FS75R12KE3B9BOSA1 TLS208D1EJV33XUMA1 ISZ75DP15LMATMA1 AIMW120R060M1HXKSA1 CY8C24894-24LTXI XMC4800F144K1024AAXQMA1 IPL60R185C7AUMA1 TLE493DW2B6A0HTSA1 BGM781N11E6327XUSA1 BSZ050N03LSGATMA1 BTS70302EPADAUGHBRDTOBO1 EVALPMG1B1DRPTOBO1 IKD10N60RFATMA1 IPD60R650CEAUMA1 CY8C29466-24PVXI FP150R12N3T4PB81BPSA1 IGCM10F60GAXKMA1 IM241S6S1BAUMA1 IPT014N08NM5ATMA1 IRF3710PBF SPP06N80C3 TC1782F320F180HRBAKXUMA2 TLF80511TCATMA2 2EDS8265HXUMA2