Datasheet

DS000556

AS73211

XYZ True Color Sensor with I²C Interface

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Content Guide

1 General Description 3
1.1 Key Benefits & Features 4
1.2 Applications 4
1.3 Block Diagram 4
2 Ordering Information 6
3 Pin Assignment 7
3.1 Pin Diagram 7
3.2 Pin Description 8
4 Absolute Maximum Ratings 9
5 Electrical Characteristics 10
6 Typical Optical Characteristics .. 13
7 Functional Description 14
7.1 Operational States 14
7.2 Configuration State 14
7.3 Measurement State 14
7.4 Measurement Modes 15
7.5 Continuous Measurement Mode – CONT .. 16
7.6 Command Measurement Mode – CMD 17
7.7 Synchronous Measurement Mode – SYNS 19
7.8 Synchronous Measurement Start and End Mode – SYND 20
7.9 Energy Saving Options 21
7.10 Power Down 21
7.11 Standby 23
7.12 Examples 24
7.13 Transfer Function 28
7.14 Divider 37
7.15 Conversion Time Measurement in SYND Mode 38
7.16 Temperature Measurement 39
7.17 I²C Communication 39
7.18 I²C Write Protocol 41
7.19 I²C Read Protocol 41
7.20 I²C Addressable Register Space 42
7.21 I²C General Procedure to start with the AS73211 43
8 Register Description 44
8.1 Register Overview 44
8.2 Operational State Register – OSR 44
8.3 API Generation Register – AGEN 46
8.4 Configuration Register - CREG1, CREG2 and CREG3 47
8.5 Register – BREAK 51
8.6 Register – EDGES 51
8.7 Register – OPTREG 51
8.8 Output Register Bank 52
9 Application Information 56
9.1 Schematic 56
9.2 External Components 56
9.3 PCB Layout 57
10 Package Drawings 58
11 Tape & Reel Information 59
12 Soldering & Storage Information 60
13 Application Notes 61
13.1 Narrowband Luminous Sources 61
13.2 Angle of Incidence 61
13.3 Effects of Temperature 61
13.4 Notes for Manufacturing 61
13.5 Sensor Calibration 62
14 Revision Information 64
15 Legal Information 65

1 General Description

The AS73211 is a low power, low noise integrated color sensor. Three channels convert light signals via photodiodes to a digital result and realize a continuous or triggered measurement. In front of the three photodiodes there are optical filter mounted for X-, Y- and Z-signals respectively. The irradiance responsivity can be set in a range of 12 steps by a factor of two for each step. The conversion time is internally controlled over a wide range of 15 steps by a factor of two for each step. With the input pin (SYN) the conversion time can be externally controlled to adapt the measurement to the given environment and time base.

With its irradiance responsivity factor and conversion time the AS73211 supports an overall huge dynamic range up to 3.43E+10 (resolution multiplied by gain range). It achieves an accuracy of up to 24-bit signal resolution (internal via I²C and shifter 16 bit) with an irradiance responsivity per count down to 0.5pW/cm².

$$Dynamic\ Range = \frac{MAX\ measureable\ value\ = Max.Full\ Scale\ Range}{MIN\ measureable\ value = Min.Least\ Significant\ Bit}$$

For high robustness at high sensitivity, the AS73211 has an inherent ripple rejection of the 50Hz / 60Hz external disturbances. Automatic Power Down (sleep function) between subsequent measurements offers operation with very low current consumption. Further, a synchronized mode and other control modes adjustable by user programming can be used. The supported operating modes of the AS73211 are:

- CMD Mode – single measurement and conversion (controlled via I²C interface),
- CONT Mode – continuous measurement and conversion (periodically recurring measuring cycles) start and stop controlled via I²C interface,
- SYN[x] Modes - synchronized measurement and conversion:
  - [SYNS Mode] synchronization of start via control signal at pin SYN,
  - [SYND Mode] synchronization of start and stop of measuring cycles via control signal at pin SYN.

The conversion data is accessed by the I²C interface with programmable slave addresses via 16-bit / 400 kHz fast mode. The measurement of the actual conversion time for an external triggered measurement can be performed. The measurement modes will not affect the settings of the irradiance responsivity and conversion time. Further, the converter supports functions like Power Down and Standby, therefore it is suitable for mobile applications. Based on the high flexibility the AS73211 is suitable as an optical converter for three different wave-lengths. The device achieves a high dynamic range in back light applications and in the measurements of integral intensity of pulsed light. That makes the color sensors excellently suited for photometry applications (brightness, color coordinate and/or color temperature), for determining current values for control of spectrally mixed LED light sources or as sensors for display and (back)light calibration and mobile devices for light measurement. The AS73211 contains an integrated temperature sensor for rough compensation of the thermic behavior of light sources. The device is available in a small SMD package.

1.1 Key Benefits & Features

The benefits and features of AS73211, XYZ True Color Sensor with I²C Interface, are listed below:

Figure 1:
Added Value of Using AS73211

Benefits	Features
Light control measurement based on CIE 1931/DIN 5033	JENCOLOR® interference filter technology
Brightness, color coordinate and/or color temperature control	High dynamic range up to 3.43E+10 (16 .24 Bit ADC)
Usable under poor lighting conditions	High sensitivity up to 2.1M counts/(µW/cm²) Smallest LSB 0.5pW/cm²
Mobile applications	Low power operation, Power on Reset, Power down and standby, small QFN package
Harsh environmental applications	-40°C up to 125°C operation temperature range
Temperature compensation	On-chip temperature sensor

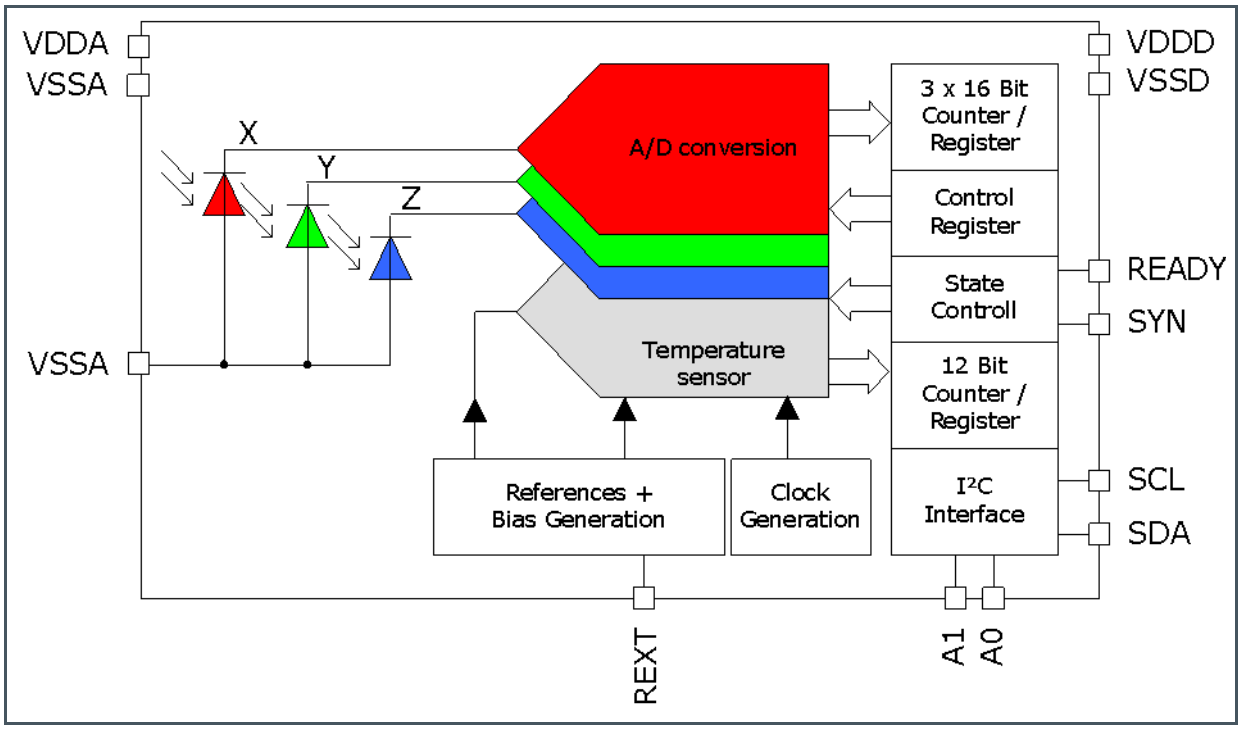
1.2 Applications

- LED lighting control management for solid-state lighting applications (SSL)
- Cabin lighting, daylight management / Human and Color Centric Lighting (HCL and CCL)
- Ambient light color detection / correction
- (O)LED display aging compensation and dynamic display color balancing
- Portable light color measurement
- Digital light projection (DLP)
- Printer, Smartphone, PDA, tablet PCs, LCD-TVs, digital picture, frames, digital cameras color enhancement
- Photometry (brightness, color coordinate and/or color temperature)

1.3 Block Diagram

Figure 2 shows the main components of the AS73211. The photodiodes convert the incoming light to a photo current and with subsequent current-to-digital converter to digital data. An internal reference generator provides all necessary references for the A/D conversion and the photodiodes by using an external resistor R_{EXT} at pin REXT. The results of the A/D conversion are stored in three 16-bit registers and can be accessed via I²C interface. For the externally triggered start or start and stop of the measurement, the input pin SYN can be used. The output READY reflects the status of the conversion. The internal temperature sensor delivers the on-chip temperature, stored as 12-bit value in a 16-bit register, which can be accessed via I²C interface, too. The pins A0 and A1 set the I²C slave address. Separated analog and digital power supply and ground pins reduces noise coupling.

Figure 2:
Functional Blocks of AS73211



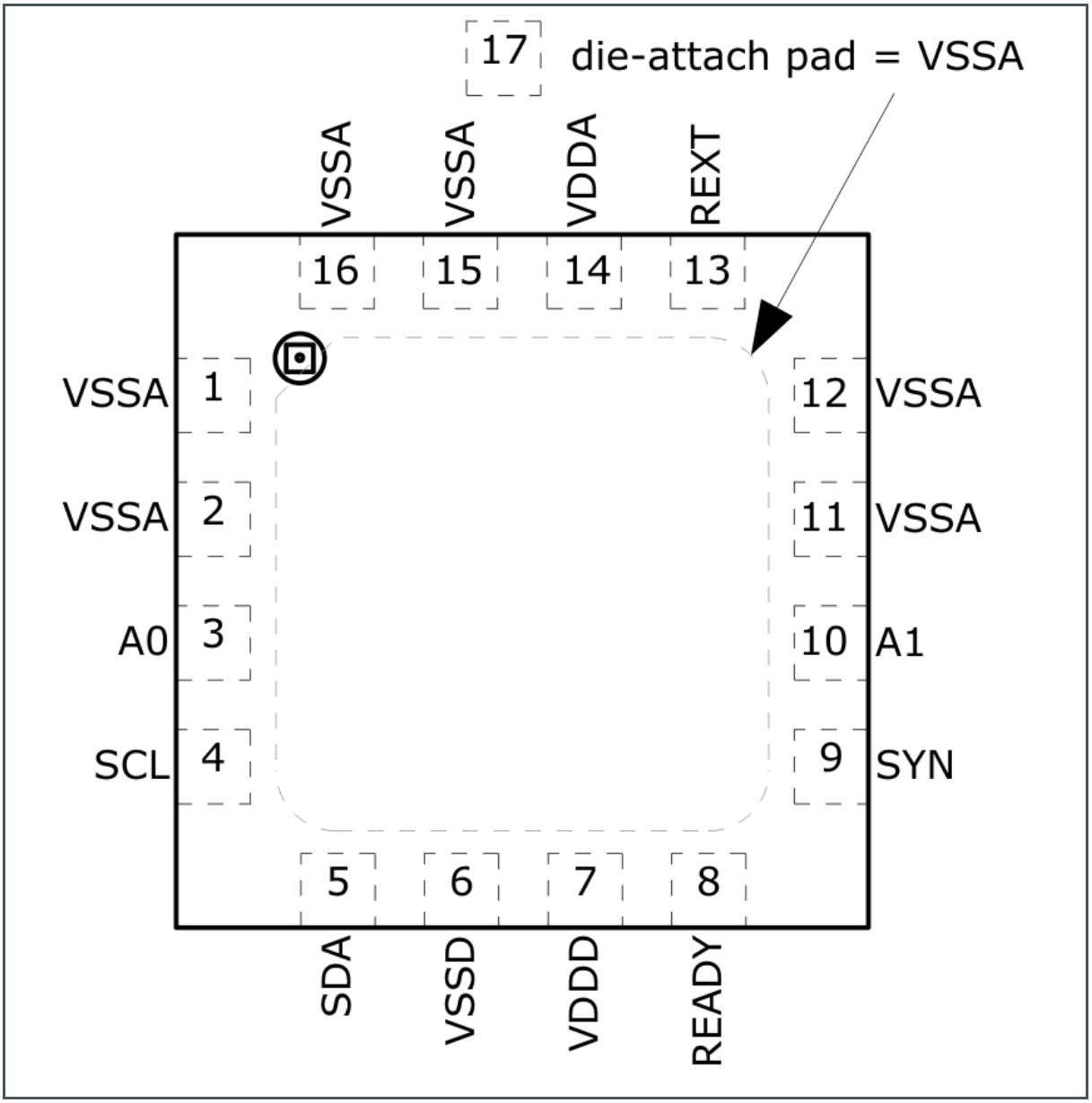
2 Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS73211-AQFM	QFN16	AS73211	Tape & Reel	500pcs/reel
AS73211-AQFT	QFN16	AS73211	Tape & Reel	3000pcs/reel

3 Pin Assignment

3.1 Pin Diagram

Figure 3:
Pin Diagram of AS73211 in QFN16 Package (top view)



3.2 Pin Description

Figure 4:
Pin Description of AS73211

Pin Number	Pin Name	Pin Type (1)	Description
1 - 2	VSSA	P	Analog ground
3	A0	DI	Variable I²C slave address bit 0
4	SCL	DI	I²C clock input
5	SDA	D_I/O_OD	I²C data input / output; open drain output stage
6	VSSD	P	Digital ground
7	VDDD	P	Digital power supply
8	READY	DO	Conversion status; configurable as push pull or open drain output stage (default push pull)
9	SYN	DI	Input for external controlled conversion
10	A1	DI	Variable I²C slave address bit 1
11 – 12	VSSA	P	Analog ground
13	REXT	A_I/O	External reference resistor
14	VDDA	P	Analog power supply
15 – 17	VSSA	P	Analog ground

(1) Explanation of abbreviations:

DI	Digital input
DO	Digital output
D_I/O_OD	Digital input / output open drain
P	Power pin
A_I/O	Analog

4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings“ may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings of AS73211

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
V_{DD}	Power Supply Voltage	-0.5	5.0	V	VDDA and VDDD
$DIFF_{VDD}$	Supply Voltage Difference	-0.3	0.3	V	VDDD-VDDA
	Input and Output Voltages	-0.5	V_{DD}+0.5	V	A0, A1, SCL, SDA, SYN, READY
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM		± 500	V	JS-001-2014
ESD_{CDM}	Electrostatic Discharge CDM		± 500	V	JEDEC JESD22-C101F Oct 2013
Temperature Ranges and Storage Conditions					
T_A	Operating Ambient Temperature	-40	125	°C	
T_{STRG}	Storage Temperature Range	-55	125	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020 (1)
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level		3		Maximum floor life time of 168h

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100 % Sn)

5 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. All voltages with respect to ground (GND). Device parameter are guaranteed at V_{DD}=3.3V and T_A=25°C unless otherwise noted.

Figure 6:
Electrical Characteristics of AS73211

Symbol	Description	Condition	Min	Typ	Max	Unit
T_{OP}	Operating Temperature		-40		125	°C
V_{DD}	Power Supply Voltage	VDDA and VDDD	2.7	3.3	3.6	V
$DIFF_{VDD}$	Supply Voltage Difference	VDDD-VDDA	-0.3	0	0.3	V
R_{EXT}	External Resistor at Pin REXT	R_{EXT} (TC_{REXT} ≤ 50ppm/K)	3.267	3.3	3.333	MΩ
I_{VDD}	Current Consumption	Active mode during measurement		1.5	2	mA
I_{VDDSB}	Standby Current Consumption	Standby state			800	µA
I_{VDDPD}	Power Down Current Consumption	Power down state			1	µA
VIH	Input High Level	A0, A1, SCL, SYN	0.7			VDDD
VIL	Input Low Level	A0, A1, SCL, SYN			0.3	VDDD
VOH	Output High Level	READY IOHL ≤ 3mA	0.8			VDDD
VOL	Output Low Level	SDA, READY IOHL ≤ 4mA			0.4	V
		SDA, READY IOHL ≤ 4mA			0.6	V
IOHL	Output Drive Strength	Concerning to VOH and VOL		3	6	mA
I_{ILEAK}	Input Leakage Current	VSSD ≤ VIN ≤ VDDD	-10		10	µA
f_{CLKMIN}	Min. Internal Clock Frequency	CREG3:CCLK = 00b	0.75	1	1.3	MHz
f_{CLKMAX}	Max. Internal Clock Frequency	CREG3:CCLK = 11b	6	8.2	10	MHz
$T_{STARTSB}$	Startup Time after Standby state	Until start of first measurement		4	5	µs
$T_{STARTPD}$	Startup Time after Power Down state	Until start of first measurement		1.2	2	ms
T_{SYNDEL}	SYN Trigger Delay	From falling SYN-edge to start of measurement			3	$1/f_{CLK}$
T_{SYN}	SYN Negative or Positive Pulse Width	SYN recognized as start or end pulse of measurement	3			$1/f_{CLK}$
T_abs_err	Temperature Absolute Error		-10		10	K

Figure 7:
I²C Slave Timing Characteristics of AS73211

Symbol	Description	Condition	Min	Typ	Max	Unit
f_{SCL}	I²C Clock Frequency at SCL	R_{PULLUP} ≥ 820Ω $CL_{(SCL, SDA)}$ ≤ 400pF			400	kHz
t_{HIGH}	SCL High Pulse Width		0.6			µs
t_{LOW}	SCL Low Pulse Width		1.3			µs
t_R	SCL and SDA Rise Time				0.3	µs
t_F	SCL and SDA Fall Time				0.3	µs
$t_{HD;STA}$	Hold Time Start Condition		0.6			µs
$t_{SU;SDA}$	Setup Time Start Condition		0.6			µs
$t_{HD;DATM}$	SDA Data Hold Time (Master)	Data transfer from master to slave	0.02			µs
$t_{HD;DATS}$	SDA Data Hold Time (Slave)	Data transfer from slave to master	0.3		0.9	µs
$t_{SU;DAT}$	Data Setup Time		0.1			µs
$t_{SU;STO}$	Setup Time Stop Condition		0.6			µs
t_{BUF}	Bus Free Time between a Stop and a Start Condition		1.3			µs

Figure 8:
I²C Slave Timing Diagram

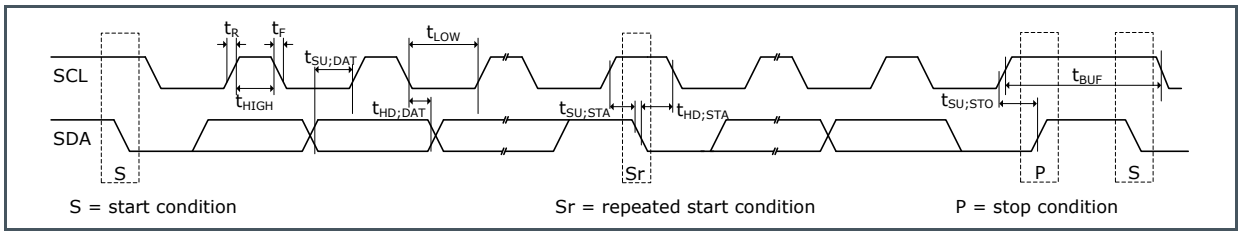


Figure 9:
ADC Specification of AS73211

Symbol	Description	Condition	Min	Typ	Max	Unit
RES	ADC Resolution		10		24	bit
T_{CONV}	Conversion Time	CREG3:CCLK = 00b f_{CLKMIN}	1		16384	ms
		CREG3:CCLK = 11b f_{CLKMAX}	0.125		2048	ms
ΔT_{CONV}	Conversion Time Tolerance	Related to f_{CLK}	-25		25	%
INL	Integral Nonlinearity		-0.02		0.02	%
DNL	Differential Nonlinearity	No missing codes	-0.5		0.5	LSB
D_{FSR}	Full Scale ADC Code	Per channel	1024		65535	counts

Symbol	Description	Condition	Min	Typ	Max	Unit
D_{DARK}	Dark ADC Count Value	E_e = 0; GAIN = 2048x T_{CONV} = 64ms @ f_{CLKMIN};			8	counts
ENOB	Effective Number of Bits	GAIN = 64x T_{CONV} = 64ms @ f_{CLKMIN};		15.4		bit

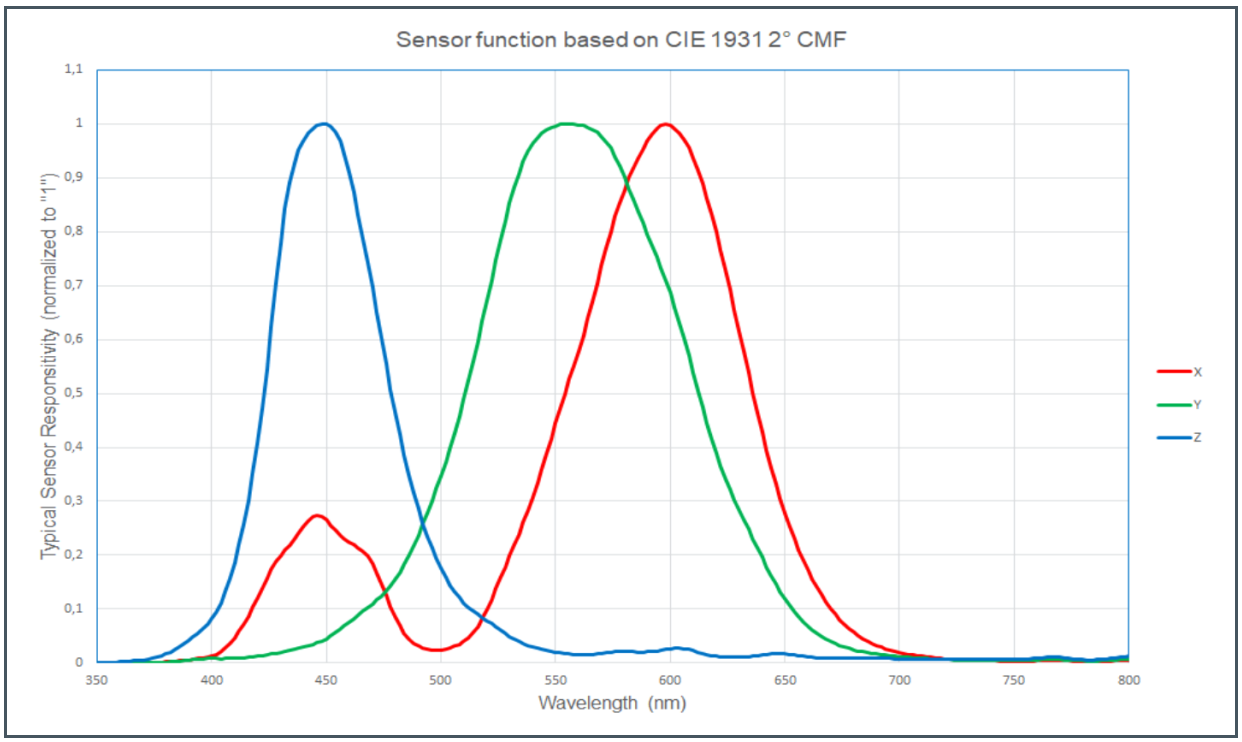
Figure 10:
Optical Characteristics of AS73211

Symbol	Description	Condition	Min	Typ	Max	Unit
$Re_{GAIN2048}$	Irradiance Responsivity for CREG1:GAIN = 2048x	X channel λ = 600nm		4730		counts/ (µW/cm²)
		Y channel λ = 555nm		4392		
		Z channel λ = 445nm		8179		
Re_{GAIN1}	Irradiance Responsivity for CREG1:GAIN = 1x	X channel λ = 600nm		2.309		counts/ (µW/cm²)
		Y channel λ = 555nm		2.145		
		Z channel λ = 445nm		3.994		
$FSR_{GAIN2048}$	Full Scale Range of detectable Irradiance for CREG1:GAIN = 2048x	X channel λ = 600nm		13.854		µW/cm²
		Y channel λ = 555nm		14.919		
		Z channel λ = 445nm		8.012		
FSR_{GAIN1}	Full Scale Range of detectable Irradiance for CREG1:GAIN = 1x	X channel λ = 600nm		28372		µW/cm²
		Y channel λ = 555nm		30554		
		Z channel λ = 445nm		16408		

6 Typical Optical Characteristics

The filter response curves based on the CIE 1931 standard are shown in the figure below.

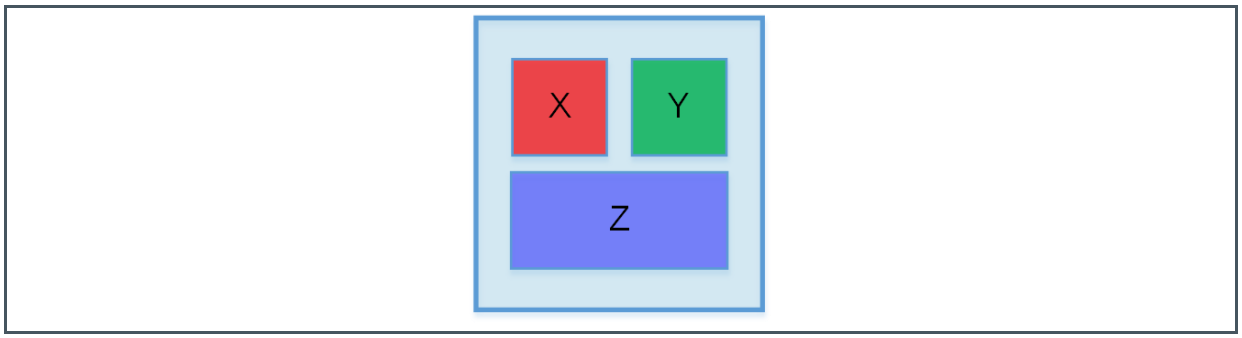
Figure 11:
Typical Spectral Sensitivity of XYZ True Color Sensor AS73211



(1) Typical characteristic sensitivity. Spectral tolerance filter curve Δλ(λ) typ. <±1%*λ determined by the deviation between the filter curve's centroid wavelength and the CIE 1931 2° Standard Observer centroid wavelength.

(2) See chapter 13.2 Angle of Incidence

Figure 12:
Photodiode Array



7 Functional Description

Three internal photodiodes with different spectral sensitivity with three A/D converters. The irradiance responsivity Re and the time of conversion TCONV are user defined and determined by registers CREG1:GAIN and CREG1:TIME and should be adapted to the application of interest. At the end of each conversion, the digital equivalents of the filtered input light signal regarding to the sensors area are stored in the output registers (MRES1 … MRES3). Additionally a temperature sensor works in parallel to the three optical channels, delivering the on-chip temperature at the end of conversion. The pin READY remains at low logic level all the time during the conversion. The rising edge and the following high logic level of READY signalize the end of conversion. Internal information related to the conversion is available in a status register, too.

7.1 Operational States

The AS73211 operates in two different states “**Configuration**” and “**Measurement**”. The three least significant bits of the Operational State Register (OSR) as Device Operational State (DOS) defined the current state. After applying the power supply voltage including power-on reset or after software reset the AS73211 stays in Power Down state. It is ready to be programmed via I²C interface. Switching off Power Down (OSR:PD set to ‚0‘) the AS73211 starts up in Configuration state (CONFIG) or in Measurement state (MMODE) according to its DOS programming.

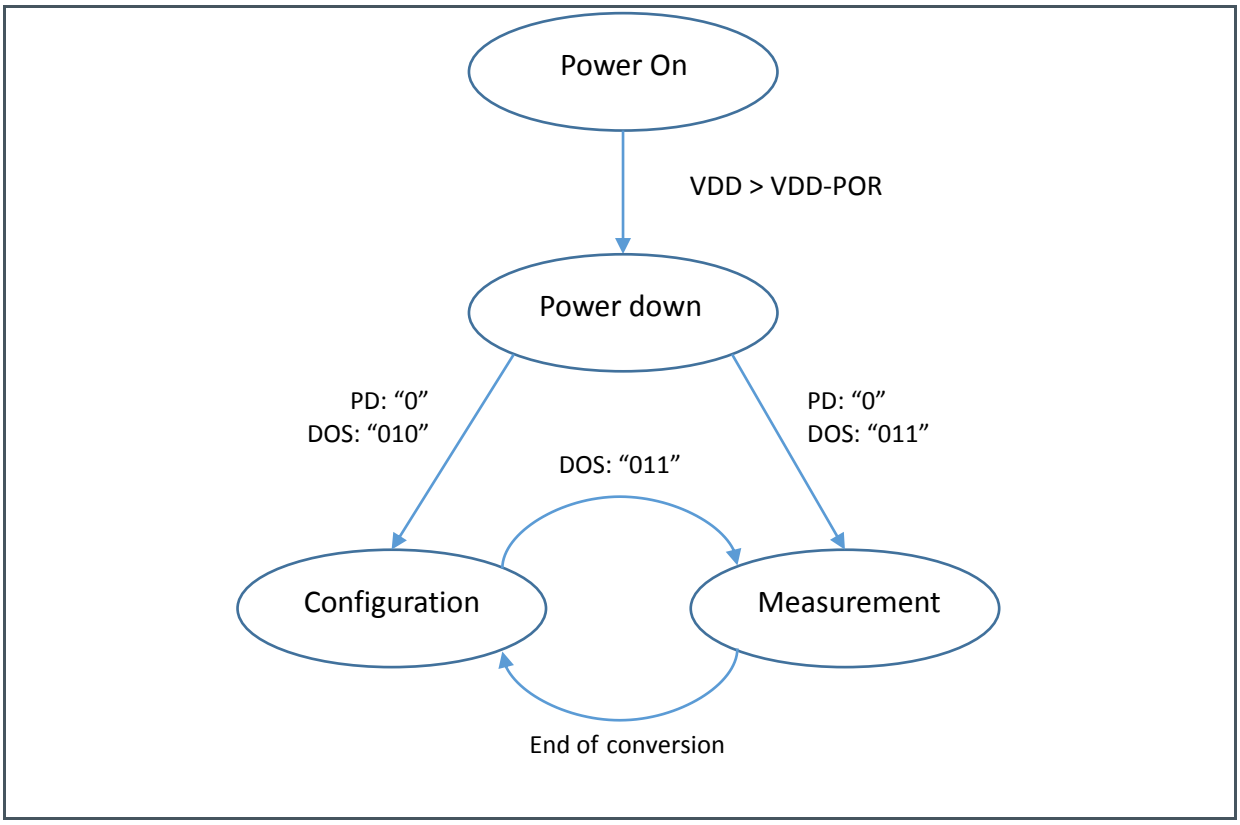
7.2 Configuration State

This state enables the access to the configuration registers (CREG1, CREG2, CREG3). Irradiance responsivity R_e and conversion time T_{CONV} can be determined by settings of registers CREG1:GAIN and CREG1:TIME as well as the kind of measurement mode can be chosen via register CREG3:MMODE. A measurement is not possible in this state and therefore no access to any measurement result registers.

7.3 Measurement State

In this state the light-to-digital conversion can be performed. The access to the output result registers is enabled, but at this time, there is no access possible to the configuration registers. Specific settings for the measuring task should be performed by programming the configuration registers before the measurement is started (see chapter 8.5). The change between Configuration and Measurement state can be performed by programming the DOS value of the operational state register OSR (see Figure 45). A change from Measurement state to Configuration state takes place immediately. Any active measurement is stopped and all output result registers and the status register are reset as well.

Figure 13:
Simplified State Diagram



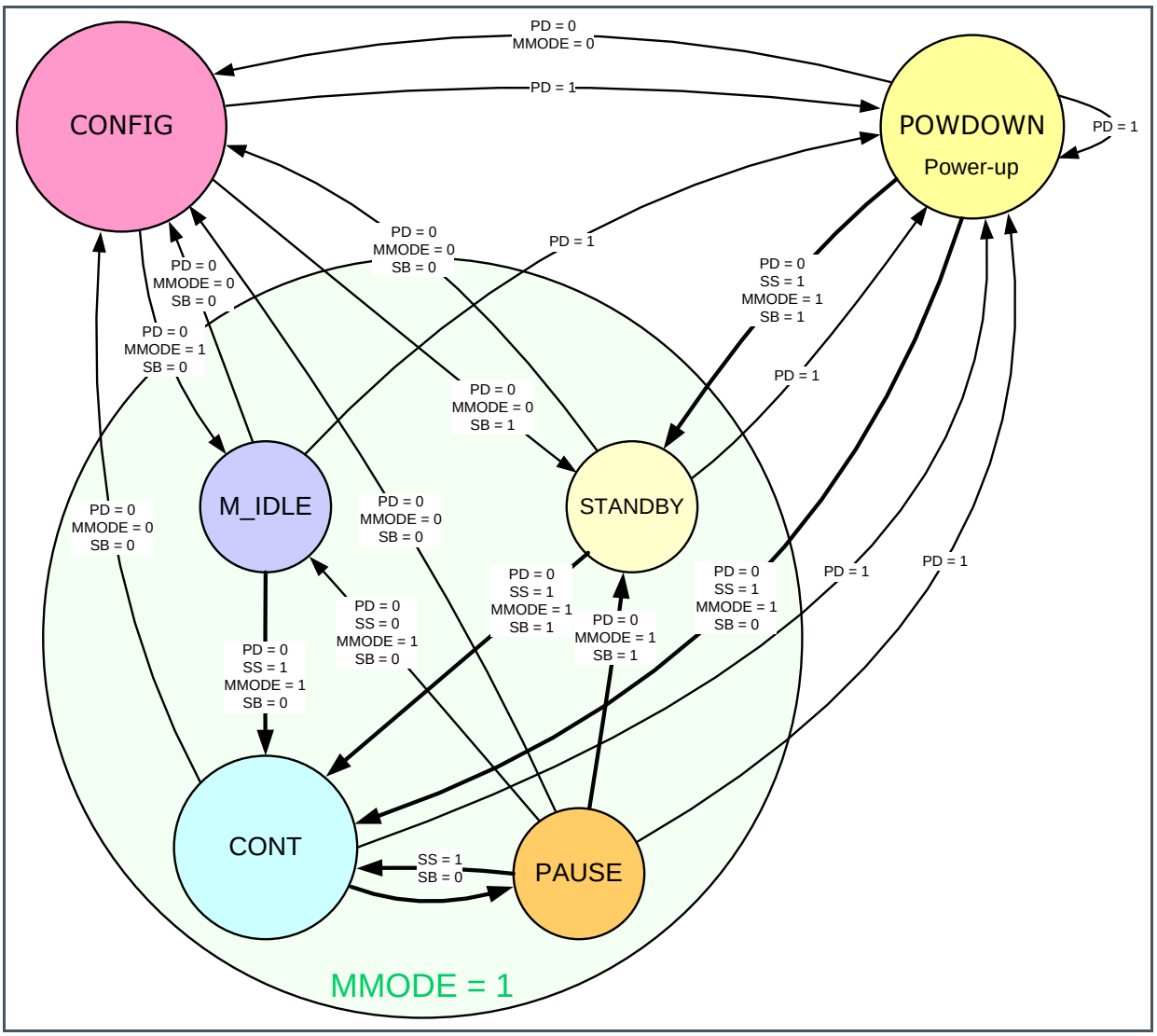
7.4 Measurement Modes

There are four different modes available to perform the measurement. The register CREG3:MMODE (see Figure 50) defines the measurement mode that is performed by the device. It is generally recommended not to communicate via I²C during the conversion. Use pause times between two conversion cycles for data transfer via I²C interface. To support such a behavior a variable pause time TBREAK is implemented (register BREAK in Figure 52), which delays the start of the next conversion cycle in the measurement modes CONT, SYNS and SYND. I²C commands sent to the AS73211 always take effect after the complete I²C write cycle with an I²C Stop condition at the end.

7.5 Continuous Measurement Mode – CONT

The A/D conversion is sequentially performed. The first conversion starts by setting the bit OSR:SS to ‚1'. If the Power Down or Standby option is switched on, the device deactivates it and initializes the continuous measurement. The measurement can only be stopped by resetting the bit OSR:SS bit.

Figure 14:
State Machine CONT Mode

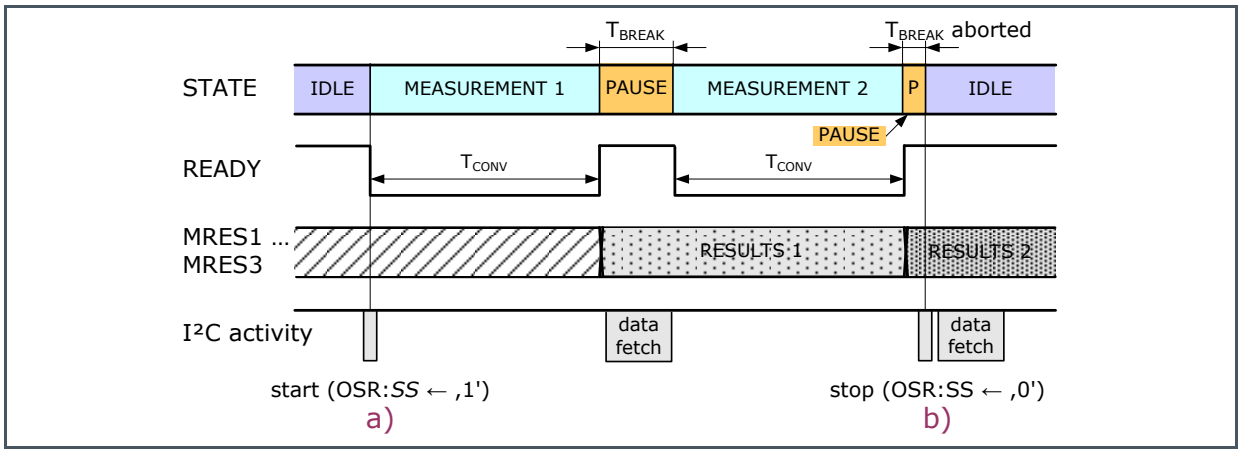


The conversion time (TCONV) is determined by the content of the register CREG1:TIME (see Figure 48). The rising edge of READY signalizes the end of each conversion and its available valid results Figure 48 shows the principle sequence for a measurement start in CONT mode, while waiting in Measurement state shows IDLE:

1. OSR programming: 83h, start of continuous measurement via OSR:SS = ‚1‘, while device is already in measurement mode (OSR:DOS = 011b),
2. OSR programming: 03h, abortion of continuous measurement via OSR:SS = ‚0‘ – here while pause time TBREAK is already activated to get the last measurement results.

It is recommended to read the measurement results during the break between two consecutive conversions. This pause time TBREAK can be configured in steps of 8µs up to 2040µs long (see Figure 52). Please note that the break time should be long enough to prevent overlapping of data fetch activities with the measurement for avoiding measurement disturbances, which could cause distortions of the measurement results

Figure 15:
Principles Sequence for a Measurement Start in CONT Mode



7.6 Command Measurement Mode – CMD

The CMD mode enables a start of a single conversion. Each conversion starts by setting the bit OSR:SS to ‚1‘. The conversion time (TCONV) is determined by the content of the register CREG1:TIME (see Figure 48). Figure 16 shows the first measurement starting from the Configuration state by setting the bits of the Device Operational State (OSR:DOS) and Start/Stop (OSR:SS) at the same time with OSR = 83h. For the next measurement start OSR = 80h is set (only bit OSR:SS, OSR:DOS = 000b corresponds to NOP – no operation, see also Figure 45.

The rising edge of READY signalizes the end of conversion and its valid output data can be read via the I²C interface (data fetch).

Figure 16:
State Machine CMD Mode

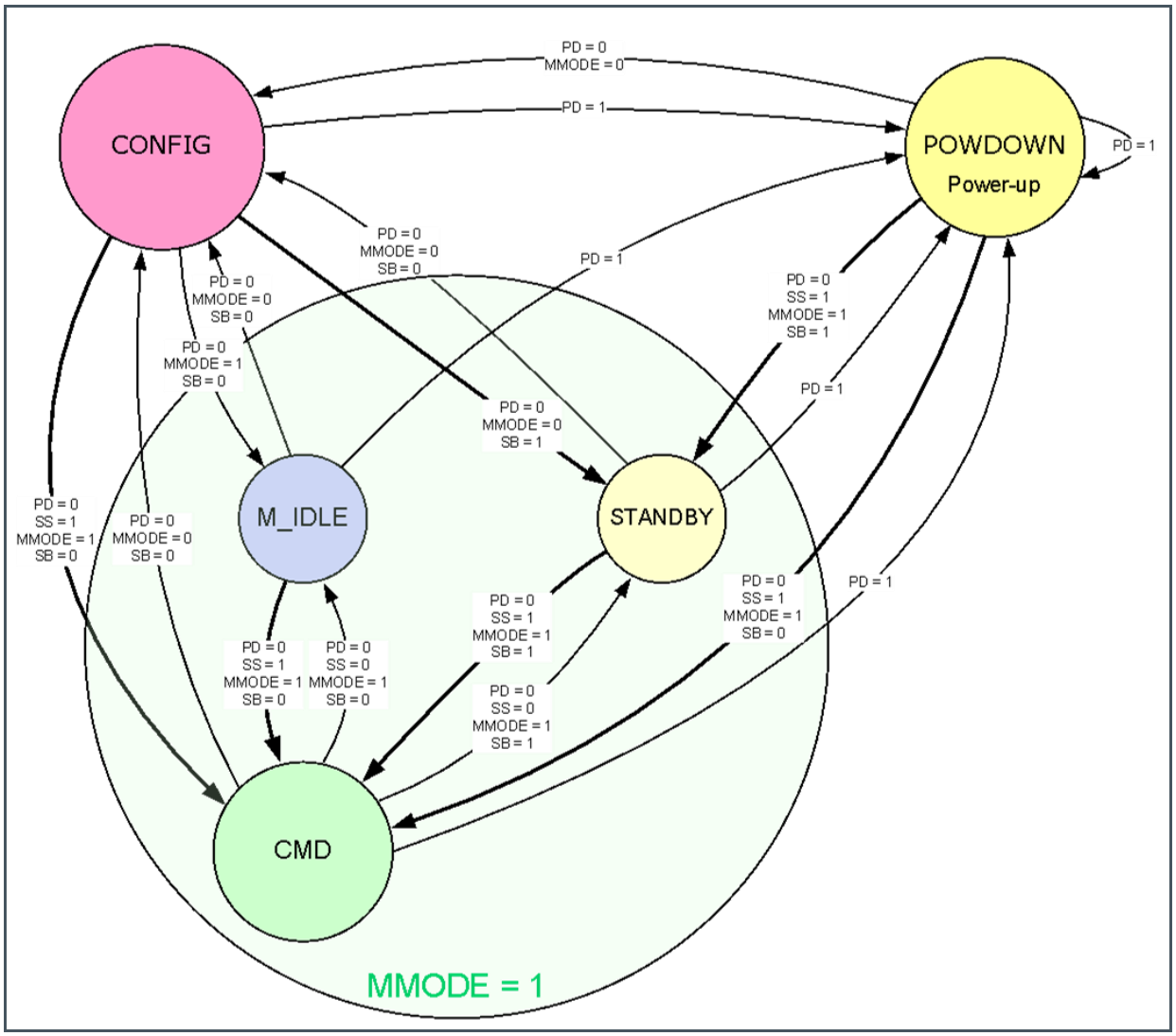
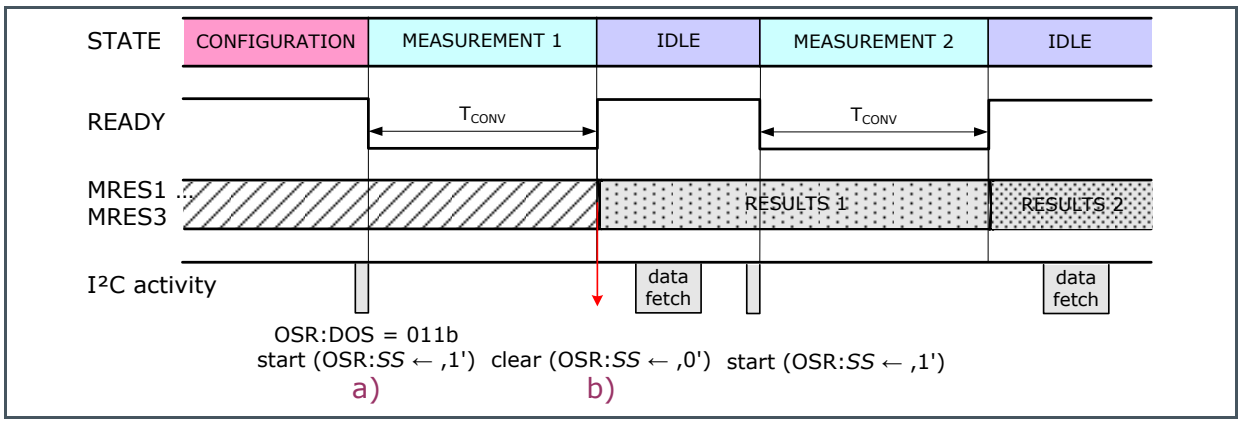


Figure 17 shows the principle sequence for a measurement start in CMD mode coming from Configuration state and waiting in Measurement state between the measurements is shown as IDLE:

1. OSR programming: 83h, change to Measurement state, start of measurement via OSR:SS = ‚1‘,
2. “Automatically” OSR programming: 03h, to reset bit OSR:SS to ‚0‘ at the end of conversion.

Figure 17:
Principle Sequence for a Measurement Start in CMD Mode Coming From Configuration State

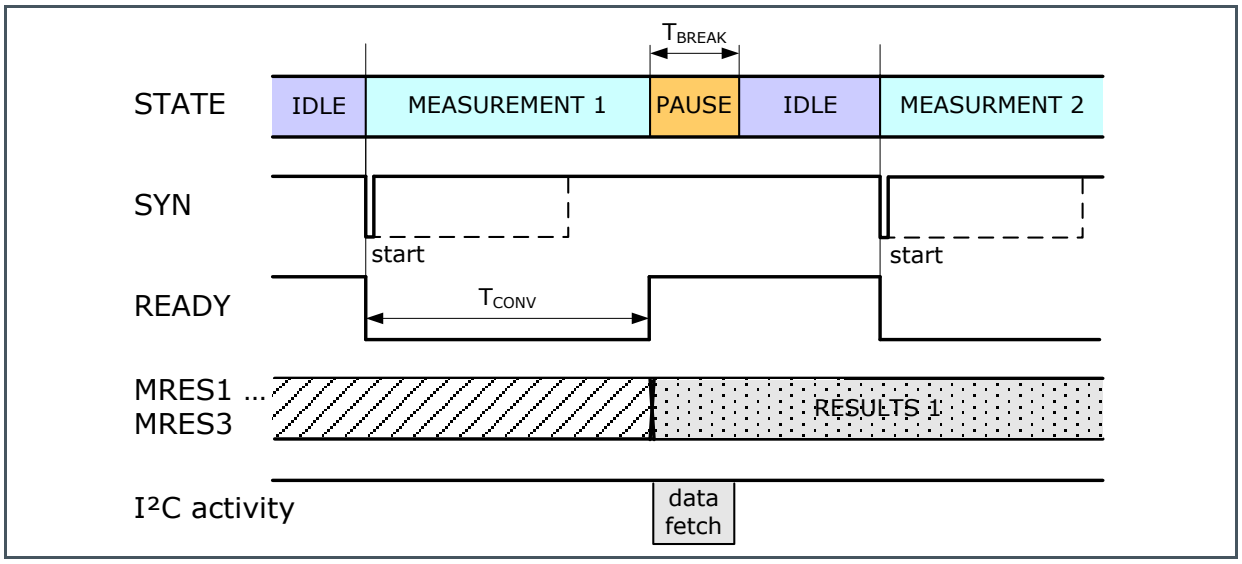


7.7 Synchronous Measurement Mode – SYNS

In this measurement mode, the input pin SYN acts as a trigger event for the start of A/D conversion. The falling edge at pin SYN starts the measurement. The conversion time (TCONV) is determined by the content of the register CREG1:TIME (see Figure 48). The pin READY signalizes the progress of conversion (see Figure 18) and its rising edge shows the end of conversion and its available valid results. The data fetch should be performed between the rising edge of signal READY and the next falling edge of signal SYN in order to allow distortion free measurement. SYN pulses during the programmed pause time TBREAK are ignored to avoid a start of the measurement during a running data fetch (see also Figure 52). The bit OSR:SS also takes effect in the SYNS mode, because the start of the measurement is only possible with OSR:SS = ‚1‘.

Figure 18 shows the principle sequence for a measurement start in SYNS mode, OSR:DOS = 011b and OSR:SS = ‚1‘ already set and waiting in Measurement state is shown as IDLE.

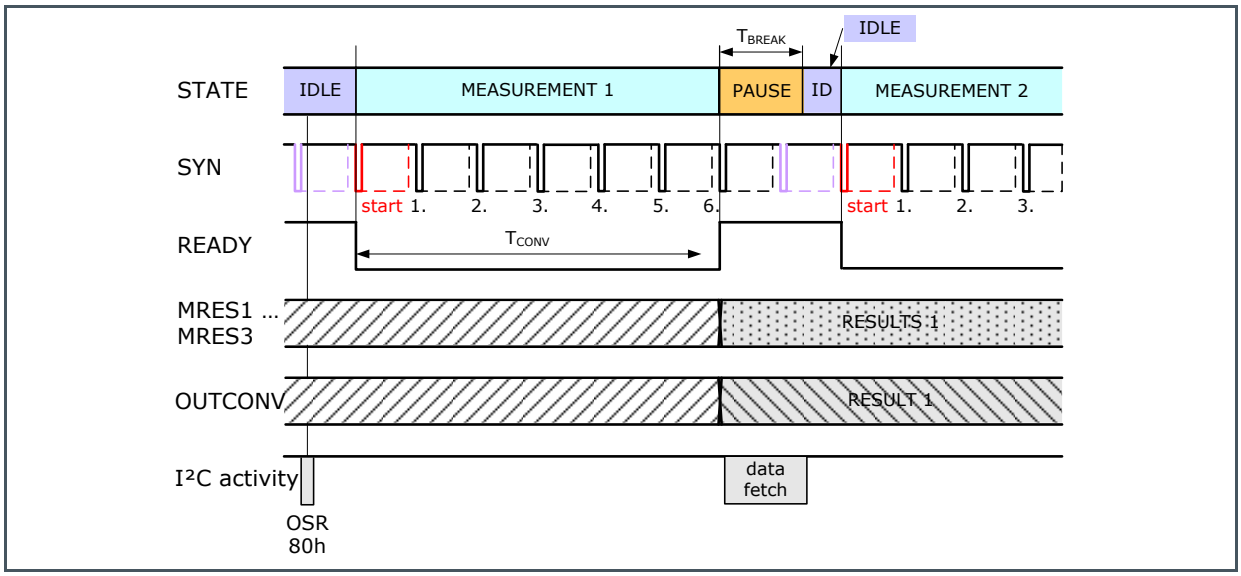
Figure 18:
Principle Sequence for a Measurement Start in SYNS Mode, OSR:DOS = 011b and OSR:SS = ‚1‘



7.8 Synchronous Measurement Start and End Mode – SYND

In this mode, the signal at pin SYN controls the start and stop of a measurement completely. When the device is waiting in Measurement state and OSR:SS is set to ‚1‘ the first falling edge at pin SYN starts the measurement. Each following falling edge of signal SYN, which occurs within the conversion time, can continue or stop the measurement. The content of the register EDGES determines, which edge is the stopping one. That means the measurement will not stop until a certain number of falling edges at pin SYN passed within the conversion time. The value of register EDGES determines the number of edges (see Figure 19 and chapter “Register - EDGES”). Figure 19 shows the principle sequence for a measurement start in SYND mode. While waiting in Measurement state is shown as IDLE, after OSR:SS is set to ‚1‘ (see Figure 45) the AS73211 waits for signal SYN to start. The conversion time is set to 06h in register EDGES, during the pause time TBREAK falling edges at pin SYN are ignored.

Figure 19:
Principle Sequence for a Measurement Start in SYND Mode



The conversion time (TCONV) is determined by the duration between the edges of start and stop of the signal SYN. If CREG2:EN_TM is set to ‚1', the register OUTCONV contains an equivalent amount of TCONV as counts of the internal clock. With the value of OUTCONV, the measurement results can be calculated more precisely (see chapter "Conversion Time Measurement in SYND Mode").

7.9 Energy Saving Options

The usage of the energy saving options is consistent for all measurement modes. The signal path at pin READY always represents independent of wake-up times or synchronizing events at pin SYN concerning the internal clock, the real measurement process. Every measurement mode can be terminated with OSR:SS = ‚0' or changing to Configuration state at every time, whereas not completed A/D conversions are not stored. In case of both energy saving options Power Down state (POWDOWN) and Standby state (STANDBY) are switched on (OSR:PD = ‚1' and CREG3:SB = ‚1'). The startup times ($T_{STARTPD}$ and $T_{STARTSB}$) run one after the other after Power Down and Standby is switched off.

7.10 Power Down

Power Down is an option to reduce the power consumption. After applying the power supply voltage including power-on reset or after software reset the AS73211 stays in Power Down state. The clock generator and all analog parts of the device are turned off. The power consumption of the device is close to zero. The digital part of the AS73211 stays idle, but a full communication via the I²C interface is granted in Configuration state and Measurement state as well.

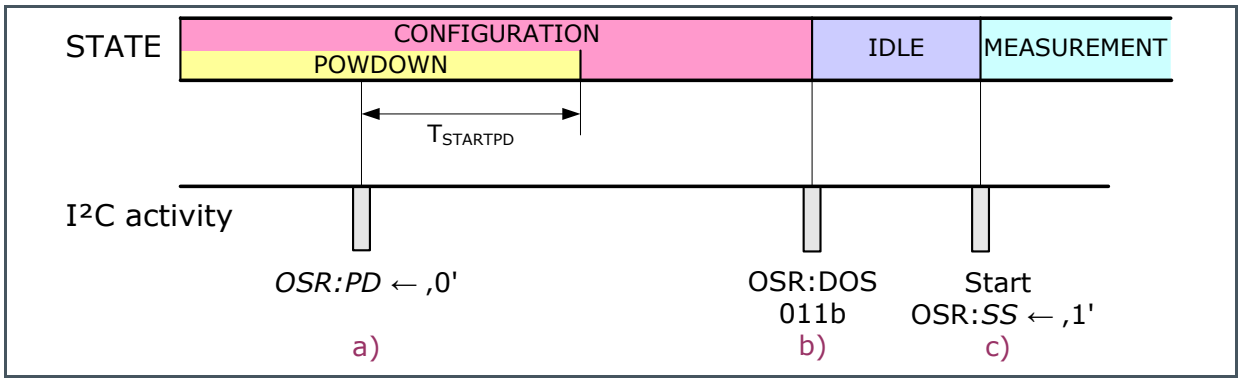
In case of the Device Operational State (DOS) is set to Measurement mode the start/stop of a measurement is possible by setting the OSR:SS bit and reading of measurement data. The Power Down can be switched on and off by the bit OSR:PD (Figure 1). Switching on Power Down via bit OSR:PD = ‚1' the AS73211 changes to the Power Down state after the end of an ongoing measurement. Switching off Power Down (OSR:PD = ‚0') results in a change to the Idle state (IDLE for waiting) or Standby state depending on bit CREG3:SB. This change to another operational state is delayed by the startup time TSTARTPD of typically 1.2ms. A conversion can start in all measurement modes while the Power Down state is activated (OSR:PD = ‚1'). In the measurement modes CMD and CONT it is done by setting the bit OSR:SS to ‚1'. In addition, the falling edge of the signal at pin SYN for the measurement modes SYNS and SYND initiate the start. In all cases, the start of conversion is delayed by the startup time TSTARTPD. After the conversion in the CMD, SYNS and SYND modes the AS73211 changes back into the Power Down state, whereas the measurement of the CONT mode is interactive until it is stopped by setting bit OSR:SS = to ‚0' before it changes back into the Power Down state.

There are two methods for startup the AS73211:

1. After applying the power supply voltage including power-on reset or after software reset the bit OSR:PD must be set to ‚0' via I²C interface communication. The analog part and the internal clock system starts to work along the defined configuration of the AS73211. Nevertheless, it is still possible to change the configuration in front of time b) of Figure 20. The Device Operational State changes to Measurement state to start the measurement (OSR:SS = ‚1') without further delay caused by energy saving options.
Figure 20 shows the principle sequence after power-on reset and separated writing of the bits OSR:PD, OSR:DOS and OSR:SS:

a) OSR programming: 02h, after TSTARTPD continuing within Configuration state only,
b) OSR programming: 03h, change to Measurement state – waiting is shown as IDLE.

Figure 20:
Principle Sequence After Power-On Reset and Separated Writing of the Bits OSR:PD, OSR:DOS and OSR:SS



2. OSR programming: 80h, start of the measurement as stated in the device's configuration. Coming from Power Down state activated by OSR:PD = ‚1' the AS73211 is active switched on not until OSR:SS is set to ‚1' (together while or with OSR:DOS = 011b). That means the bit OSR:SS is a direct start condition for the CMD and CONT modes whereas for both SYN modes also the falling edge at pin SYN is necessary for the startup. The programmed measurement mode follows after startup marked by the falling edge of the signal path at pin READY. If the configuration even contains CREG3:SB = ‚1' (as the example of Figure 21shows), additionally after startup time TSTARTPD the wake-up time TSTARTSB of 4µs follows before the measurement starts.

Figure 21:
Principle Start of the Measurement from OSR:PD = ‚1' and CREG3:SB = ‚1'

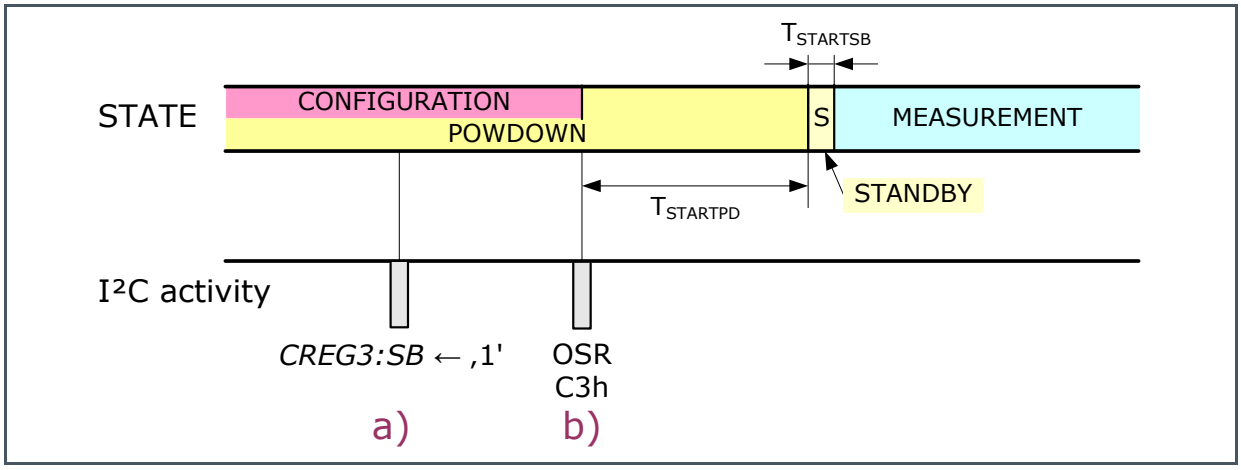


Figure 21 shows the principle start of the measurement from OSR:PD = ‚1' and CREG3:SB = ‚1':

a) CREG3 programming: bit CREG3:SB = ‚1',
b) OSR programming: C3h, start of the measurement with prior run of TSTARTPD and TSTARTS.

The programmed energy saving option (before or when measurement is started or while the measurement runs) is switched on after the regular end of the measurement and storing of the results within the buffer registers. In case of an abortion of the measurement with OSR:SS = ‚0' or switching to Configuration state the energy saving option is switched on without saving any results.

7.11 Standby

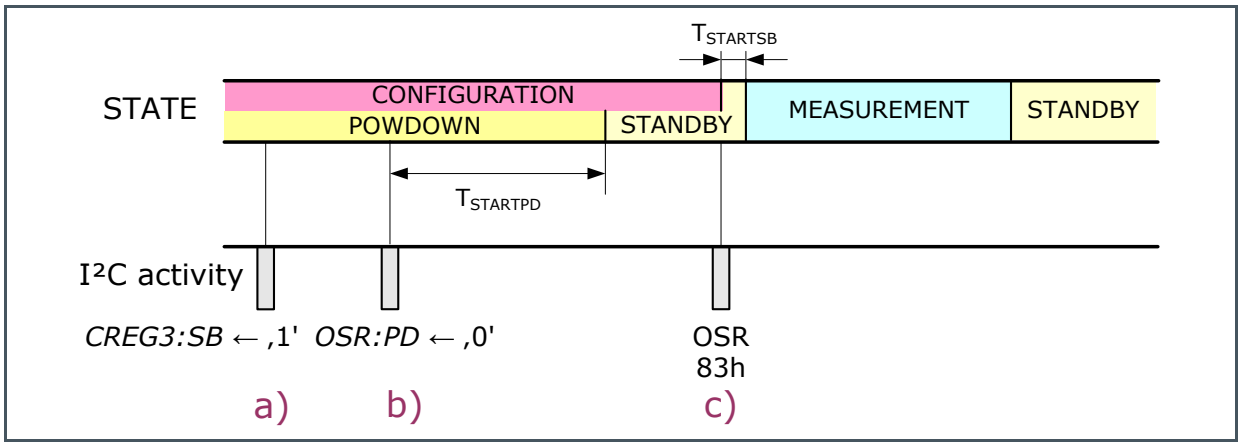
Standby is another option for reducing the power consumption, but compared to Power Down less internal analog components are switched off to be able to get back active in a very short time. The digital part of the AS73211 stays idle, but a full communication via the I²C interface is granted in Configuration state and Measurement state as well. The bit CREG3:SB can only be changed in Configuration mode. The wake-up process is possible in combination with the start condition of the configured Measurement mode. Standby is automatically deactivated by starting the CMD or CONT

measurement mode by setting the bit OSR:SS to ‚1'. In addition, for the measurement modes SYNS and SYND an initiated start is necessary by the falling edge of the signal at pin SYN. While starting the measurement the A/D conversion follows immediately after the wake-up time TSTARTSB of about 4µs.

Figure 22 shows the principle start and stop sequence of a measurement after startup with OSR:PD = ‚0' and CREG3:SB = ‚1:

a) CREG3 programming: bit CREG3:SB = ‚1',
b) OSR programming: 02h, after startup continuing with Configuration mode,
c) OSR programming: 83h, measurement start, wake-up and conversion, return to standby after measurement ends.

Figure 22:
Principle Start and Stop Sequence of a Measurement After Startup with OSR:PD = ‚0' and CREG3:SB = ‚1'

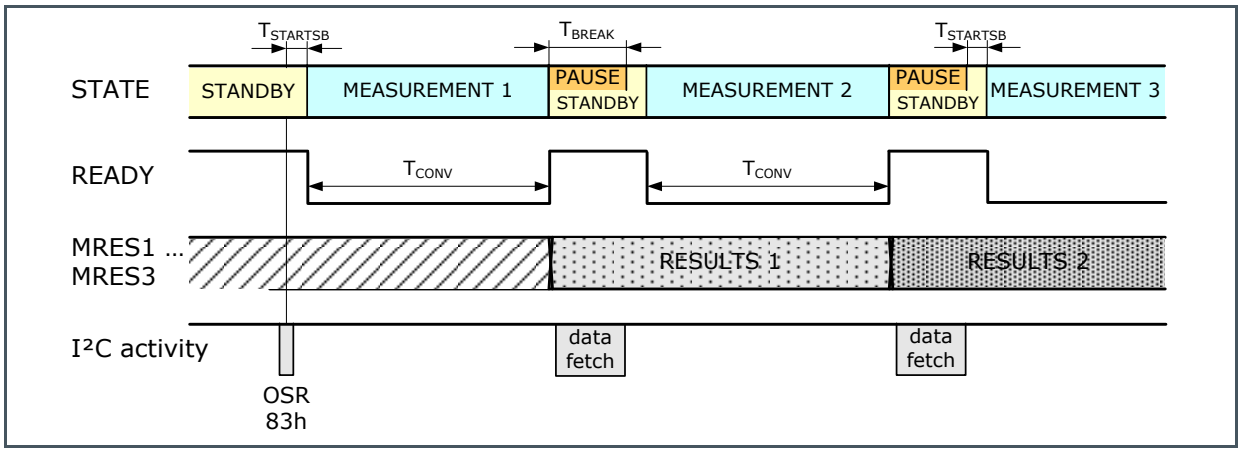


7.12 Examples

For both modes CONT and SYN it is recommended to configure a pause time TBREAK (register BREAK of Figure 52) to avoid disturbances during the A/D conversion caused by I²C interface communication. The selectable pause time using register BREAK should be long enough, that all output results are read before the next conversion starts (automatically in CONT modus or synchronized via pin SYN in SYN modes). While the pause time TBREAK is running it is possible to save energy if the bit CREG3:SB is configured to ‚1'. The wake-up time TSTARTSB of about 4µs is short compared to the necessary time for the I²C communication protocol represented by register BREAK.

Figure 23 shows the principle sequence of CONT mode: if CREG3:SB is set to ‚1', saving energy is possible while the pause time TBREAK is activated for I²C interface communication.

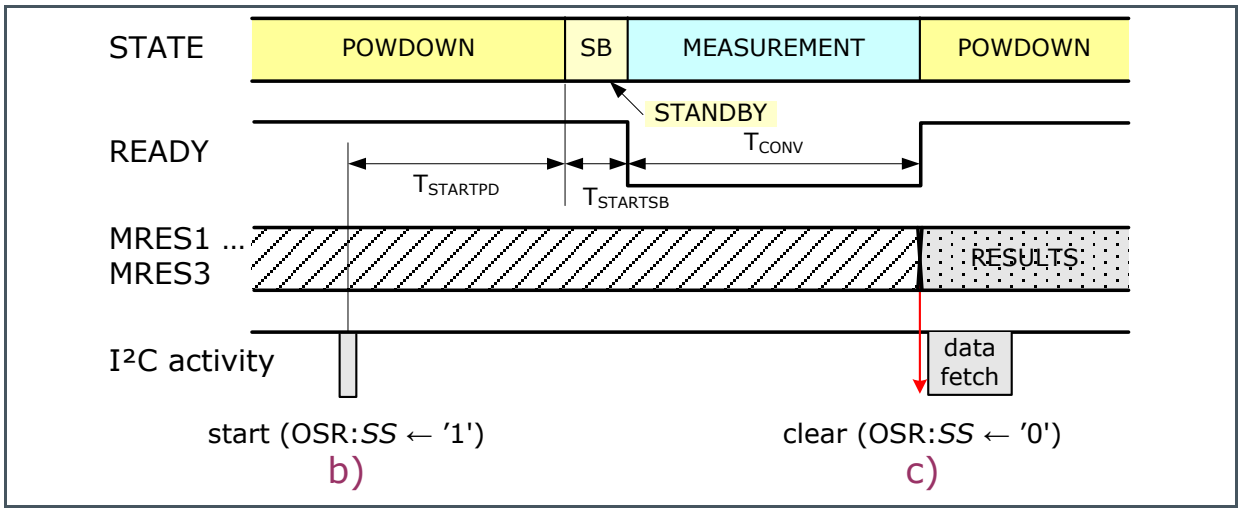
Figure 23:
Principle Sequence of CONT Mode – if CREG3:SB is Set to ‚1'



Another example shows, that after the end of a conversion in CMD mode the AS73211 returns to Power Down and/or Standby state depending on the bits OSR:PD and CREG3:SB. In case of both bits are ‚0' while in Measurement state the device would return to idle, waiting for the next measurement to start. Figure 24: Principle sequence whereas measurement starts in CMD mode with Power Down and Standby switched on (device is already in Measurement state):

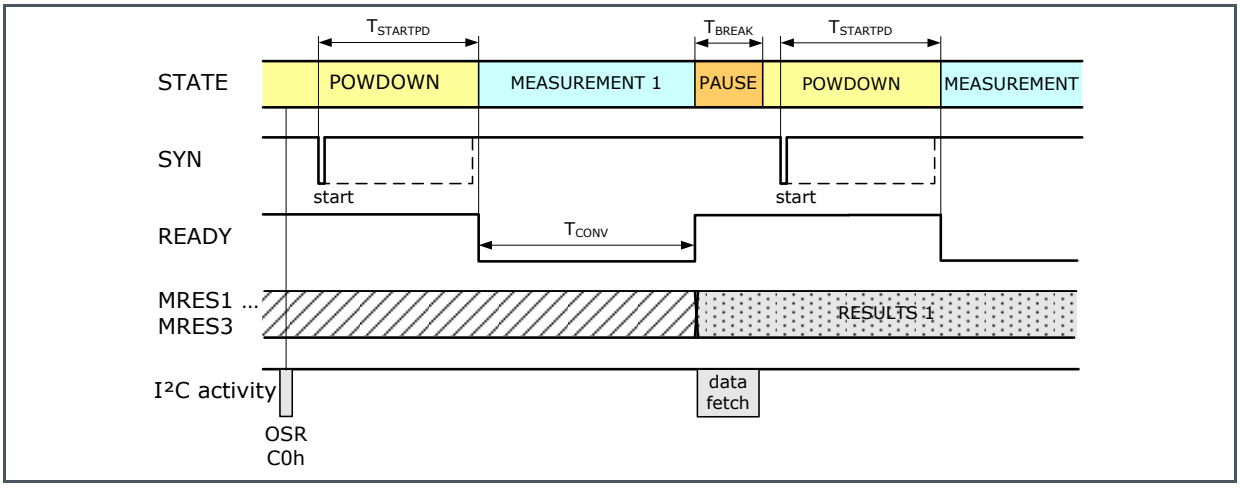
a) CREG3 programming: bit CREG3:SB = ‚1' was set in Configuration state (not shown),
b) OSR programming: C0h, “startup” and “wake-up” before conversion starts,
c) “Automatically” OSR programming: 43h, the end of conversion resets bit OSR:SS, return to Power Down.

Figure 24:
Principle Sequence Whereas Measurement is Started in CMD Mode with Power Down, Standby Switched On



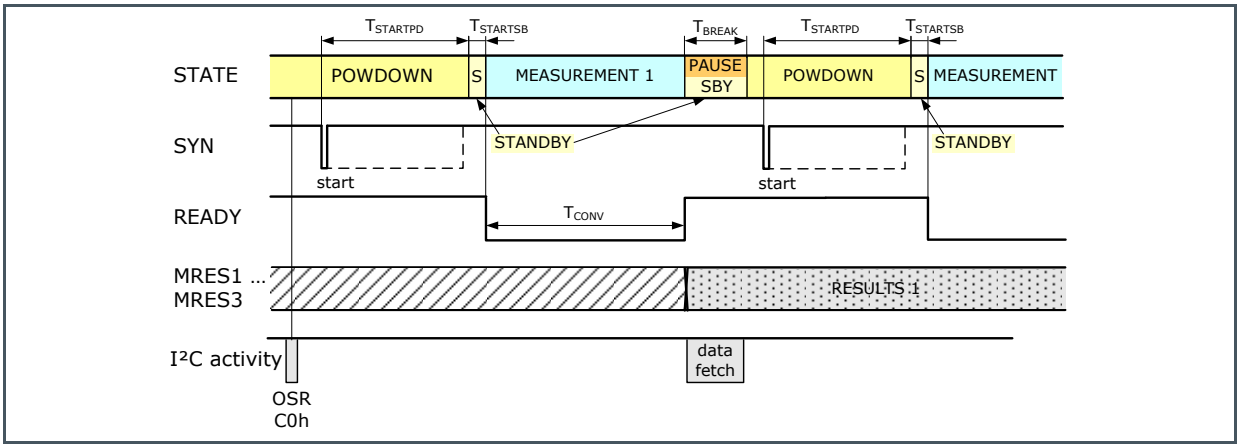
It is also possible to use Power Down state in combination with SYNS mode. The falling edge at pin SYN immediately starts the conversion after Power Down ends shown by the signal at pin READY. That kind of measurement is only useful in case of the distance between falling edges at pin SYN is more than the conversion time, pause time and startup time together. Figure 25 shows the principle sequence of measurement in SYNS mode being ready (bits OSR:PD = ‚1' and OSR:SS = ‚1') and waiting for falling edge at pin SYN to startup.

Figure 25:
Principle Sequence of Measurement in SYNS Mode



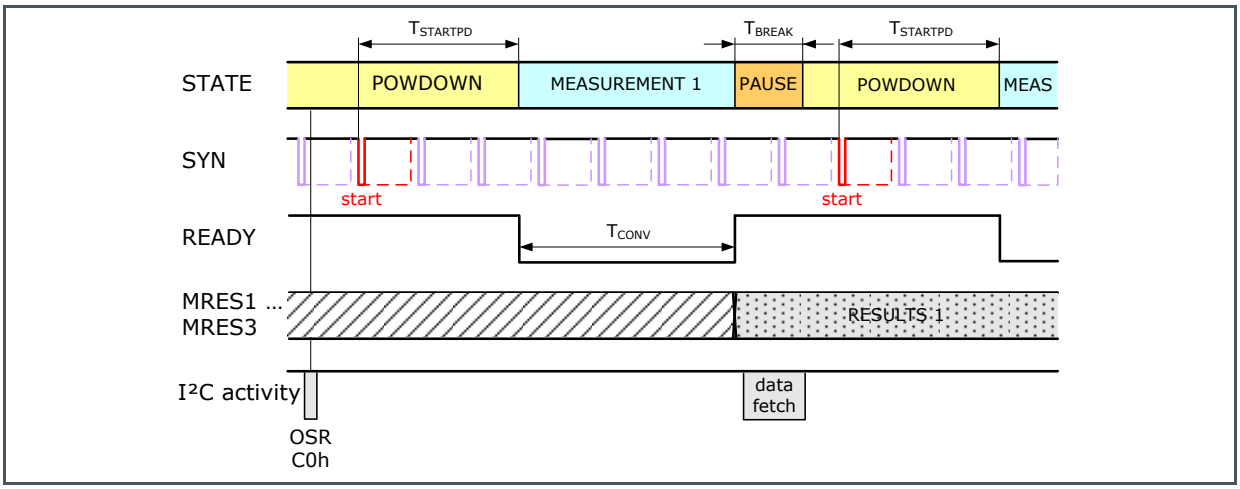
By additionally activated Standby (bit CREG3:SB = ‚1') a maximum of energy can be saved, because the operational readiness is given not until short before A/D conversion starts and with the beginning read process of the results (pause time) the device is already again saving energy in Standby state (see Figure 26). Figure 26 shows the principle sequence of measurement in SYNS mode being ready with OSR:PD = ‚1' (as in Figure 25), but now with bit CREG3:SB = ‚1' to save a maximum of energy as explained above.

Figure 26:
Principle Sequence of Measurement in SYNS Mode Being Ready with OSR:PD = ‚1'



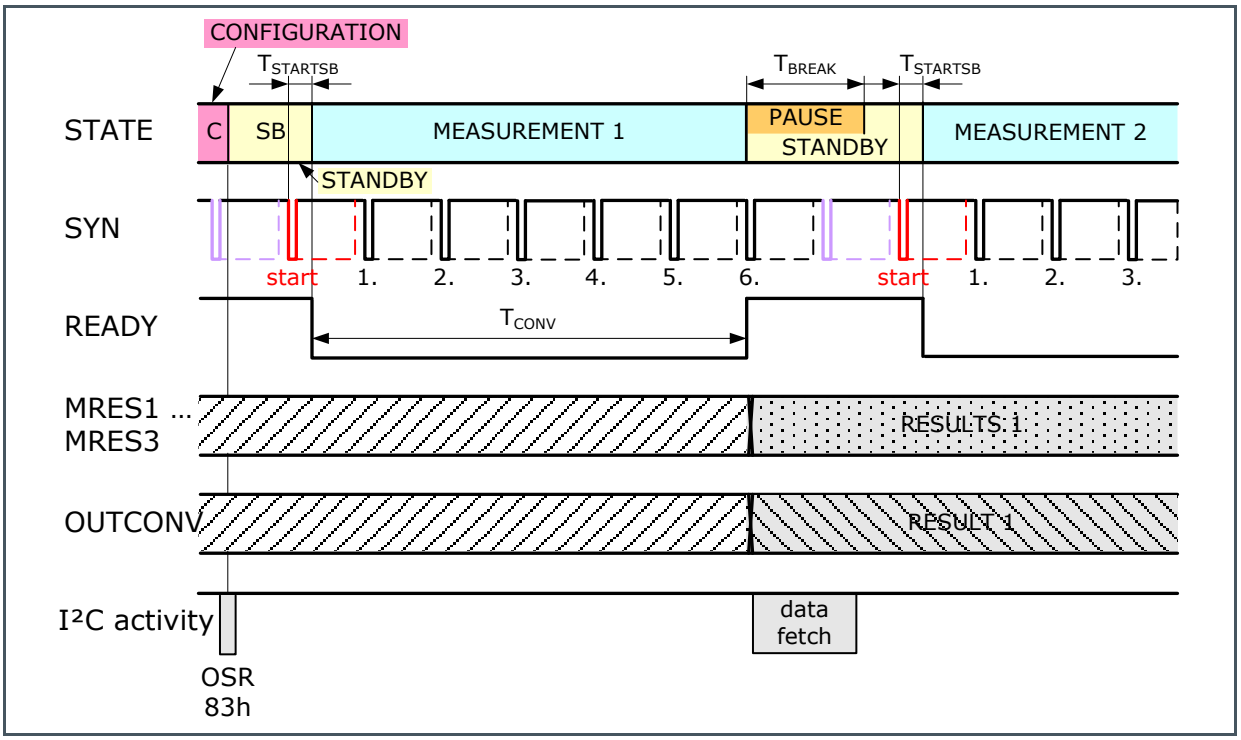
The following example of a SYNS mode shows a correct measurement procedure but with an unfavorable chosen application. After start of measurement with bit OSR:SS = ‚1‘ only the red marked falling edges (see Figure 27) at pin SYN are accepted as start condition, because of the too tight distances of the SYN edges a lot of falling edges are ignored during startup phase (TSTARTPD), conversion time (TCONV) and pause time (TBREAK).

Figure 27:
Principle Sequence of Measurement in SYNS Mode (OSR:PD , OSR:SS are set to ‚1‘)



Continuously occurring SYN pulses (e.g. generated by a PWM controlling in measurement mode SYND) are ignored in Configuration state and while pause time TBREAK (see Figure 28) is activated. It is recommended to increase the default value of register BREAK accordingly, if the time reference result OUTCONV must be read via I²C interface. The conversion time is given by register EDGES, but as shown in Figure 28 the real conversion time is always represented by TCONV at pin READY. Furthermore, the output result OUTCONV can be used to get the right measurement result (see also chapters “Transfer Function” and “Conversion Time Measurement in SYND Mode”). Figure 28 shows the principle sequence of measurement in SYND mode ready for wake-up after switch off Power Down state with OSR:PD = ‚0‘ and setting of OSR:SS to ‚1‘ in Configuration state, then waiting for start via pin SYN (with exemplary settings of EDGES = 06h and CREG3:SB = ‚1‘ for energy saving while pause time TBREAK).

Figure 28:
Principle Sequence of Measurement in SYND Mode Ready for Wake-Up After Switch Off Power Down State



7.13 Transfer Function

In generally the implemented A/D converter represents a delta-sigma converter, which performs charge balancing between the input light at the photodiodes and an internal reference. The input currents of the photodiodes result in pulse density modulated digital signals, further filtered by counters up to 24 bits. At the end, each channel's counter status represents a digital equivalent of the average input light irradiance regarding to the channel's sensor area within the conversion time interval. The input light irradiance can be calculated from the measurement result by:

Equation 1:

$$E_e = \frac{MRES}{R_e} = \frac{FSR_{E_e}}{N_{CLK}} \bullet MRES$$

Equation 2:

$$E_e = \frac{FSR_{E_e}}{T_{CONV} \bullet f_{CLK}} \bullet MRES$$

MRES: Digital output value of the conversion (content of output registers MRES1 to MRES3)

E_e: Input light irradiance regarding to the photodiode's area within the conversion time interval

FSR_{Ee}: Full Scale Range of detectable input light irradiance E_e

R_e: Irradiance responsivity (see Figure 14)

T_{CONV}: Conversion time interval

N_{CLK}: Number of clock cycles within the conversion time interval T_{CONV} (see Figure 13)

f_{CLK}: Clock frequency

In the CONT, CMD and SYNS modes the conversion time T_{CONV} is internally generated[1].In the SYND mode the conversion time is defined by the timing of the external pulses at SYN pin and the number of pulses stored in the register EDGES (see Figure 19 chapter "Conversion time measurements in SYND mode" and chapter "Register - EDGES").

The number of clock counts within this interval is a constant number, which keeps the output result independent of the internal clock frequency. In this case the input light irradiance E_e regarding to the photodiodes area of the channel can be represented by the Equation 1. In SYND mode, the Equation 2 represents the externally generated conversion time TCONV and the conversion result. If the conversion time measurement is activated (CREG2:EN_TM = ‚1') the number of clock counts within the externally given conversion time can also be internally captured. So the input light irradiance E_e regarding to the photodiode's area of the channel can be calculated as:

Equation 3:

$$E_e = \frac{FSR_{E_e}}{OUTCONV} \bullet MRES$$

MRES: Digital output value of the conversion (content of output registers MRES1 to MRES3)

E_e: Input light irradiance regarding to the photodiode's area within the conversion time interval

FSR_{Ee}: Full Scale Range of detectable input light irradiance E_e

OUTCONV: Conversion time duration expressed as the number of clock counts within this time.

In this way, the input light irradiance can be measured independently of the internal frequency and furthermore external conversion time variations in SYND mode.

The calculation of the input light irradiance by Equation 3 is more precise than the result of Equation 2 because the tolerances of the clock frequency f_{CLK} are eliminated. The irradiance responsivity R_e and

[1] The system clock is internally generated and is subject to technological tolerances. So the clock frequency may vary, which must be considered when calculating the time to be programmed (e. g. registers BREAK for pause time TBREAK or CREG1:TIME for conversion time TCONV).

internal conversion time TCONV are determined by the content of register bits CREG1:GAIN and CREG1:TIME (see Figure 48). Their values directly determine the sensitivity, the LSB value and the full-scale range (FSR) of the detectable irradiance E_e of the A/D conversion.

Figure 29:
X-Channel (λ = 600nm) Programmable FSR and LSB of the Detectable Input Light Irradiance E_e with CREG1:TIME Programming from 0 to 7 and CREG1:GAIN Programming from 0 to 11 – CONT, CMD and SYNS Mode

TIME (1)	0	1	2	3	4	5	6	7
NCLK(1)	1024	2048	4096	8192	16384	32768	65536	131072
TCONV[ms](1)	1	2	4	8	16	32	64	128
RESOL[bit](1)	10	11	12	13	14	15	16	17
GAIN(1)	FSR [µW/cm²] of detectable irradiance Ee (channel X)							
2048x	13.854							6.927
1024x	27.707							13.854
512x	55.414							27.707
256x	110.828							55.414
128x	221.657							110.828
64x	443.314							221.657
32x	886.628							443.314
16x	1773.255							886.628
8x	3546.510							1773.255
4x	7093.020							3546.510
2x	14186.041							7093.020
1x	28372.081							14186.041
GAIN (1)	LSB [nW/cm²] – least significant bit of FSR (channel X)							
2048x	13.5289	6.7644	3.3822	1.6911	0.8456	0.4228	0.2114	0.1057
1024x	27.0577	13.5289	6.7644	3.3822	1.6911	0.8456	0.4228	0.2114
512x	54.1155	27.0577	13.5289	6.7644	3.3822	1.6911	0.8456	0.4228
256x	108.2309	54.1155	27.0577	13.5289	6.7644	3.3822	1.6911	0.8456
128x	216.4618	108.2309	54.1155	27.0577	13.5289	6.7644	3.3822	1.6911
64x	432.9236	216.4618	108.2309	54.1155	27.0577	13.5289	6.7644	3.3822
32x	865.8472	432.9236	216.4618	108.2309	54.1155	27.0577	13.5289	6.7644
16x	1731.6944	865.8472	432.9236	216.4618	108.2309	54.1155	27.0577	13.5289
8x	3463.3888	1731.6944	865.8472	432.9236	216.4618	108.2309	54.1155	27.0577
4x	6926.7777	3463.3888	1731.6944	865.8472	432.9236	216.4618	108.2309	54.1155
2x	13853.5554	6926.7777	3463.3888	1731.6944	865.8472	432.9236	216.4618	108.2309
1x	27707.1108	13853.5554	6926.7777	3463.3888	1731.6944	865.8472	432.9236	216.4618

(1) TIME (TCONV) – given by CREG1:TIME = 0 … 7 dec, NCLK – number of clock cycle within conversion time TCONV, RESOL – Resolution of internal A/D conversion, GAIN = 1x given by CREG1:GAIN = 11dec up to GAIN = 2048x given by CREG1:GAIN = 0dec (see Figure 48)

Figure 30:
X-Channel (λ = 600nm) Programmable FSR and LSB of the Detectable Input Light Irradiance Ee with CREG1:TIME Programming from 8 to and CREG1:GAIN Programming from 0 to 11 – CONT, CMD and SYNS Mode

TIME (1)	8	9	10	11	12	13	14	15
N_{CLK}(1)	262144	524288	1.05E+06	2.10E+06	4.19E+06	8.39E+06	1.68E+07	1024
T_{CONV}[s](1)	0.256	0.512	1.024	2.048	4.096	8.192	16.384	0.001
R_{ESOL}[bit](1)	18	19	20	21	22	23	24	10
GAIN(1)	FSR [µW/cm²] of detectable irradiance Ee (channel X)							
2048x	3.463	1.732	0.866	0.433	0.216	0.108	0.054	13.854
1024x	6.927	3.463	1.732	0.866	0.433	0.216	0.108	27.707
512x	13.854	6.927	3.463	1.732	0.866	0.433	0.216	55.414
256x	27.707	13.854	6.927	3.463	1.732	0.866	0.433	110.828
128x	55.414	27.707	13.854	6.927	3.463	1.732	0.866	221.657
64x	110.828	55.414	27.707	13.854	6.927	3.463	1.732	443.314
32x	221.657	110.828	55.414	27.707	13.854	6.927	3.463	886.628
16x	443.314	221.657	110.828	55.414	27.707	13.854	6.927	1773.255
8x	886.628	443.314	221.657	110.828	55.414	27.707	13.854	3546.510
4x	1773.255	886.628	443.314	221.657	110.828	55.414	27.707	7093.020
2x	3546.510	1773.255	886.628	443.314	221.657	110.828	55.414	14186.041
1x	7093.020	3546.510	1773.255	886.628	443.314	221.657	110.828	28372.081
GAIN(1)	LSB [nW/cm²] – least significant bit of FSR (channel X)							
2048x	0.0528	0.0264	0.0132	0.0066	0.0033	0.0017	0.0008	13.5289
1024x	0.1057	0.0528	0.0264	0.0132	0.0066	0.0033	0.0017	27.0577
512x	0.2114	0.1057	0.0528	0.0264	0.0132	0.0066	0.0033	54.1155
256x	0.4228	0.2114	0.1057	0.0528	0.0264	0.0132	0.0066	108.2309
128x	0.8456	0.4228	0.2114	0.1057	0.0528	0.0264	0.0132	216.4618
64x	1.6911	0.8456	0.4228	0.2114	0.1057	0.0528	0.0264	432.9236
32x	3.3822	1.6911	0.8456	0.4228	0.2114	0.1057	0.0528	865.8472
16x	6.7644	3.3822	1.6911	0.8456	0.4228	0.2114	0.1057	1731.6944
8x	13.5289	6.7644	3.3822	1.6911	0.8456	0.4228	0.2114	3463.3888
4x	27.0577	13.5289	6.7644	3.3822	1.6911	0.8456	0.4228	6926.7777
2x	54.1155	27.0577	13.5289	6.7644	3.3822	1.6911	0.8456	13853.5554
1x	108.2309	54.1155	27.0577	13.5289	6.7644	3.3822	1.6911	27707.1108

(1) TIME (TCONV) – given by CREG1:TIME = 8 … 15 dec, NCLK – number of clock cycle within conversion time TCONV, RESOL – Resolution of internal A/D conversion, GAIN = 1x given by CREG1:GAIN = 11dec up to GAIN = 2048x given by CREG1:GAIN = 0dec (see Figure 48)

Figure 31:
Y-Channel (λ = 555nm) Programmable FSR and LSB of the Detectable Input Light Irradiance Ee with CREG1:TIME Programming from 0 to 7 and CREG1:GAIN Programming from 0 to 11 – CONT, CMD and SYNS Mode

TIME(1)	0	1	2	3	4	5	6	7
N_{CLK}(1)	1024	2048	4096	8192	16384	32768	65536	131072
T_{CONV}[ms](1)	1	2	4	8	16	32	64	128
R_{ESOL}[bit](1)	10	11	12	13	14	15	16	17
GAIN(1)	FSR [µW/cm²] of detectable irradiance Ee (channel Y)							
2048x	14.919							7.460
1024x	29.838							14.919
512x	59.677							29.838
256x	119.354							59.677
128x	238.707							119.354
64x	477.415							238.707
32x	954.830							477.415
16x	1909.659							954.830
8x	3819.319							1909.659
4x	7638.637							3819.319
2x	15277.275							7638.637
1x	30554.549							15277.275
GAIN(1)	LSB [nW/cm²] – least significant bit of FSR (channel Y)							
2048x	14.570	7.285	3.642	1.821	0.911	0.455	0.228	0.114
1024x	29.139	14.570	7.285	3.642	1.821	0.911	0.455	0.228
512x	58.278	29.139	14.570	7.285	3.642	1.821	0.911	0.455
256x	116.556	58.278	29.139	14.570	7.285	3.642	1.821	0.911
128x	233.113	116.556	58.278	29.139	14.570	7.285	3.642	1.821
64x	466.225	233.113	116.556	58.278	29.139	14.570	7.285	3.642
32x	932.451	466.225	233.113	116.556	58.278	29.139	14.570	7.285
16x	1864.902	932.451	466.225	233.113	116.556	58.278	29.139	14.570
8x	3729.803	1864.902	932.451	466.225	233.113	116.556	58.278	29.139
4x	7459.607	3729.803	1864.902	932.451	466.225	233.113	116.556	58.278
2x	14919.214	7459.607	3729.803	1864.902	932.451	466.225	233.113	116.556
1x	29838.427	14919.214	7459.607	3729.803	1864.902	932.451	466.225	233.113

(1) TIME (TCONV) – given by CREG1:TIME = 0 … 7 dec, N_{CLK} – number of clock cycle within conversion time TCONV, R_{ESOL} – Resolution of internal A/D conversion, GAIN = 1x given by CREG1:GAIN = 11dec up to GAIN = 2048x given by CREG1:GAIN = 0dec (see Figure 48).

Figure 32:
Y-Channel (λ = 555nm) Programmable FSR and LSB of the Detectable Input Light Irradiance Ee with CREG1:TIME Programming from 8 to 15 and CREG1:GAIN Programming from 0 to 11 – CONT, CMD and SYNS Mode

TIME(1)	8	9	10	11	12	13	14	15
N_{CLK}(1)	262144	524288	1.05E+06	2.10E+06	4.19E+06	8.39E+06	1.68E+07	1024
T_{CONV}[s](1)	0.256	0.512	1.024	2.048	4.096	8.192	16.384	0.001
R_{ESOL}[bit](1)	18	19	20	21	22	23	24	10
GAIN(1)	FSR [µW/cm²] of detectable irradiance Ee (channel Y)							
2048x	3.730	1.865	0.932	0.466	0.233	0.117	0.058	14.919
1024x	7.460	3.730	1.865	0.932	0.466	0.233	0.117	29.838
512x	14.919	7.460	3.730	1.865	0.932	0.466	0.233	59.677
256x	29.838	14.919	7.460	3.730	1.865	0.932	0.466	119.354
128x	59.677	29.838	14.919	7.460	3.730	1.865	0.932	238.707
64x	119.354	59.677	29.838	14.919	7.460	3.730	1.865	477.415
32x	238.707	119.354	59.677	29.838	14.919	7.460	3.730	954.830
16x	477.415	238.707	119.354	59.677	29.838	14.919	7.460	1909.659
8x	954.830	477.415	238.707	119.354	59.677	29.838	14.919	3819.319
4x	1909.659	954.830	477.415	238.707	119.354	59.677	29.838	7638.637
2x	3819.319	1909.659	954.830	477.415	238.707	119.354	59.677	15277.275
1x	7638.637	3819.319	1909.659	954.830	477.415	238.707	119.354	30554.549
GAIN(1)	LSB [nW/cm²] – least significant bit of FSR (channel Y)							
2048x	0.057	0.028	0.0142	0.007	0.004	0.002	0.001	14.570
1024x	0.114	0.057	0.0285	0.014	0.007	0.004	0.002	29.139
512x	0.228	0.114	0.0569	0.028	0.014	0.007	0.004	58.278
256x	0.455	0.228	0.1138	0.057	0.028	0.014	0.007	116.556
128x	0.911	0.455	0.2276	0.114	0.057	0.028	0.014	233.113
64x	1.821	0.911	0.4553	0.228	0.114	0.057	0.028	466.225
32x	3.642	1.821	0.9106	0.455	0.228	0.114	0.057	932.451
16x	7.285	3.642	1.8212	0.911	0.455	0.228	0.114	1864.902
8x	14.570	7.285	3.6424	1.821	0.911	0.455	0.228	3729.803
4x	29.139	14.570	7.2848	3.642	1.821	0.911	0.455	7459.607
2x	58.278	29.139	14.5695	7.285	3.642	1.821	0.911	14919.214
1x	116.556	58.278	29.1391	14.570	7.285	3.642	1.821	29838.427

(1) TIME (T_{CONV}) – given by CREG1:TIME = 8 … 15 dec, N_{CLK} – number of clock cycle within conversion time T_{CONV}, R_{ESOL} – Resolution of internal A/D conversion, GAIN = 1x given by CREG1:GAIN = 11dec up to GAIN = 2048x given by CREG1:GAIN = 0dec (see Figure 48).

Figure 33:
Z-Channel (λ = 445nm) Programmable FSR and LSB of the Detectable Input Light Irradiance Ee with CREG1:TIME Programming from 0 to 7 and CREG1:GAIN Programming from 0 to 11 – CONT, CMD and SYNS Mode

TIME(1)	0	1	2	3	4	5	6	7
N_{CLK}(1)	1024	2048	4096	8192	16384	32768	65536	131072
T_{CONV}[ms](1)	1	2	4	8	16	32	64	128
R_{ESOL}[bit](1)	10	11	12	13	14	15	16	17
GAIN(1)	FSR [µW/cm²] of detectable irradiance Ee (channel Z)							
2048x	8.012				4.006			
1024x	16.024				8.012			
512x	32.048				16.024			
256x	64.097				32.048			
128x	128.194				64.097			
64x	256.387				128.194			
32x	512.774				256.387			
16x	1025.548				512.774			
8x	2051.097				1025.548			
4x	4102.193				2051.097			
2x	8204.387				4102.193			
1x	16408.773				8204.387			
GAIN(1)	LSB [nW/cm²] – least significant bit of FSR (channel Z)							
2048x	7.8243	3.9122	1.9561	0.9780	0.4890	0.2445	0.1223	0.0611
1024x	15.6486	7.8243	3.9122	1.9561	0.9780	0.4890	0.2445	0.1223
512x	31.2973	15.6486	7.8243	3.9122	1.9561	0.9780	0.4890	0.2445
256x	62.5945	31.2973	15.6486	7.8243	3.9122	1.9561	0.9780	0.4890
128x	125.1890	62.5945	31.2973	15.6486	7.8243	3.9122	1.9561	0.9780
64x	250.3780	125.1890	62.5945	31.2973	15.6486	7.8243	3.9122	1.9561
32x	500.7560	250.3780	125.1890	62.5945	31.2973	15.6486	7.8243	3.9122
16x	1001.5120	500.7560	250.3780	125.1890	62.5945	31.2973	15.6486	7.8243
8x	2003.0241	1001.5120	500.7560	250.3780	125.1890	62.5945	31.2973	15.6486
4x	4006.0482	2003.0241	1001.5120	500.7560	250.3780	125.1890	62.5945	31.2973
2x	8012.0963	4006.0482	2003.0241	1001.5120	500.7560	250.3780	125.1890	62.5945
1x	16024.1927	8012.0963	4006.0482	2003.0241	1001.5120	500.7560	250.3780	125.1890

(1) TIME (TCONV) – given by CREG1:TIME = 0 … 7 dec, N_{CLK} – number of clock cycle within conversion time TCONV, R_{ESOL} – Resolution of internal A/D conversion, GAIN = 1x given by CREG1:GAIN = 11dec up to GAIN = 2048x given by CREG1:GAIN = 0dec (see Figure 48).

Figure 34:
Z-Channel (λ = 445nm) Programmable FSR and LSB of the Detectable Input Light Irradiance Ee with CREG1:TIME Programming from 8 to 15 and CREG1:GAIN Programming from 0 to 11 – CONT, CMD and SYNS Mode

TIME(1)	8	9	10	11	12	13	14	15
N_{CLK}(1)	262144	524288	1.05E+06	2.10E+06	4.19E+06	8.39E+06	1.68E+07	1024
T_{CONV}[s](1)	0.256	0.512	1.024	2.048	4.096	8.192	16.384	0.001
R_{ESOL}[bit](1)	18	19	20	21	22	23	24	10
GAIN(1)	FSR [µW/cm²] of detectable irradiance Ee (channel Z)							
2048x	2.003	1.002	0.501	0.250	0.125	0.063	0.031	8.012
1024x	4.006	2.003	1.002	0.501	0.250	0.125	0.063	16.024
512x	8.012	4.006	2.003	1.002	0.501	0.250	0.125	32.048
256x	16.024	8.012	4.006	2.003	1.002	0.501	0.250	64.097
128x	32.048	16.024	8.012	4.006	2.003	1.002	0.501	128.194
64x	64.097	32.048	16.024	8.012	4.006	2.003	1.002	256.387
32x	128.194	64.097	32.048	16.024	8.012	4.006	2.003	512.774
16x	256.387	128.194	64.097	32.048	16.024	8.012	4.006	1025.548
8x	512.774	256.387	128.194	64.097	32.048	16.024	8.012	2051.097
4x	1025.548	512.774	256.387	128.194	64.097	32.048	16.024	4102.193
2x	2051.097	1025.548	512.774	256.387	128.194	64.097	32.048	8204.387
1x	4102.193	2051.097	1025.548	512.774	256.387	128.194	64.097	16408.773
GAIN(1)	LSB [nW/cm²] – least significant bit of FSR (channel Z)							
2048x	0.0306	0.0153	0.0076	0.0038	0.0019	0.0010	0.0005	7.8243
1024x	0.0611	0.0306	0.0153	0.0076	0.0038	0.0019	0.0010	15.6486
512x	0.1223	0.0611	0.0306	0.0153	0.0076	0.0038	0.0019	31.2973
256x	0.2445	0.1223	0.0611	0.0306	0.0153	0.0076	0.0038	62.5945
128x	0.4890	0.2445	0.1223	0.0611	0.0306	0.0153	0.0076	125.1890
64x	0.9780	0.4890	0.2445	0.1223	0.0611	0.0306	0.0153	250.3780
32x	1.9561	0.9780	0.4890	0.2445	0.1223	0.0611	0.0306	500.7560
16x	3.9122	1.9561	0.9780	0.4890	0.2445	0.1223	0.0611	1001.5120
8x	7.8243	3.9122	1.9561	0.9780	0.4890	0.2445	0.1223	2003.0241
4x	15.6486	7.8243	3.9122	1.9561	0.9780	0.4890	0.2445	4006.0482
2x	31.2973	15.6486	7.8243	3.9122	1.9561	0.9780	0.4890	8012.0963
1x	62.5945	31.2973	15.6486	7.8243	3.9122	1.9561	0.9780	16024.1927

(1) TIME (TCONV) – given by CREG1:TIME = 8 … 15 dec, N_{CLK} – number of clock cycle within conversion time TCONV, R_{ESOL} – Resolution of internal A/D conversion, GAIN = 1x given by CREG1:GAIN = 11dec up to GAIN = 2048x given by CREG1:GAIN = 0dec (see Figure 48).

In the SYND mode, the maximum value of the conversion result depends on the external controlled conversion time. This maximum achievable count is equal to OUTCONV and differs from the full-scale count achievable in CMD, CONT and SYNS mode.

The value of CREG1:TIME defines the number of clock counts during the conversion time. It defines the conversion time duration and maximal resolution of the A/D conversion. This is valid for the CONT, CMD and SYNS mode.

In the SYND mode the value of CREG1:TIME does not have any meaning for the conversion time duration, because this time is externally defined.

For values of CREG1:TIME higher than 6dec (0110b) T_{CONV} becomes bigger than 2^{16}, which results in A/D conversions with a higher resolution starting from 17 bit up to 24 bit. Only the least 16 significant bits are further processed and stored in the result registers. Using the implemented divider (see chapter ”Divider”) helps to access the upper 8 bits, too.

The value of CREG1:GAIN defines the A/D converter’s gain (see Figure 48 and FSR values in Figure 29 to Figure 34), which determines the sensor’s irradiance responsivity R_e. The values of CREG1:GAIN of the referred tables are only valid for a clock frequency f_{CLK} of 1MHz. For higher clock frequencies, some gain increments are not accessible. Figure 45 shows the valid gains in dependency of the chosen internal system clock via CREG3:CCLK.

Figure 35:
Achievable GAIN for Different Internal Clock Frequencies Chosen by CREG3:CCLK

CREG3:CCLK [dec]	0	1	2	3
fCLK [MHz]	1.024	2.048	4.096	8.192
CREG1:GAIN [dec]		adjustable GAIN		
0	2048x	1024x	512x	256x
1	1024x			
2	512x	512x		
3	256x	256x	256x	
4	128x	128x	128x	64x
5	64x	64x	64x	
6	32x	32x	32x	16x
7	16x	16x	16x	
8	8x	8x	8x	4x
9	4x	4x	4x	
10	2x	2x	2x	1x
11	1x	1x	1x	

During the measurement cycle within the conversion time TCONV an input signal overdriving must be avoided, even if it occurs limited in time related to TCONV. In this case, the input light is too much concerning the chosen irradiance responsivity Re of the AS73211 tolerates. An internal function of the analog conversion monitors all channels during the conversion process in terms of the relation of input light and chosen irradiance responsivity Re determined via CREG1:GAIN. In case the input light of at least one of the channels is too much, the status bit STATUS:ADCOF (see Figure 54) is set to signalize the problem and the chosen GAIN of the A/D converter (CREG1:GAIN) has to be decreased for reducing the irradiance responsivity Re of the sensor.

7.14 Divider

For the purpose to expand the measurement ranges, an internal implemented divider or prescaler can be used to scale the results. This might be necessary if the resolution of the conversion is set to a value higher than 16 bits. If the digital divider is used the conversion result is downscaled according to:

Equation 4:

$$E_e = \frac{2^{1+DIV[\mathrm{dec}]} \bullet MRES}{R_e} = \frac{FSR_{E_e}}{N_{CLK}} \bullet 2^{1+DIV[\mathrm{dec}]} \bullet MRES$$

MRES: Digital output value of the conversion (content of output registers MRES1 to MRES3)

E_e: Input light irradiance regarding to the photodiode's area within the conversion time interval

FSR_{Ee}: Full Scale Range of detectable input light irradiance E_e

R_e: Irradiance responsivity (see Figure 48)

N_{CLK}: Number of clock cycles within the conversion time interval T_{CONV} (see Figure 48)

$2^{1+DIV[dec]}$: Value of the divider factor respectively prescaler (CREG2:DIV = 7…0), see Figure 49.

The A/D converters of the AS73211 operate with a resolution of 24 bits, but their results are only provided as 16-bit wide values. The divider allows to read out the otherwise not available upper 8 bits, depending on the value of CREG2:DIV, if CREG2:EN_DIV is set to ‚1'.

Therefore, the divider acts as feature to digitally downscale the converter gain, but with a larger full scale range (FSR). The effective dynamic range of the device is increased without changing the conversion time.

Figure 36:
Relation of the Measurement Result to the Conversion Time Without Divider Respectively Prescaler

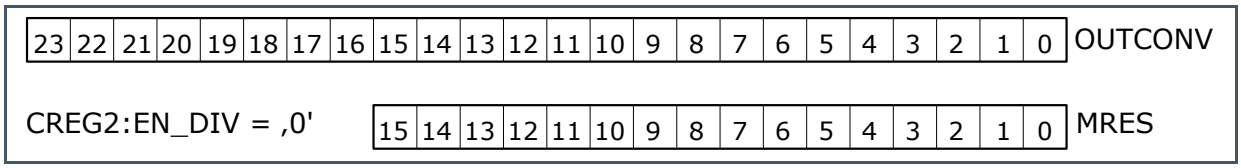
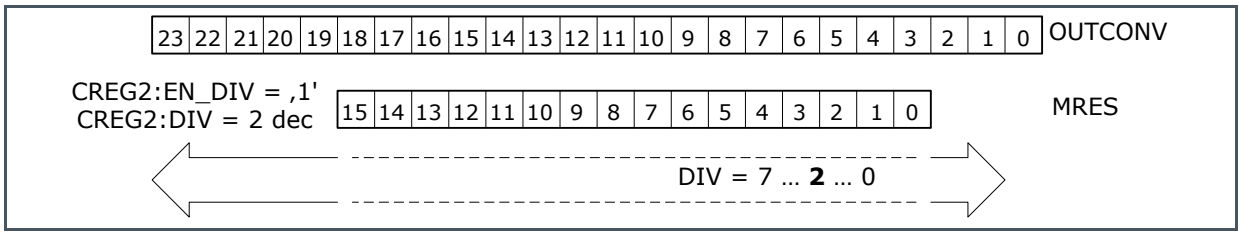


Figure 36 shows the width of the register for the conversion time (OUTCONV), which represents the internal resolution of the A/D conversion. Furthermore the measurement result (MRES[1…3]) is shown, which is 16 bits wide. For all conversion times from 2^{10} to 2^{16} there is no need to use the divider, because OUTCONV is limited to the conversion time length.

For conversion times bigger than 2^{16} the conversion result is longer than 16 bits. Without the function of the divider, the result contains always the 16 least significant bits. Now the divider makes it possible to access most significant bits by shifting the 16-bit resolution of the measurement result over the possible range of the resolution given by the conversion time register (OUTCONV).

Figure 37 shows an example, where CREG2:DIV = 2dec and therefore the divider factor is 2^3. MRES corresponds now to the bits 18 to 3 of register OUTCONV and therefore the Least Significant Bits and the Full Scale Range are 8 times higher than in case of the divider is not used.

Figure 37:
Relation of the Measurement Result to the Conversion Time with Enabled and Set Divider



7.15 Conversion Time Measurement in SYND Mode

In case of SYND measurement mode the conversion time is fully controlled by the external signal at pin SYN. The relative deviation of this time to the internal clock frequency[2] can produce some deviations in the conversion result. However, this time can be measured in time units of the internal system clock extended up to 24 bits. It gives the opportunity to recalculate the measured input light more precisely (see chapter “Transfer Function”). Even further, the measurement result can be compensated for any deviation, which can occur in the clock frequency due to temperature or supply

[2] The system clock is internally generated and is subject to technological tolerances, which means that clock frequencies of different devices may vary

voltage variations. The conversion time measurement can be enabled by setting bit CREG2:EN_TM bit to ‚1' (see Figure 49). At the end of the conversion the result is stored into the output register OUTCONV (see Figure 53) synchronously with the measurement results (MRES). The stored value follows the relation:

Equation 5:

$$OUTCONV = T_{CONV} \bullet f_{CLK}$$

The bit STATUS:OUTCONVOF of the status register (see Figure 54) shows an overflow of the conversion time counter OUTCONV. In case it happens and the conversion is still in process, the counter OUTCONV starts again at 0. For the calculation of the full scale range (FSR) see formula 1, 2 and 3 in chapter “Transfer function.

7.16 Temperature Measurement

Additional to the three optical channels a temperature measurement is done in parallel. The measurement result is available as TEMP of the output result registers. The resolution of the temperature measurement is 12 bits by a step size of 0.05

K per bit, which means 20 counts per Kelvin. The value of the chip temperature (silicon – measured in °C) is equal to:

Equation 6:

$$T_{CHIP} = TEMP \bullet 0.05°C - 66.9°C$$

With other words TEMP = 922h (2338dec) corresponds to 50°C as a reference point to start calculations.

The temperature measurement is available in the measurement modes CONT, CMD and SYNS. By values of CREG1:TIME < 2dec the resolution of the temperature measurement is reduced, but in this case the output value of TEMP is internally corrected.

In the SYND measurement mode it is important to enable the conversion time measurement (CREG2:EN_TM = ‚1') to get any result of the temperature measurement. In addition, the value of output register OUTCONV has to be more than 2^{12} given by the external conversion time at pin SYN!

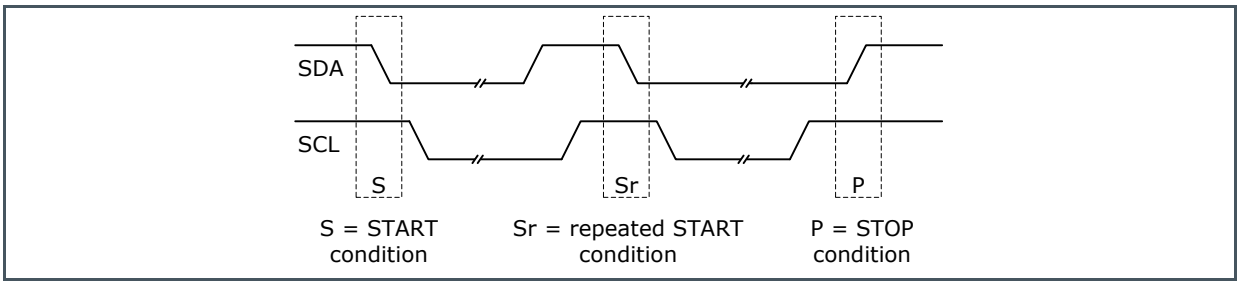
7.17 I²C Communication

The two wire serial interface is compatible to the fast mode I²C protocol with a bit rate up to 400kbit/s. The AS73211 exclusively operates as slave with its slave address [6:0] = (1, 1, 1, 0, 1, A1, A0). The two lowest-order bits are defined by the input pins A1 and A0, which allows to run four AS73211 on the same I²C bus at the same time. Within the AS73211 the pin SCL of the I²C interface is realized as input pin, wherefore in single master applications the I²C master could drive the SCL line with a push-pull stage. In all other cases the requirements for bus termination using standard pull-up according to

I²C (pins SCL and SDA) should be considered, especially regarding to noise environments and EMC in PCB design. For the I²C interface timing diagram and its timing specification please see Figure 7 . Clock stretching is not supported by the AS73211. I²C commands towards AS73211 takes effect after the end of the I²C write cycle (I²C Stop condition).

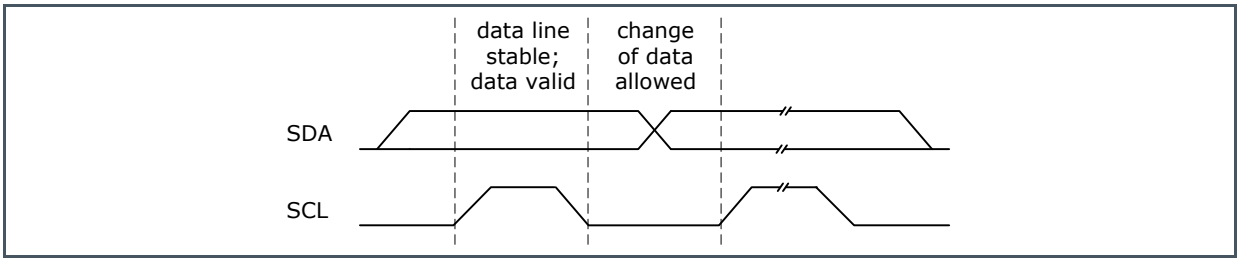
Each data transfer begins with a start (S) condition, defined by a high to low transition of SDA while SCL is high. The transfer is terminated by a stop (P) condition, which is defined by a low to high transition of SDA while SCL is high. A repeated start condition (Sr) can be generated instead of a stop condition, if the transfer should be continued with a new data block. The start and repeated start condition are functionally equivalent.

Figure 38:
Start and Stop Conditions of the I²C Bus



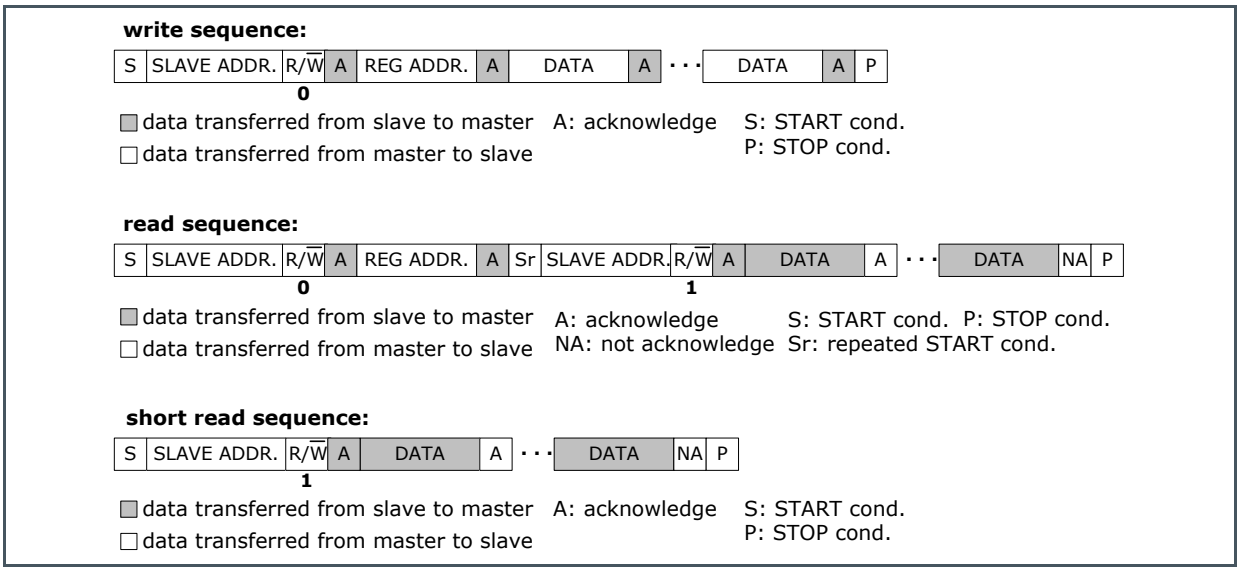
After the protocol started, the data at pin SDA must be stable as long as the high phase of I²C clock at pin SCL takes. The change of the communication data at pin SDA is only allowed during the low phase of SCL clock.

Figure 39:
Bit – Transfer on I²C Bus



Each data transfer consists of 1 byte, which has to be followed by an acknowledge bit (A) (see Figure 40). The bits arrive with the MSB first. The acknowledge signal shall be pulled low by the receiver during the high period of the ninth clock pulse while the transmitter releases the SDA line. When SDA stays high during the ninth clock pulse the not acknowledge signal (NA) is output. After the not acknowledge signal the master generates either a stop or a repeated start condition depending on whether the master either wants to abort or start a new transfer. In case of the AS73211 as slave a not acknowledge (NA) is only generated if the device address did not match.

Figure 40:
I²C Write and Read Sequences



7.18 I²C Write Protocol

The start byte consists of the slave address followed by the bit R/W set to ‚0' for the write direction. The first byte after the start byte is always the device (see Figure 43) sends the address pointer to the internal register, which the master wants to write and acknowledge. When the master sends the next byte, it is stored in the internal register addressed before by the address pointer (REG ADDR.). Then acknowledge is sent by the device and it internally increments the address pointer to the next internal register address. Each next data byte, which is transferred by the master, is sequentially stored in the internal register.

If the master generates a stop condition, the transfer is aborted and a new write sequence must be started from the beginning.

7.19 I²C Read Protocol

The start byte consists of the slave address followed by the bit R/W set to ‚0' for the write direction. The first byte after the start byte is always the device (see Figure 40) sends the address pointer to the internal register, which the master wants to read and acknowledge. After that, the master sends a repeated start condition and repeats the slave address but with the bit R/W reversed. Acknowledge is sent by the slave, which starts the data transfer to the master. The first transferred byte is the content of the internal register, which was pointed by the address pointer. The master acknowledges each transferred byte. The internal address pointer of the AS73211 automatically increments after each transferred register, which allows a sequentially read out of internal registers. If a not acknowledge occurs from the master it sends the stop condition next and the transfer is finished.

A shortened read sequence is also possible as shown in Figure 52. With the default of the bit OPTREG:INIT_IDX = ‚1‘ (see Figure 52) the internal address pointer starts at register address 2h if Measurement state is activated (OSR:DOS = 011b) and if Configuration state is activated (OSR:DOS = 010b) the internal address pointer starts at register address 0h.

7.20 I²C Addressable Register Space

Figure 41 shows the overview of the internal registers of the AS73211, which can be accessed via I²C interface. The control register bank can only be accessed in the configuration state and the registers are all 8 bits long. The output registers can only be accessed in the measurement state. They are read-only registers and 16 bits long, except OUTCONV, which is 24 bits long.

OUTCONV is separated into two parts to fit into the output register’s structure. OUTCONV_L contains the first lower bytes and OUTCONV_H contains the most significant byte of OUTCONV in the first byte. The second byte is 00h.

The AS73211 transfers the output data registers with the least significant byte first. The output register data transfer can start at any address. If during the sequential data read the highest possible address is achieved (CREG2:EN_TM = ‚0‘: address 4h; CREG2:EN_TM = ‚1‘: address 6h), the internal pointer is reset to the address 2h so that the next transferred data byte corresponds to the low byte of MRES1. However, the maximum number of output data transferred must not exceed a total number of bytes accessible at all (6 bytes if conversion time measurement (CREG2:EN_TM) is not activated otherwise 10 bytes). The register OUTCONV is only available in case of bit CREG2:EN_TM is set to ‚1‘.

Figure 41:
Register Overview

ADDRESS (1) [hex]	ACCESS IN CONFIGURATION STATE		ACCESS IN MEASUREMENT STATE	
	WRITE	READ	WRITE (1 BYTE)	READ (2 BYTES)
0	OSR		OSR	OSR + STATUS
1	–		–	TEMP
2	–	–	–	MRES1 (X)
3	–		–	MRES2 (Y)
4	–		–	MRES3 (Z)
5	–		–	OUTCONV_L (2)
6	CREG1		–	OUTCONV_H (2)
7	CREG2		–	–
8	CREG3		–	–
9	BREAK		–	–
A	EDGES		–	–
B	OPTREG		–	–

(1) The 4 MSB bits of the register address are ignored.
(2) OUTCONV is only available in SYND measurement mode with bit CREG2:EN_TM = ‚1‘. The least significant byte comes first.

7.21 I²C General Procedure to start with the AS73211

After applying the power supply voltage the AS73211 is in the Configuration state, but in Power Down. The User can now set up the device for the application by writing the control registers. The success of the configuration can be proven by reading the control registers.

Before a measurement can be started the state must be changed to the Measurement state. The last three bits (DOS) of the register OSR should be loaded with 011b. Now a conversion can be started with the measurement mode, which is selected by CREG3:MMODE. A falling slope of the output pin READY indicates the start. The rising edge at pin READY signalizes the end of conversion and the measurement results can be read via I²C communication.

If a new configuration should be implemented, the device's state has to be changed to Configuration state. Therefore the value 010b should be written into the bits OSR:DOS. This operation resets all measurement result registers to 00h, while the configuration registers keep their actual values. The new configuration can be done now.

Figure 42:
Example of Addressing the AS73211 to Read the Configuration Registers Starting at Address 0h with "automatically incremented values" After Power-On Reset or Software Reset (OSR:SW_RES)

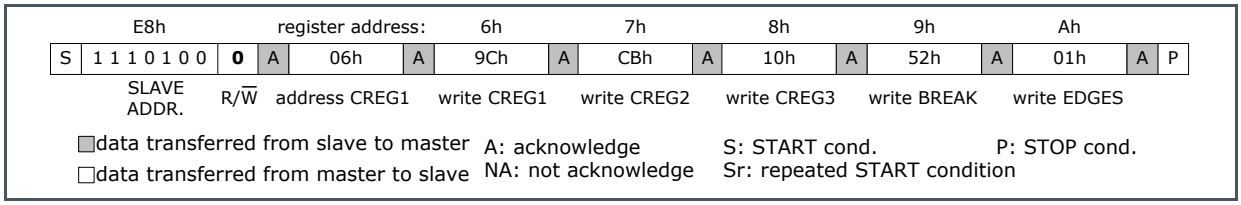
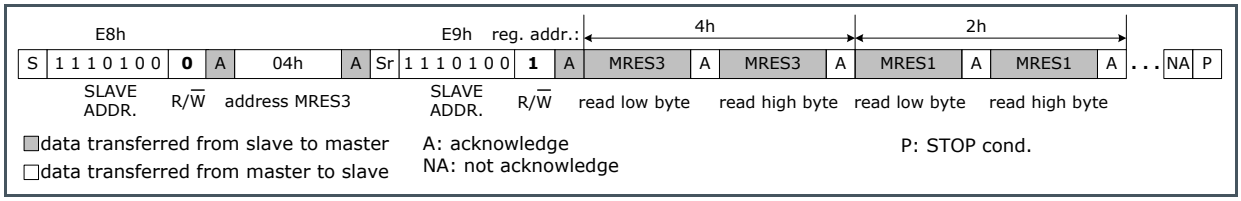


Figure 43:
Example of Addressing the AS73211 to Read the Measurement Result Registers Starting at Address 4h



The access of the result register bank with 2 byte each address (starting with the low byte), which is only possible within the Measurement state, has a special feature (see

Figure 43). Reaching the last valid result register address (4h or 6h if SYND mode is activated with CREG2:EN_TM = ‚1') the next result register address is the default one 2h during read on. The setback to result register address 2h in Measurement mode does not take place if an address was set above the valid addressable space.

8 Register Description

The register contents defined in Figure 44 controls the AS73211 configuration and operational state.

8.1 Register Overview

Figure 44:
Control Register Bank

Address (1) [hex]	Access (2)	Name	Reset Value (3)	Description
0	rw	OSR	42h	Operational State Register
1	-	-	00h (4)	Reserved
2	ro	AGEN	21h	API generation
3	-	-	00h	Reserved
4	-	-	FFh	Reserved
5	-	-	80h	Reserved
6	rw	CREG1	A6h	Configuration register 1
7	rw	CREG2	40h	Configuration register 2
8	rw	CREG3	40h	Configuration register 3
9	rw	BREAK	19h	Break time after measurement
A	rw	EDGES	01h	Edge count value in SYND mode
B	rw	OPTREG	73h	Options register

(1) The 4 MSB bit of the register address are ignored.
(2) ro: read-only, wo: write-only, rw: read-write
(3) Default value after power-on reset and software reset.
(4) Default value after power-on reset and software reset, but different, not relevant values after Power Down state is switched off.

8.2 Operational State Register – OSR

The register OSR defines the fundamental function (Device Operational State – DOS) of the AS73211 according to Figure 45. The register's access is possible and necessary in both operational states – configuration and measurement. Here the initializing, wake up, switch to and start of measurement take place.

Figure 45:
Operational State Register (OSR) ¬– Address 0h

OPERATIONAL STATE REGISTER	NAME	VALUE [b]	OPERATIONAL STATE
bit 7	SS	0 (1)	Stop of the measurement
		1	Start of the measurement (only possible with DOS = MEASUREMENT)
bit 6	PD	0	Power Down state switched OFF
		1 (2)	Power Down state switched ON
bit 5 and 4	Reserved (3)		
bit 3 (4)	SW_RES	0 (5)	-
		1	Software reset
bit 2 to 0	**D**evice **O**perational **S**tate (6) (DOS)	00X	NOP (no change of DOS)
		010 (7)	Operational state: **CONFIGURATION**
		011	Operational state: **MEASUREMENT**
		1XX	NOP (no change of DOS)

(1) Default value after power-on reset, software reset and change into Configuration state.
(2) Default value after power-on reset and software reset.
(3) The read value is always 00b as well as the recommended write value.
(4) Bit 3 (SW_RES) is only active during write access, a read access always returns ‚0‘.
(5) Default value after power-on reset and software reset
(6) The OSR result of a register read process always returns 010b or 011b for the DOS bits.
(7) Default value after power-on-reset, software reset or after mode change from measurement mode to configuration mode.

DOS switches the operational state of the AS73211 between configuration and measurement. The configuration state enables the access to the control register bank (Figure 44) and no measurement takes place. The measurement the access to the result registers can only be performed in the measurement state. Then any access to the control register bank (except OSR) is not possible. If the operational state is switched back to the configuration state by DOS = 010b, the control registers keep their values. The measurement result registers are cleared. Any ongoing measurement is stopped immediately. The DOS sequence “NOP” (00Xb or 1XXb) does not change the operational state, but the values of the other written OSR bits are effective.

SW_RES = ‚1‘ causes a software reset of the AS73211. A running measurement is stopped immediately and the AS73211 is set to configuration state. All registers are reset to their initial values. The start of a measurement is controlled by the value of bit SS. This bit is only interpreted in the measurement state.

The Power Down state is controlled by the value of bit PD.

The Power Down takes effect in both operational states: configuration and measurement. If the Power Down state is switched on while the device is in measurement state, the power down is only performed during the breaks between two conversions.

Figure 46:
Examples for Programming the Operational State Registers at Address 0h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
SS	PD	-	-	SW_RES	DOS			Operational State	
0	1	-	-	0	0	1	0	Configuration state (Power Down state switched on)	42h
0	0	-	-	0	0	1	0	Configuration state (Power Down state switched off)	02h
0	0	-	-	0	0	1	1	Measurement state (Power Down state switched off)	03h
1	0	-	-	0	0	1	1	Measurement state and Start of measurement (Power Down state switched off)	83h
1	0	-	-	0	0	0	0	Provided that Measurement state is active – Start of measurement (Power Down state switched off)	80h
0	1	-	-	0	0	1	1	Measurement state (Power Down state switched on)	43h
1	1	-	-	0	0	1	1	Measurement state, Start of measurement and internal startup (“overwrite” of PD = ‚1‘)	C3h
1	1	-	-	0	0	0	0	Provided that Measurement state is active – Start of measurement and internal startup (“overwrite” of PD = ‚1‘)	C0h
(0)	(1)	-	-	1	(0)	(1)	(0)	Software reset	0Ah

8.3 API Generation Register – AGEN

The value of this read only register indicates the generation of the Control Register Bank. The register’s value changes whenever any formal modification is introduced to the Control Register Bank. This case indicates that the Application Programming Interface (API) has been changed. The default value for the AS73211 is 21h.

Figure 47:
API Generation Register (AGEN) – Address 2h

AGEN	NAME	VALUE [b]	DESCRIPTION
bit 7 to 4	DEVID	0010	Device ID number
bit 3 to 0	MUT	0001	Mutation number of Control Register Bank

8.4 Configuration Register - CREG1, CREG2 and CREG3

CREG1:GAIN determines the irradiance responsivity of the sensor, which is different regarding to the channels X, Y and Z and in each case regarding to the used wave length λ. Internally the A/D converter runs with different gain factors concerning to the bit CREG1:GAIN (see also Figure 35).

CREG1:TIME controls the conversion time duration as a multiple of the internal clock periods. In case of the start and end of a measurement are controlled externally via input trigger signal at pin SYN (equal to SYND mode), CREG1:TIME has no influence to the conversion time.

In general the registers CREG2 and CREG3 define the measurement modes and additional device specific options.

Figure 48:
Configuration Register 1 (CREG1) – Address 6h

CREG1	NAME	VALUE [b]	CONFIGURATION		
bit 7 to 4	GAIN		INDEX X-channel λ = 0nm Y-channel λ = 555nm Z-channel λ = 445nm	CREG1:TIME = 1010b (1024ms) CREG3:CCLK = 00b (1MHz) Full Scale Range of detectable irradiance E_e [µW/cm²]	Effective Least Significant Bit (LSB) of Full Scale Range [nW/cm²]
		0000	$GAIN_X$ = 2048x	0.866	0.0132
			$GAIN_Y$ = 2048x	0.932	0.0142
			$GAIN_Z$ = 2048x	0.501	0.0076
		0001	$GAIN_X$ = 1024x	1.732	0.0264
			$GAIN_Y$ = 1024x	1.865	0.0285
			$GAIN_Z$ = 1024x	1.002	0.0153
		0010	$GAIN_X$ = 512x	3.463	0.0528
			$GAIN_Y$ = 512x	3.730	0.0569
			$GAIN_Z$ = 512x	2.003	0.0306
		0011	$GAIN_X$ = 256x	6.927	0.1057
			$GAIN_Y$ = 256x	7.460	0.1138
			$GAIN_Z$ = 256x	4.006	0.0611
		0100	$GAIN_X$ = 128x	13.854	0.2114
			$GAIN_Y$ = 128x	14.919	0.2276
			$GAIN_Z$ = 128x	8.012	0.1223
		0101	$GAIN_X$ = 64x	27.707	0.4228
			$GAIN_Y$ = 64x	29.838	0.4552
			$GAIN_Z$ = 64x	16.024	0.2445
		0110	$GAIN_X$ = 32x	55.414	0.8456
			$GAIN_Y$ = 32x	59.677	0.9106
			$GAIN_Z$ = 32x	32.048	0.4890

CREG1	NAME	VALUE [b]	CONFIGURATION			
		0111	$GAIN_X$ = 16x	110.828	1.6911	
			$GAIN_Y$ = 16x	119.354	1.8212	
			$GAIN_Z$ = 16x	64.097	0.9780	
		1000	$GAIN_X$ = 8x	221.657	3.3822	
			$GAIN_Y$ = 8x	238.707	3.6424	
			$GAIN_Z$ = 8x	128.194	1.9561	
		1001	$GAIN_X$ = 4x	443.314	6.7644	
			$GAIN_Y$ = 4x	477.415	7.2848	
			$GAIN_Z$ = 4x	256.387	3.9122	
		1010 (1)	$GAIN_X$ = 2x	886.628	13.5289	
			$GAIN_Y$ = 2x	954.830	14.5695	
			$GAIN_Z$ = 2x	512.774	7.8243	
		1011	$GAIN_X$ = 1x	1773.255	27.0577	
			$GAIN_Y$ = 1x	1909.659	29.1391	
			$GAIN_Z$ = 1x	1025.548	15.6486	
bit 3 to 0	TIME		VALUE [dec]	Conversion Time (f_{CLK} = 1.024MHz)		
				T_{CONV} [ms]	Number of clocks	
		0000	0	1	1024	2^{10}
		0001	1	2	2048	2^{11}
		0010	2	4	4096	2^{12}
		0011	3	8	8192	2^{13}
		0100	4	16	16384	2^{14}
		0101	5	32	32768	2^{15}
		0110 (1)	6	64	65536	2^{16}
		0111	7	128	131072	2^{17}
		1000	8	256	262144	2^{18}
		1001	9	512	524288	2^{19}
		1010	10	1024	1048576	2^{20}
		1011	11	2048	2097152	2^{21}
		1100	12	4096	4194304	2^{22}
		1101	13	8192	8388608	2^{23}
		1110	14	16384	16777216	2^{24}
		1111	15	1	1024	2^{10}

(1) Default value after power-on reset and software reset.

Figure 49:
Configuration Register 2 (CREG2) – Address 7h

CREG2	NAME	VALUE [b]	CONFIGURATION
bit 7	Reserved (1)		
bit 6	EN_TM	0	In combination with SYND mode the internal measurement of the conversion time is disabled and no temperature measurement takes place.
		1 (2)	Internal measurement of the externally defined conversion time via SYN pulse in SYND mode is enabled (OUTCONV results are generated as well as temperature values for output register TEMP).
bit 5 to 4	Reserved (1)		
bit 3	EN_DIV	0 (2)	Digital divider of the measurement result registers is disabled
		1	Digital divider of the measurement result registers is enabled (might be needed @ CREG1:TIME > 6 dec)
bit 2 to 0	DIV		Value of the divider ($2^{1+DIV[dec]}$)
		000 (2)	2^1
		001	2^2
		010	2^3
		011	2^4
		100	2^5
		101	2^6
		110	2^7
		111	2^8

(1) The default value after power-on reset and software reset is ‚0' as well as the recommended write value.
(2) Default value after power-on reset and software reset.

In SYND mode, the conversion time is externally controlled via pin SYN. In that case the bit CREG2:EN_TM enables the counting of internal clocks within the external given conversion time as well as the access to the output register OUTCONV, which contains the counting result. It is possible to count a number of clocks up to 24 bits. In case of this function is not used in SYND mode (equal to CREG2:EN_TM = ‚0') no result for temperature measurement is generated. The values for output register TEMP are not valid.

The bit CREG2:EN_DIV enables the internal prescaler, which could be interesting for conversion times more than 16 bits (CREG1:TIME ≥ 0111b) and in case of SYND mode is used. The value of CREG2:DIV is only valid with CREG2:EN_DIV = ‚1'. Then the measurement range is extended while the resolution of the 16-bit register results is reduced at the same time (see Divider). Thus it is also possible to generate complete measurement results for conversion times from 2^{17} to 2^{24} system clocks (CREG1:TIME). If the chosen value of the prescaler is too small, a counter overflow could occur, which is shown by the bit STATUS:MRESOF of the result register bank.

Figure 50:
Configuration Register 3 (CREG3) – Address 8h

CREG3	NAME	VALUE [b]	CONFIGURATION
bit 7 to 6	MMODE	00	CONT mode (continuous measurement)
		01 (1)	CMD mode (measurement per command)
		10	SYNS mode (externally synchronized start of measurement)
		11	SYND mode (start and end of measurement are externally synchronized)
bit 5	Reserved (2)		
bit 4	SB	0 (1)	Standby is switched OFF
		1	Standby is switched ON
bit 3	RDYOD	0 (1)	Pin READY operates as Push Pull output
		1	Pin READY operates as Open Drain output
bit 2	Reserved (2)		
bit 1 to 0	CCLK	00 (1)	Internal clock frequency f_{CLK} = 1.024MHz
		01	Internal clock frequency f_{CLK} = 2.048MHz
		10	Internal clock frequency f_{CLK} = 4.096MHz
		11	Internal clock frequency f_{CLK} = 8.192MHz

(1) Default value after power-on reset and software reset.
(2) The default value after power-on reset and software reset is ‚0' as well as the recommended write value.

The bits CREG3:MMODE specify the measurement mode, which should be compatible to the given application.

The bit CREG3:SB controls the operational state Standby of the AS73211. Within Standby state the power consumption of the device is reduced, but the internal circuit is ready to continue after 4 µs wake-up time by switching off Standby.

With bit CREG3:RDYOD the output pin READY can be changed from push pull to open drain behavior. The open drain output allows running two or more AS73211 at the same time connected to one READY line with pull-up resistor. As long as one device still measures, the READY line is low active.

The internal clock frequency f_{CLK} is controlled by the bits of CREG3:CCLK. Higher clock rates result in shorter conversion times for the measurement. But take care of CREG1:GAIN – with higher frequencies than 1 MHz in some cases the irradiance responsivity is reduced (see Figure 35).

8.5 Register – BREAK

The register BREAK defines the time between two consecutive measurements of CONT, SYNS and SYND mode. The default value of register BREAK is 19h. The value 0h results in a minimum time of three clocks of f_{CLK}.

Figure 51:
Register BREAK – Address 9h

BREAK	NAME	VALUE [dec]	DESCRIPTION
bit 7 to 0	BREAK	0 to 255 (25) (1)	Pause time T_{BREAK} between two measurements (except CMD mode): from 0 (2) to 2040 µs, step size 8 µs

(1) Default value after power-on reset and software reset.
(2) The value 0h results in a minimum time of 3 clocks of f_{CLK}.

8.6 Register – EDGES

The register EDGES becomes operative in SYND mode. After a measurement was started in SYND mode it defines the necessary number of additional falling edges at input SYN until the conversion is terminated. The value EDGES = ‚0‘ is not allowed and results in the initial value ‚1’.

8.7 Register – OPTREG

The register bit OPTREG:INIT_IDX allows to communicate via I²C with simple masters, which do not support the I²C Repeated START condition. In this case the start address for a read operation can only be set by a complete write access with I²C STOP condition at the end. For this kind of simple I²C masters the bit INIT_IDX has to be ‚0‘. Reading of data starts then at the given index address. After each data transfer the index address is incremented.

With INIT_IDX set to ‚1‘ each short read operation starts at the default address 2h in Measurement mode and 0h in Configuration mode. The setting of the internal read index address by writing to a register address followed by I²C Repeated START condition works as usual. After each data transfer the index address is incremented. Please see also chapter “I²C Read Protocol”.

Figure 52:
Register OPTREG – Address Bh

OPTREG	NAME	VALUE [b]	N
bit 7 to 1	-	0111001 (1)	Reserved
bit 0	INIT_IDX	0	Defining the index address is only possible via write sequence and not affected by I²C STOP condition, which is necessary, if the I²C master does not support the I²C Repeated START condition.
		1 (2)	Each I²C STOP condition sets the internal register address to the default value. After writing an index address, it is possible to change the data direction for reading using I²C Repeated START condition.

(1) Default value after power-on reset and software reset, but different, not relevant values after changing CREG1:GAIN or CREG3:CCLK. The recommended write value is 0000000b in case of OPTREG:INIT_IDX should be changed.
(2) Default value after power-on reset and software reset.

8.8 Output Register Bank

All output result registers are 16-bit registers. The registers read access is only possible if state Measurement is activated. One exception offers register OSR, which is writable too. In that case one byte is assigned to address 0h (see also chapter “Operational State Register – OSR”). But the reading access of address 0h in Measurement state results in a first byte for OSR information and a second byte for STATUS information.

Figure 53:
Output Result Register Bank

ADDRESS(1) [hex]	ACCESS(2)	NAME	NUMBER OF BITS	DESCRIPTION
0	rw	OSR	8 (1)	Operational State Register
	ro	STATUS	8 (1)	Status Register
1	ro	TEMP	16 (2)	Temperature Measurement Result (0h + 12bits for the value)
2	ro	MRES1	16 (2)	Measurement Result X-Channel
3	ro	MRES2	16 (2)	Measurement Result Y-Channel
4	ro	MRES3	16 (2)	Measurement Result Z-Channel
5	ro	OUTCONVL	16 (2)	Time reference, result of conversion time measurement (least significant byte and middle byte)
6	ro	OUTCONVH	16 (2)	Time reference, result of conversion time measurement (most significant byte and one empty byte with 00h)

(1) Reading access of address 0h in measurement state results in a first byte for OSR information and a second byte for STATUS information.
(2) Least Significant Byte comes first.

Figure 54:
Status Register (STATUS) – Address 0h

BREAK	NAME	DESCRIPTION
7	OUTCONVOF (1)(2)	Digital overflow of the internal 24 bit time reference OUTCONV
6	MRESOF(2)	Overflow of at least one of the measurement result registers MRES1 … MRES3
5	ADCOF(2)	Overflow of at least one of the internal conversion channels during the measurement (e.g. caused by pulsed light) – analog evaluation is made
4	LDATA (3)	Measurement results in the buffer registers were overwritten before they were transferred to the output result registers. A transfer takes place as part of an I²C read process of at least one register of the output register bank.
3	NDATA (4)	New measurement results were transferred from the temporary storage to the output result registers.
2	NOTREADY	‚0': Measurement process is finished or not yet started ‚1': Measurement is in progress (corresponds to the inverted signal at output pin READY)
1	STANDBYSTATE	‚0': Standby state is switched OFF ‚1': Standby state is switched ON
0	POWERSTATE	‚0': Power Down state is switched OFF ‚1': Power Down state is switched ON

(1) Overflow of the internal 24-bit conversion time counter – only possible in SYND mode with externally synchronized start and stop of conversion.
(2) The status flag is generated while a measurement is in progress. It always matches to the actual results of the output register bank.
(3) A reading process of the register STATUS always resets this status flag.
(4) A reading process of the register STATUS and/or at least one result register always resets this status flag.

The bit STATUS:OUTCONVOF shows an overflow of the 24 bit counter of the internal reference for the conversion time. This can only occur in SYND mode with CREG2:EN_TM = ‚1' and in case of accordingly long externally given conversion times. After a counter overflow the counter starts again from zero.

The bit STATUS:MRESOF shows an overflow in one or more result registers of MRES1 … MRES3. This can only happen if the conversion time is longer than 2^{16} (CREG1:TIME = 7…15 dec) in accordance with a higher input signal. The overflowed register stops at its maximum value FFFFh.

With the bit STATUS:ADCOF an input signal overdriving is signalized, which could occur during the measurement cycle limited in time, so that no overflow of the result registers (MRESOF) is necessarily produced. But the measurement results are not correct in this case. To eliminate this problem the irradiance responsivity R_e of the sensor has to be decreased via CREG1:GAIN.

The status bits OUTCONVOF, MRESOF and ADCOF always correspond to the actual content of the measurement result registers MRES1…3.

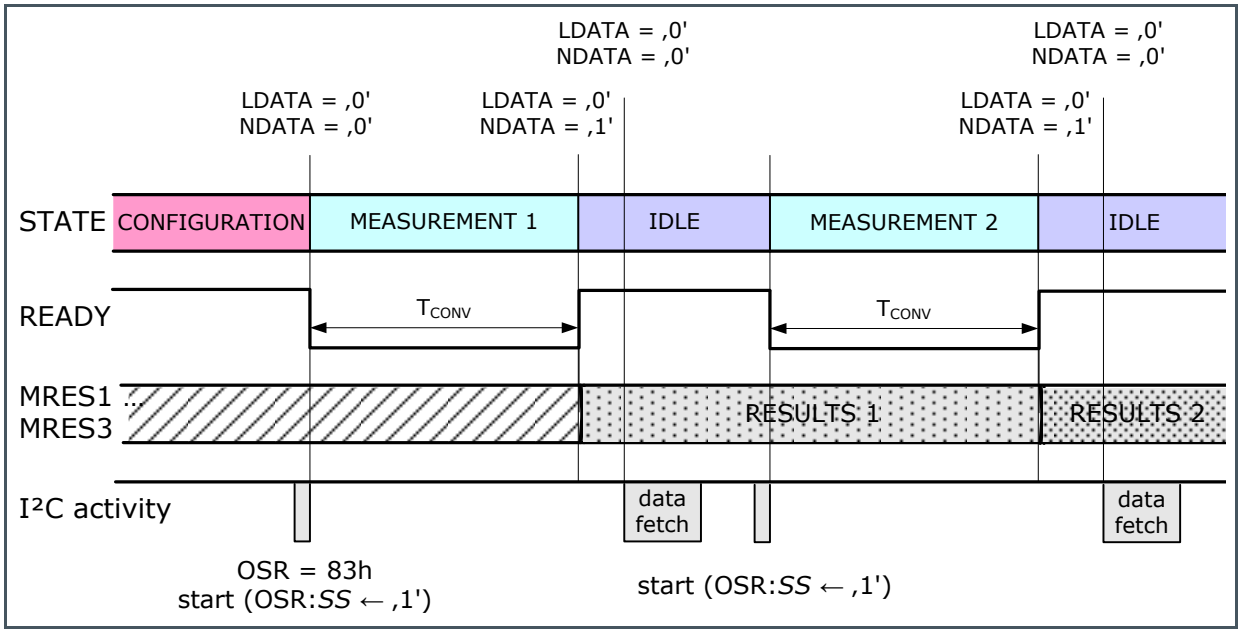
The bits STATUS:LDATA and STATUS:NDATA show the status of the measurement results. At the end of each measurement cycle, the results of the counters are stored into buffer registers. The flag

NDATA is set to ‚1' to show the update (see Figure 55). With the start of each I²C read operation the content of all buffer registers is transferred to the result registers. This ensures that during the I²C readout operation the values of the result registers do not change.

As long as an I²C-reading of the measurement result registers is in process (no I²C stop condition has been sent), no further update of the measurement result registers concerning to newer data of the buffer registers will happen.

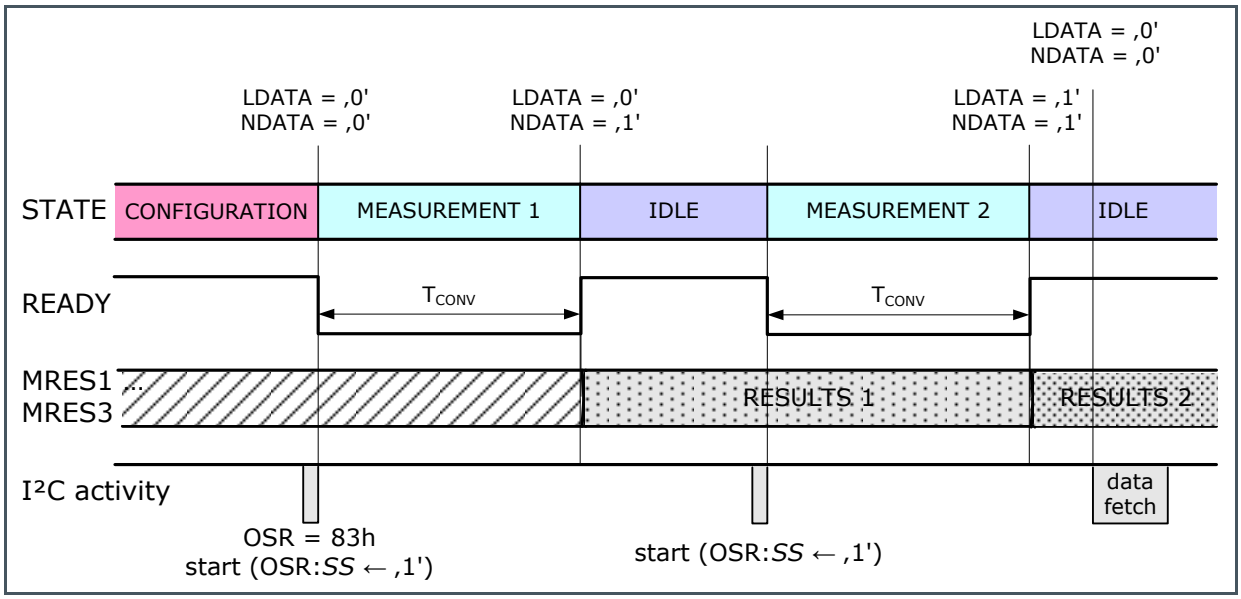
The status bit NDATA is reset to ‚0' after reading the status register or at least one measurement result register.

Figure 55:
Update Time of the Status Register Bits for an Accurate Measurement and Read Behavior



If the buffer registers contain new values (NDATA = ‚1') and then a new measurement finishes before an I²C reading process occurs, the new measurement results is stored in the buffer registers. The older measurement results are overwritten. The status bit LDATA as shown in Figure 56 indicates this. The LDATA bit is only reset to ‚0' by reading the status register, because it allows checking for the loss of information after multiple measurement cycles.

Figure 56:
Update Time of the Status Register Bits, if Some Measurement Results Were Not Picked Up



The status bits STATUS:STANDBYSTATE and STATUS:POWERSTATE always show the actual status of the internal control signals for Standby and Power Down. In both cases it can differ from the actual set bits CREG3:SB and OSR:PD, because of the behavior of the control signals while a measurement is in process. The reading of the 16-bit values of the output result registers always starts with the least significant byte.

The measurement value TEMP at address 1h is a 12-bit value, but its higher 4 bits until 16 are filled up with 0h. For Measurement modes programmed with CREG1:TIME < 2^{12} there is a TEMP result with a lower resolution. If the SYND mode is used and register OUTCONV is set inactive by CREG2:EN_TM = ‚0', any temperature measurement is not possible. In case of CREG2:EN_TM is enabled (‚1') the TEMP value is only valid for conversion times with ≥ 2^{12} internal system clocks f_{CLK} represented by register OUTCONV.

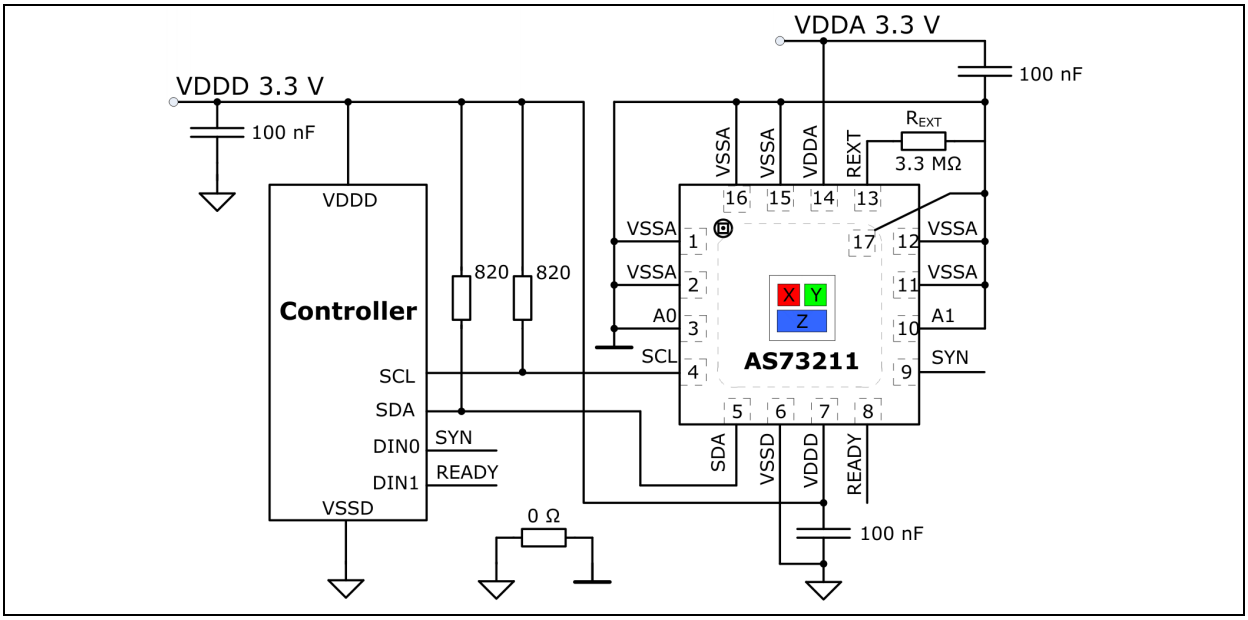
Power-on reset, software-reset or return to Configuration state resets the complete output register bank.

9 Application Information

9.1 Schematic

Figure 57 shows a typical application circuit. Digital and analog grounds should be routed separately onto the printed circuit board and must be connected together near the device. The die attach pad (no. 17) of the QFN16 must be connected to analog ground VSSA. Without this contact it can lead to errors of the sensor.

Figure 57:
Typical Application Circuit



Please make sure that all specified components within the application circuit work according to their operating range and to the parameters in the data sheet. For example, voltage regulators (workspace load current, separated analog and digital or decoupled power supplies based on a common regulator) need special treatment to avoid noise or deviations during operation.

9.2 External Components

The AS73211 and its external components for references and/or power supply (e.g. reference resistor R_{EXT}) should be placed on the same PCB side.

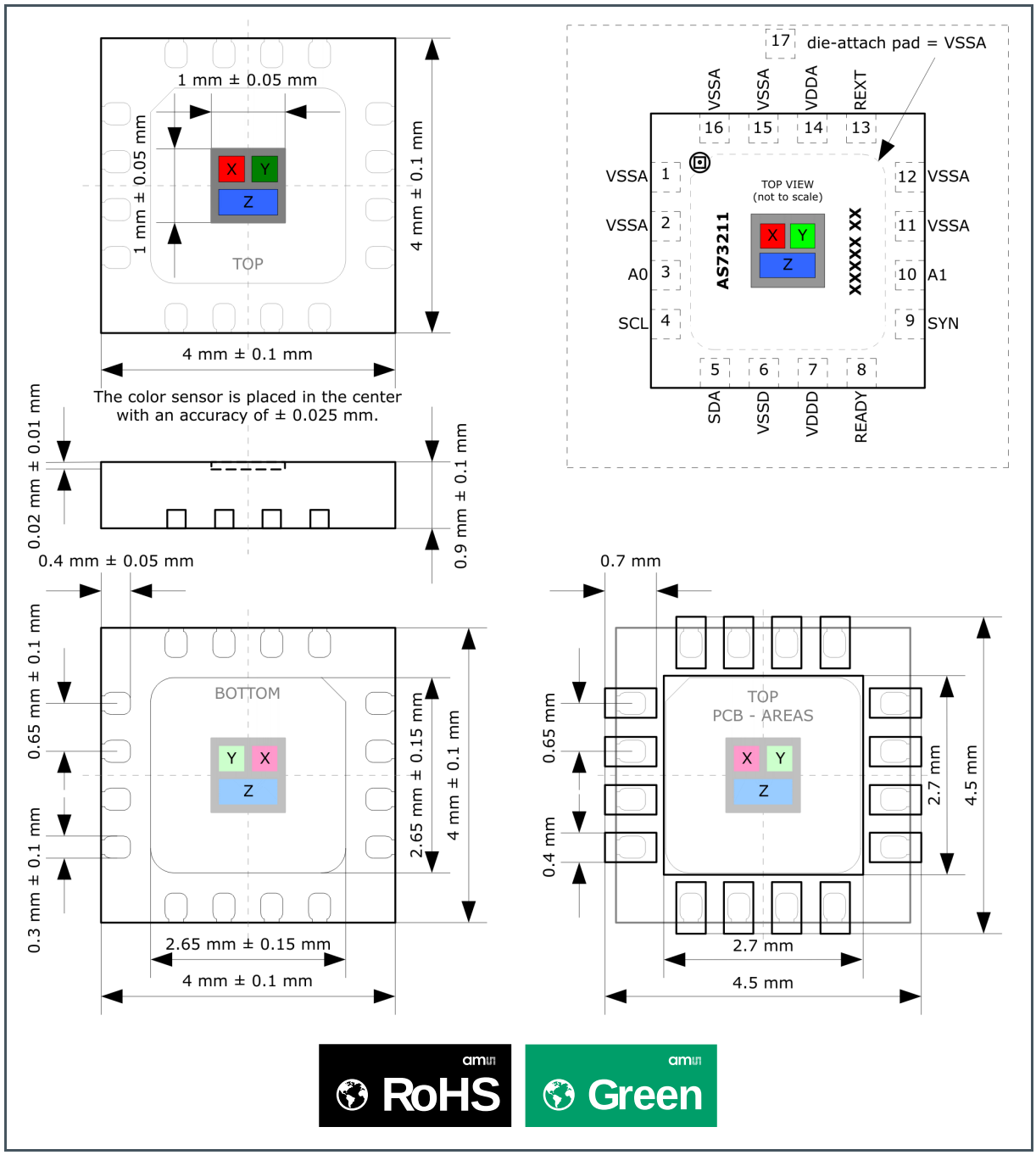
9.3 PCB Layout

The analog supply must be placed as close as possible to the AS73211. The connection between the analog and digital grounds must be beneath (LP level) and/or near the AS73211.

The die-attach pad (exposed pad) of the QFN16 package (AS73211) must be connected to analog ground VSSA.

10 Package Drawings

Figure 58:
Package Outline Drawing QFN16



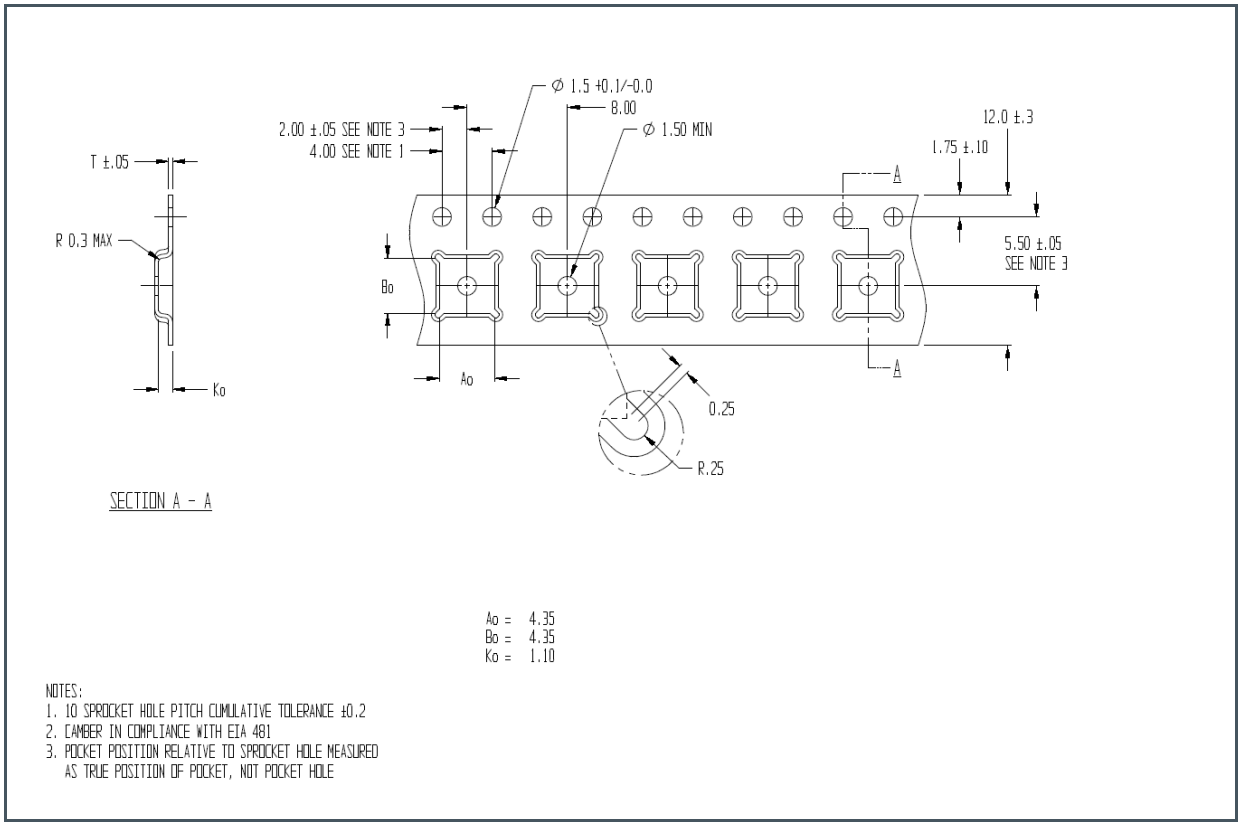
(1) All dimensions are in millimeters. Angles in degrees.
(2) Dimensioning and tolerancing conform to ASME Y14.5M-1994.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

11 Tape & Reel Information

Standard packing is tape and reel. Usually in a moisture barrier bag (MBB sealed aluminized envelope) with desiccant (e.g. silica gel) and humidity indicator card to protect them from ambient moisture during shipping, handling, and storage before use. This package has been assigned a moisture sensitivity level of MSL 3 and the devices should be stored under the following conditions:

- Temperature range 5°C to 50°C
- Relative humidity 60% maximum
- Total time 6 months from the date code on the aluminized envelope – if unopened
- Opening time 168 hours or less

Figure 59:
QFN16 Tape & Reel Dimensions



12 Soldering & Storage Information

The die-attach pad 17 (exposed pad) of the QFN16 package must be connected to analog ground VSSA on PCB. Realize this before soldering by a conductive adhesive and bonding this pad of the sensor backside to a ground pad on the PCB.

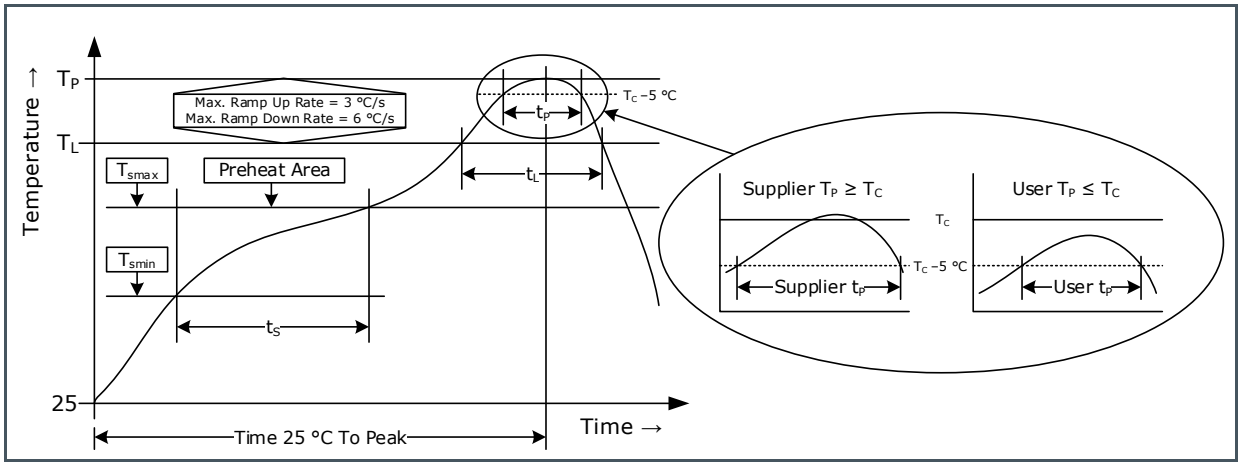
According to the JEDEC standard, the QFN16 package has been tested and has demonstrated the ability to be reflow-soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The component should be limited to a maximum of three passes through this solder reflow profile.

Figure 60:
Profile Features According to JEDEC

	IPC/JEDEC J-STD-020D.1 (Pb-Free)	RECOMMENDED DATA
Time [s] from 150°C to 200°C (preheat)	60 – 120	100
Average ramp-up rate [°C/s]	maximum 3.0	0.5 – 1.0
Liquidus temperature [°C]	217	217
Peak package body temperature [°C]	maximum 260	≤ 260
Time [s] within 5°C of the classification	minimum 30	35 – 45
Average ramp-down rate [°C/s] (peak	maximum 6.0	3.0
Time [s] from 25°C to peak temperature	maximum 480	350

Do not exceed the recommended values shown in the table or following figure. For further information, see the JEDEC standard J-STD-020D.1.

Figure 61:
Solder Reflow Profile Graph



13 Application Notes

13.1 Narrowband Luminous Sources

The spectral filters of the color sensors are specialized for applications with broadband source of lighting >10nm. Please ask our sales team before utilizing our sensor in combination with narrowband luminous sources.

13.2 Angle of Incidence

The packaging of the sensor IC has an aperture angle (beam width) of nearly 90°. Traditional interference filter work depending on angle of incidence. Using an angle of incidence < 10° allows the best results with no filter shifts. This can be ensured by using lenses or optical holes that limit the angle of incidence to the sensor device < 10°. An angle of incidence of more than 10° results in a filter shift. The filter response and accuracy is distorted the greater the angle deviation is. Please note a filter deviation resulting from this fact can differ from standard observer function and/or from the filter functions specified in this document. Please ask our sales team for support.

13.3 Effects of Temperature

The specified operation temperature range and documented parameters regarding temperature influence are described in chapter “Absolute Maximum Ratings”. The functionality of the filters do not depend on any temperature changes. The temperature coefficient of the photo sensitivity and the dark current of the photodiodes need to be considered, since these have an influence on the sensor’s response in case of changing temperature.

13.4 Notes for Manufacturing

JENCOLOR® sensors are optoelectronic components operating at high precision, resolution and smallest currents of nA in operation and pA in standby. This must be considered in the development and manufacturing. So mechanical stress, EMC, dirt and moisture must be avoided.

For manufacturing purposes we recommend completely removing moisture and dirtying (dirt and residue solder as solder) on the boards with JENCOLOR® sensors. This refers to residual moisture on / below the sensor and converter. In sensor operations residual moisture or residues of solder can lead to leakage currents and result in increased offset values. Offset means a lower resolution, lower accuracy and measuring inaccuracies in sensor mode. These have particular impact on small measurement signals from the sensor. If cleaning of a PCB with water is necessary then make sure to fully dry the board later on with suitable processes and technologies (e.g. baking 120°C, over 24h). This avoids residual moisture as reason for leakage currents and noise.

13.5 Sensor Calibration

Since the main variables of color change upon the arrangement of the observer, the object and light - it is essential to optimize and calibrate color measurement tasks to the specific application, especially for absolute color measurements according to the CIE 1931/DIN 5033.The calibration has three functions. It converts the measured values from light-to-digital converter into the color space XYZ/xyY/Luv/Lab or others. Secondly, it compensates production-related tolerances of the individual sensors. Thirdly, the accuracy of the XYZ sensor is extremely sensitive to the opto-mechanical design and variations of the system in, which it resides. These influences need to be corrected as other (e.g. external) effects like temperatures or others can influence other components in the sensor system and therefore the overall sensor response. Depending on the application and system accuracy, a sensor calibration will be possible by an individual system or by an in-series calibration. In the process of calibration there are conditions, which are required to receive reliable results in the CIE 1931 color space. Using a standardized illumination source such as A, F2 and D65 as reference, the angle of incidence as well as the arrangement of sensor and illumination are important input variables of the calibration and determine the quality of the XYZ transformation. ams Sensors Germany offers special white papers and application notes to find an optimized application-specific solution (time, costs and quality) for calibration. Please ask our sales team.

For calibration the (color) target, measured by a spectrometer (n * XYZ as absolute color values and reference) and the color sensor (n * ADC measured) must be known. By a simple coefficient matrix method the relationship between the measured sensors values and absolute color coordinates in CIE 1931 color space can be made: T (1) is the matrix of the reference measurement (XYZ values of spectrometer), S (EQ1) is the sensor signal matrix (ADC values of Sensor) and K is the transformation matrix (EQ2). After the transposition of S, a transformation matrix K (linear regression) is calculated (EQ2). The result (EQ3) is the correction matrix K, which is used to transform measured sensor values (ADC result of a color target) into the color space XYZ based in CIE 1931 (EQ4).

Information

Matrixes are not set up as a square matrix and depend on the number of targets n.

Equation 7:

$$T = \begin{pmatrix} X_1 & X_2 & X_n \\ Y_1 & Y_2 & \dots Y_n \\ Z_1 & Z_2 & Z_n \end{pmatrix}; \quad S = \begin{pmatrix} adcX_1 & adcX_2 & adcX_n \\ adcY_1 & adcY_2 & \dots adcY_n \\ adcZ_1 & adcZ_2 & adcZ_n \end{pmatrix}$$

Equation 8:

$$K = \left(T \bullet S^T\right) \bullet \left(S \bullet S^T\right)^{-1}$$

Equation 9:

$$K = \begin{pmatrix} xk_1 & xk_2 & xk_3 \\ yk_1 & yk_2 & yk_3 \\ zk_1 & yk_2 & zk_3 \end{pmatrix}$$

Equation 10:

$$\begin{pmatrix} X_{SENSOR} \\ Y_{SENSOR} \\ Z_{SENSOR} \end{pmatrix} = K \bullet \begin{pmatrix} adcX \\ adcY \\ adcZ \end{pmatrix}$$

XSENSOR, YSENSOR, and ZSENSOR are the corrected sensor values in the CIE system, which specifies the color and brightness of particular homogenous visual stimulus. adcX, adcY, adcZ are measured values of the sensor. Xn, Yn, Zn are by a spectrometer measured color coordinates of the target for the calibration. xk…, yk…, zk… are coefficients of the correction matrix.

14 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Changes from previous version to current revision v3-01	Page
Datasheet was updated to latest **ams** design	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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