TPS2358 Dual-Slot ATCA AdvancedMC™ Controller

Check for Samples: TPS2358

FEATURES

- **ATCA AdvancedMC™ Compliant**
- **Full Power Control for Two AdvancedMC™Modules**
- **Independent 12-V Current Limit and Fast Trip**
- **12-V FET ORing for MicroTCA™**
- **Internal 3.3-V Current Limit**
- **Power Good and Fault Outputs**
- **48-Pin PQFN Package**
- **Latch Off After Fault**

APPLICATIONS

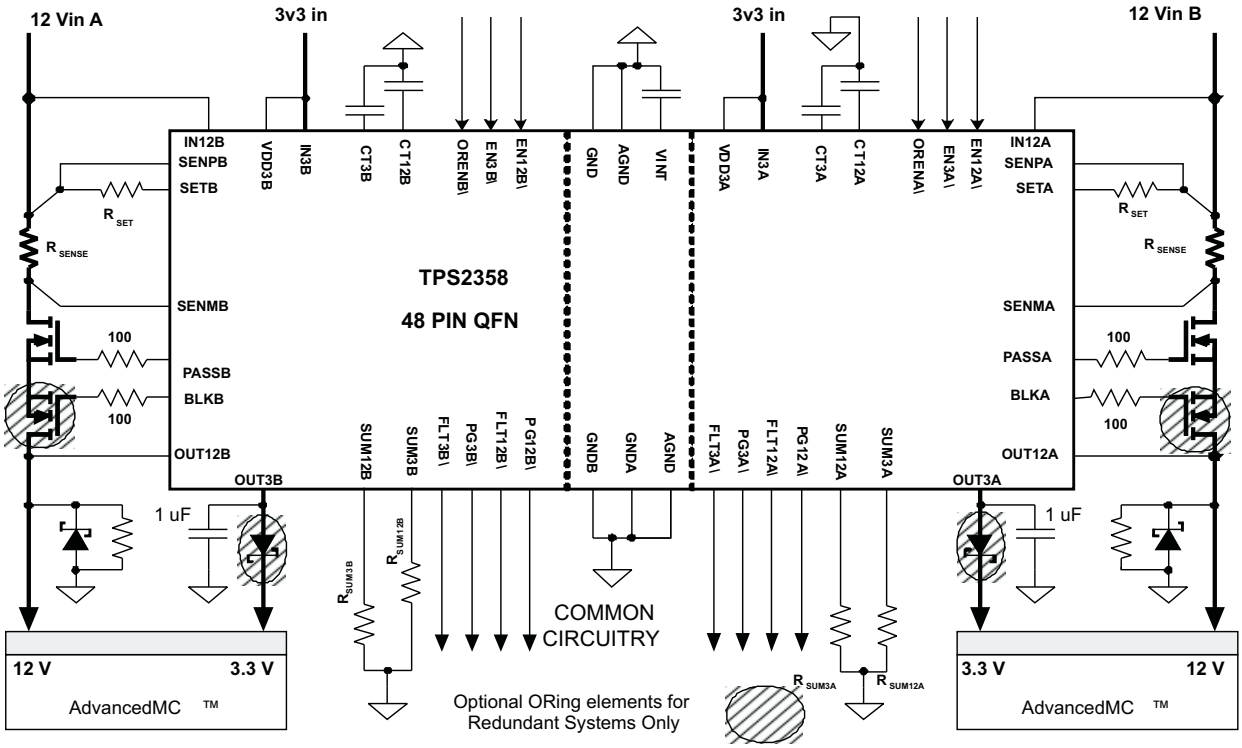
- **ATCA Carrier Boards**
- **MicroTCA™ Power Modules**
- **AdvancedMC™ Slots**
- **Systems Using 12 V and 3.3 V**
- **Base Stations**

DESCRIPTION

The TPS2358 dual-slot hot-plug controller provides all required power interface functions for two AdvancedMC™ (Advanced Mezzanine Card) modules.

Two fully integrated 3.3-V channels provide inrush control, current limiting, and overload protection. The two 12-V channels use an external FET to provide the same functions, along with ORing control circuits that allow an external FET to prevent reverse current flow. External capacitors are used to set fault times. There is one capacitor for each channel. The 3.3-V current limits are factory set to AdvancedMC™ compliant levels and the 12-V current limits are programmed using external sense resistors. The accurate current sense comparators of the TPS2358 satisfy the narrow ATCA AdvancedMC™ current limit requirements.

TYPICAL APPLICATION DIAGRAM



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION(1)

DEVICE	TEMPERATURE	PACKAGE(2)	ORDERING CODE
TPS2358	-40°C to 85°C	QFN48	TPS2358RGZ

(1) Add an R suffix to the device type for tape and reel.
(2) For the most current package and ordering information see the Package Option Addendum at the end of this document or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, all voltages referenced to GND (unless otherwise noted).

PARAMETER	VALUE	Unit
PASSx, BLKx	–0.3 to 30	V
IN12x, OUT12x, SENPx, SENMx, SETx, $\overline{EN12x}$, $\overline{FLTx}$, $\overline{PGx}$, $\overline{ORENx}$	–0.3 to 17	
IN3x, OUT3x, $\overline{EN3x}$, VDDx, CTx, SUMx	–0.3 to 5	
AGND, GNDx	–0.3 to 0.3	
$\overline{FLTx}$, $\overline{PGx}$	5	mA
SUMx	5	
VINT	–1 to 1	
OUT3x	Internally limited	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device under any conditions beyond those indicated under recommended operating conditions is neither implied nor guaranteed. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

TEST METHOD	MIN	UNITS
Human Body Model (HBM)	2	kV
Charged Device Model (CDM)	0.5	

DISSIPATION RATINGS

PACKAGE	θ_{JA} - High-k (°C/W)
QFN48 - RGZ	29.1

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNITS
V_{IN12x}	12-V input supply	8.5	12	15	V
V_{IN3x}	3.3-V input supply	3	3.3	4	
V_{VDD3x}	3.3-V input supply	3	3.3	4	
I_{OUT3x}	3.3-V output current			165	mA
I_{SUMx}	Summing pin current		100	1000	µA
	PASSx pin board leakage current	-1		1	
	VINT bypass capacitance	1	10	250	nF
T_J	Operating junction temperature range	–40		125	°C

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ELECTRICAL CHARACTERISTICS

IN3A = IN3B = VDD3A = VDD3B = 3.3 V. IN12A = IN12B = SENPA = SENPB = SENMA = SENMB = SETPA = SETPB = 12 V. $\overline{EN12A}$ = $\overline{EN12B}$ = $\overline{EN3A}$ = $\overline{EN3B}$ = $\overline{ORENA}$ = $\overline{ORENB}$ = CT12A = CT12B = CT3A = CT3B = AGND = GNDA = GNDB = 0 V. SUM12A = SUM12B = 6.8 kΩ to ground. SUM3A = SUM3B = 3.3 kΩ to ground. All other pins open. Over free air temperature operating range and all voltages referenced to AGND, -40°C ≤ T_A ≤ 85°C, typical vales at 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE Inputs					
Threshold voltage, falling edge		1.2	1.3	1.4	V
Hysteresis		20	50	80	mV
Pullup current	$\overline{ENx}$ = $\overline{ORENx}$ = 0 V	5	8	15	μA
Input bias current	$\overline{EN12x}$ = $\overline{ORENx}$ = 17 V		6	15	
Input bias current	$\overline{EN3x}$ = 5 V		1	5	
3.3-V turn off time	$\overline{EN3x}$ deasserts to V_{OUT3x} < 1.0 V, C_{OUT} = 0 μF			10	μs
12-V turn off time	$\overline{EN12x}$ deasserts to V_{OUT12x} < 1.0 V, C_{OUT} = 0 μF, Q_{GATE} = 35 nF			20	
POWER GOOD Outputs					
Low voltage	Sinking 2 mA		0.14	0.25	V
Leakage current	$\overline{PGx}$ = 17 V			1	μA
Threshold voltage	$\overline{PG12x}$, falling VOUT12x	10.2	10.5	10.8	V
	$\overline{PG3x}$, falling VOUT3x	2.7	2.8	2.9	
Hysteresis	$\overline{PG12x}$, measured at OUT12x		130		mV
	$\overline{PG3x}$, measured at OUT3x		50		
Deglitch time	$\overline{PGx}$ falling	50	100	150	μs
FAULT Outputs					
Low voltage	Sinking 2 mA		0.14	0.25	V
Leakage current	$\overline{PGx}$ = 17 V			1	μA
VINT					
Output voltage	0 < I_{VINT} < 50 μA	2	2.3	2.8	V
Fault Timer					
Sourcing current	V_{CTx} = 0 V, during fault	–7	–10	–13	μA
Sinking current	V_{CTx} = 2 V	7	10	13	
Upper threshold voltage		1.3	1.35	1.4	V
Lower threshold voltage		0.33	0.35	0.37	
12-V Summing Node					
Input referred offset	V_{SENMx} = 10.8 – 13.2 V, V_{SENPx} = V_{SENMx} + 50 mV, measure V_{SETx} – V_{SENMx}	–2		2	mV
Summing threshold	V_{PASSx} = 15 V	0.66	0.675	0.69	V
Leakage current	V_{SETx} = V_{SENMx} – 10 mV			1	μA
12-V Current Limit					
Current limit threshold	R_{SUMx} = 6.8 kΩ, R_{SETx} = 422 Ω, increase I_{LOADx} and measure V_{SENPx} – V_{SENMx} when V_{PASSx} = 15 V	47.5	50	52.5	mV
Sink current in current limit	V_{SUMx} = 1 V, V_{PASSx} = 12 V, measure I_{PASSx}	20		40	μA
Fast trip threshold	Measure V_{SENPx} – V_{SENMx}	80	100	120	mV
Fast turn-off delay	20 mV overdrive, C_{PASSx} = 0 pF, t_{p50-50}		200	300	ns
Timer start threshold	V_{PASSx} - V_{INx} when timer starts, while V_{PASSx} falling due to over current	5	6	7	V

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ELECTRICAL CHARACTERISTICS (continued)

IN3A = IN3B = VDD3A = VDD3B = 3.3 V. IN12A = IN12B = SENPA = SENPB = SENMA = SENMB = SETPA = SETPB = 12 V. $\overline{EN12A}$ = $\overline{EN12B}$ = $\overline{EN3A}$ = $\overline{EN3B}$ = $\overline{ORENA}$ = $\overline{ORENB}$ = CT12A = CT12B = CT3A = CT3B = AGND = GNDA = GNDB = 0 V. SUM12A = SUM12B = 6.8 kΩ to ground. SUM3A = SUM3B = 3.3 kΩ to ground. All other pins open. Over free air temperature operating range and all voltages referenced to AGND, -40°C ≤ T_A ≤ 85°C, typical vales at 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
12-V UVLO					
UVLO rising	IN12x rising	8.1	8.5	8.9	V
UVLO hysteresis	IN12x falling	0.44	0.5	0.59	
12-V BLOCKING					
Turn-on threshold	Measure $V_{SENPx} – V_{OUTx}$	5	10	15	mV
Turn-off threshold	Measure $V_{SENPx} – V_{OUTx}$	–5	–3	0	
Turn-off delay	20 mV overdrive, C_{BLKx} = 0 pF, t_{p50-50}		200	300	ns
12-V Gate Drivers (PASSx, BLKx)					
Output voltage	$V_{INx} = V_{OUTx}$ = 10 V	21.5	23	24.5	V
Sourcing current	$V_{IN12x} = V_{OUT12x}$ = 10 V, $V_{PASSx} = V_{BLKx}$ = 17 V	20	30	40	µA
Sinking current	Fast turnoff, $V_{PASSx} = V_{BLKx}$ = 14 V	0.5	1		A
	Sustained, $V_{PASSx} = V_{BLKx}$ = 4 – 25 V	6	14	25	mA
Pulldown resistance	In OTSD (at 150 °C)	14	20	26	kΩ
Fast turn-off duration		5	10	15	µs
Disable delay	EN12x pin to PASSx and BLKx, t_{p50-90}			1	µs
Startup time	IN12x rising to PASSx and BLKx sourcing			0.25	ms
3.3-V Summing Node					
Summing threshold		655	675	695	mV
3.3-V Current Limit					
On resistance	I_{OUT3x} = 150 mA		290	500	mΩ
Current limit	R_{SUM3x} = 3.3 kΩ , V_{OUT3x} = 0 V	170	195	225	mA
Fast trip threshold		250	300	400	
Fast turn-off delay	I_{OUT3x} = 400 mA, t_{p50-50}		750	1300	ns
3.3-V UVLO					
UVLO rising	IN3x rising	2.65	2.75	2.85	V
UVLO hysteresis	IN3x falling	200	240	300	mV
Supply Currents ($I_{INx} + I_{SENPx} + I_{SENMx} + I_{SETx} + I_{VDDx}$)					
All channels enabled	$I_{OUT3A} = I_{OUT3B}$ = 0		3.1	4	mA
All channels disabled			2	2.8	
Thermal Shutdown					
Whole-chip shutdown temperature	T_J rising, $I_{OUT3A} = I_{OUT3B}$ = 0	140	150		°C
3.3 V channel shutdown temperature	T_J rising, I_{OUT3A} or I_{OUT3B} in current limit	130	140		
Hysteresis	Whole chip or 3.3-V channel		10		

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DEVICE INFORMATION

SIGNAL AND PIN NAMING BLOCK

The PICMG™ AdvancedMC™ specification refers to 3.3-V power as management power and refers to 12-V power as payload power. This datasheet uses a naming convention that reflects the associated voltage (12 V to 3 V) and AdvancedMC™ slot (A or B).

- Signals and pins associated with slot A 12-V payload power end with 12A.
- Signals and pins associated with slot A 3.3-V management power end with 3A.
- Signals and pins associated with slot B 12-V payload power end with 12B.
- Signals and pins associated with slot B 3.3-V management power end with 3B.

Pins and signals unique to 12-V channels have only an A or B suffix.

TPS2358 Block Diagrams

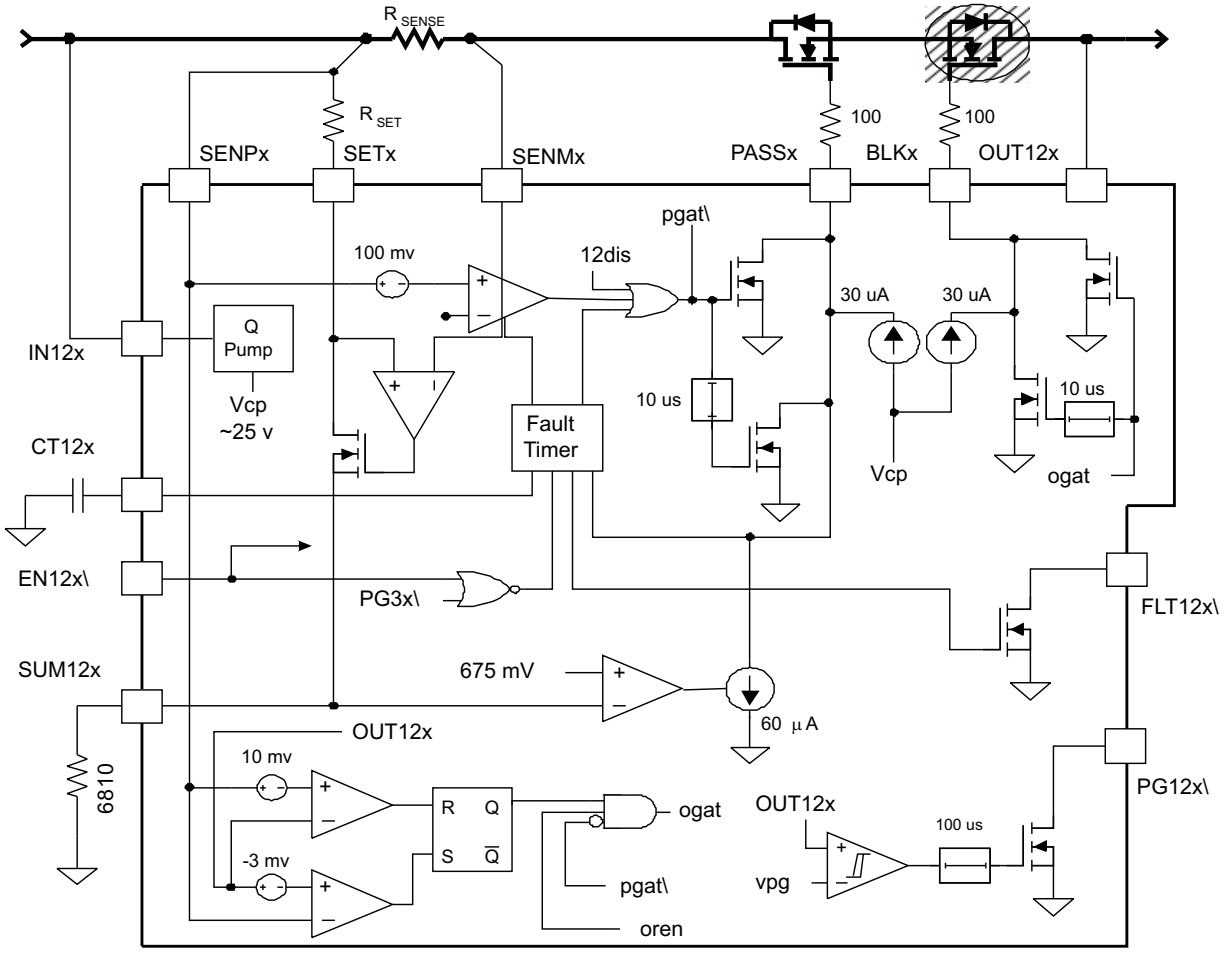


Figure 1. 12-V Channel Circuitry

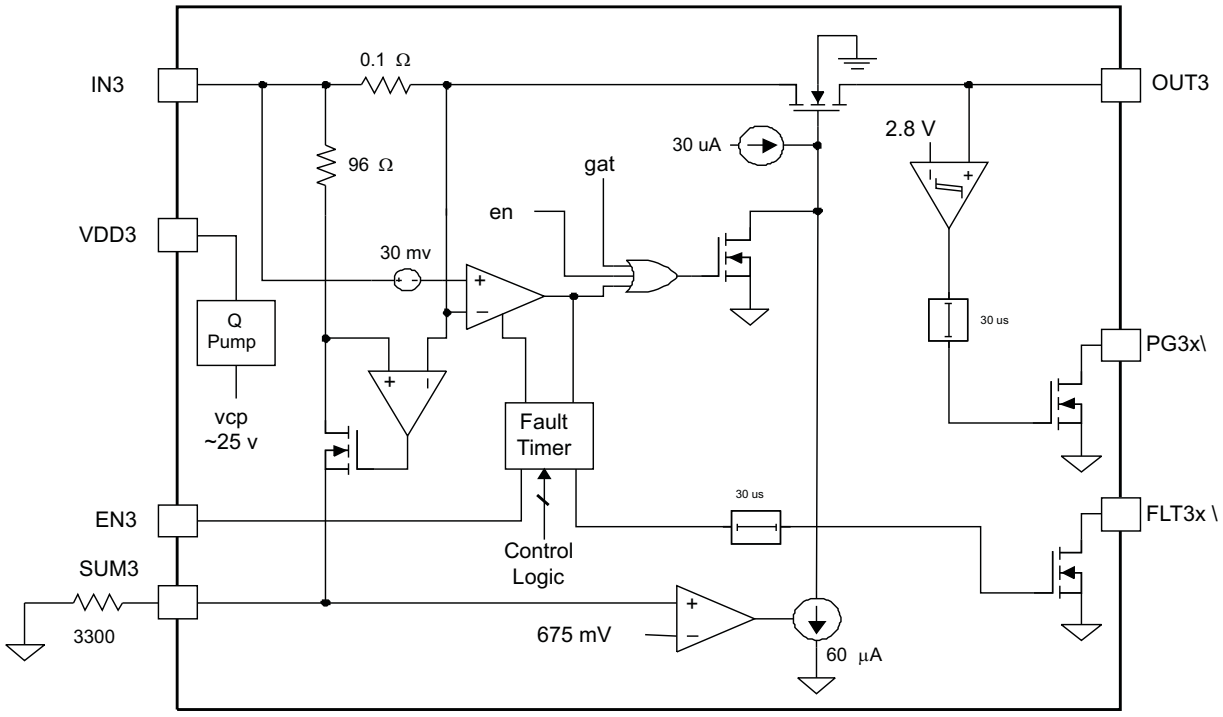


Figure 2. 3-V Channel Circuitry

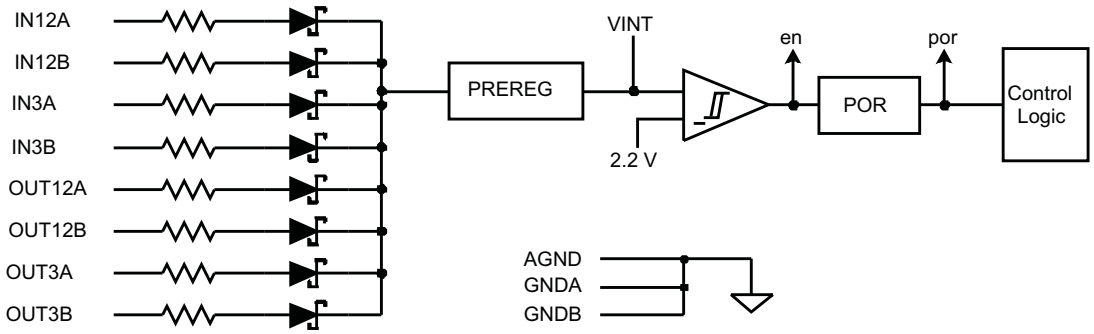
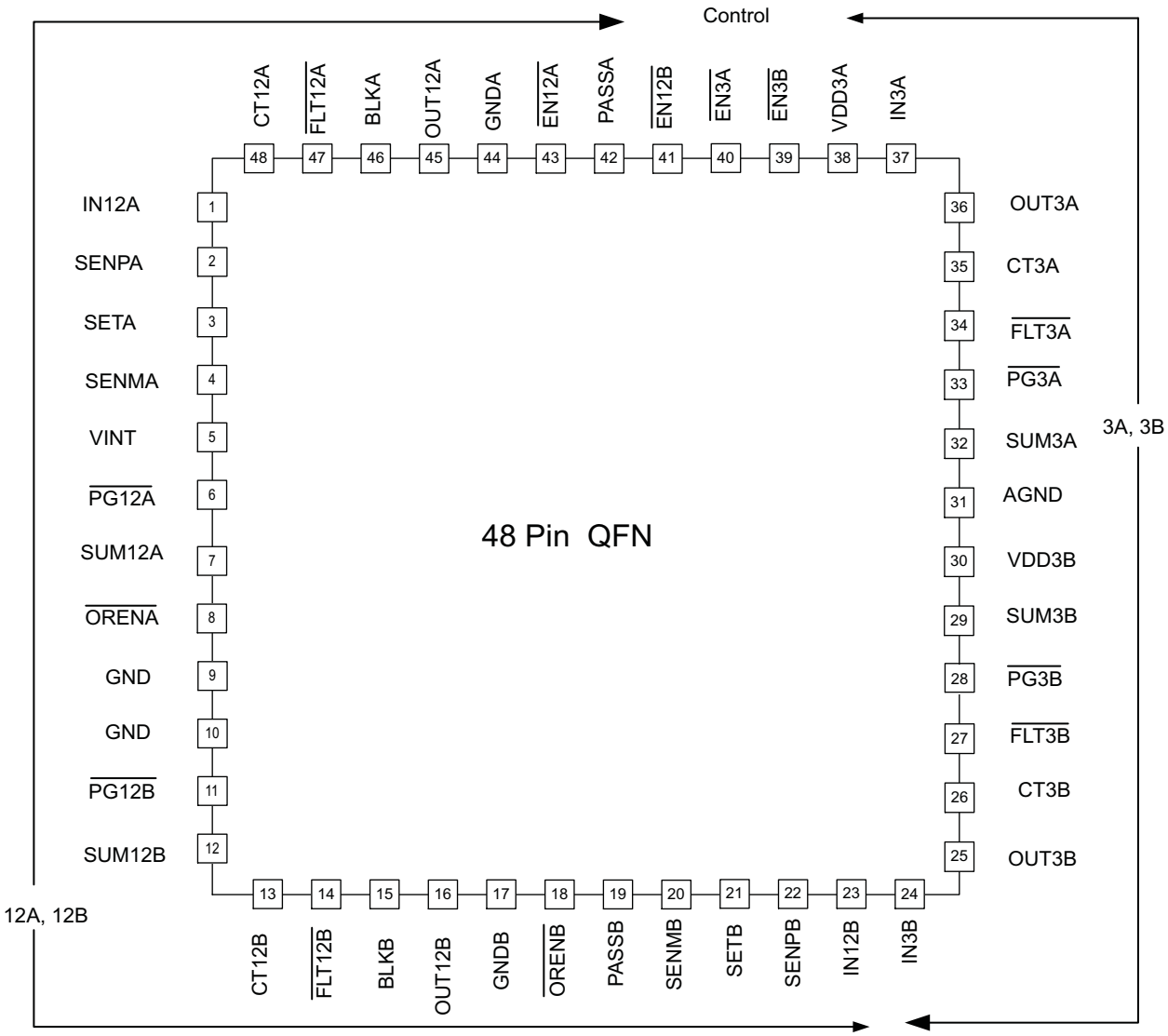


Figure 3. Circuitry Common to all Channels

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TERMINAL FUNCTIONS

PIN#	NAME	TYPE	DESCRIPTION
1	IN12A	V_{DD}	12A input
2	SENPA	I	12A input sense
3	SETA	I	12A current limit set
4	SENMA	I	12A current limit sense
5	VINT	I/O	Bypass capacitor connection point for internal supply
6	$\overline{\text{PG12A}}$	O	12A power good output, active low, asserts when OUT12A > VPG12A
7	SUM12A	I/O	12A summing node
8	$\overline{\text{ORENA}}$	I	12A blocking transistor enable, active low
9	GND	GND	Connect pin to ground
10	GND	GND	Connect pin to ground
11	$\overline{\text{PG12B}}$	O	12B power good output, active low, asserts when OUT12B > VPG12B
12	SUM12B	I/O	12B summing node

TERMINAL FUNCTIONS (continued)

PIN#	NAME	TYPE	DESCRIPTION
13	CT12B	I/O	12B fault timing capacitor
14	$\overline{\text{FLT12B}}$	O	12B fault output, active low, asserted when 12B fault timer runs out
15	BLKB	O	12B blocking transistor gate drive
16	OUT12B	I/O	12B output
17	GNDB	GND	12B power ground
18	$\overline{\text{ORENB}}$	I	12B blocking transistor enable, active low
19	PASSB	O	12B pass transistor gate drive
20	SENMB	I	12B current limit sense
21	SETB	I	12B current limit set
22	SENPB	I	12B input sense
23	IN12B	V_{DD}	12B input
24	IN3B	V_{DD}	3B input
25	OUT3B	I/O	3B output
26	CT3B	I/O	3B fault timing capacitor
27	$\overline{\text{FLT3B}}$	O	3B fault output, active low, asserted when 3B fault timer runs out
28	$\overline{\text{PG3B}}$	O	3B power good output, active low, asserts when OUT3B > 2.8 V
29	SUM3B	I/O	3B summing node
30	VDD3B	V_{DD}	3B charge pump input
31	AGND	GND	Analog ground
32	SUM3A	I/O	3A summing node
33	$\overline{\text{PG3A}}$	O	3A power good output, active low, asserts when OUT3A > 2.8 V
34	$\overline{\text{FLT3A}}$	O	3A fault output, active low, asserted when 3A fault timer runs out
35	CT3A	I/O	3A fault timing capacitor
36	OUT3A	I/O	3A output
37	IN3A	V_{DD}	3A input
38	VDD3A	V_{DD}	3A charge pump input
39	$\overline{\text{EN3B}}$	I	3B enable, (default active low)
40	$\overline{\text{EN3A}}$	I	3A enable, (default active low)
41	$\overline{\text{EN12B}}$	I	12B enable, (default active low)
42	PASSA	O	12A pass transistor gate drive
43	$\overline{\text{EN12A}}$	I	12A enable, (default active low)
44	GNDA	GND	12A power ground
45	OUT12A	I/O	12A output
46	BLKA	O	12A blocking transistor gate drive
47	$\overline{\text{FLT12A}}$	I/O	12A fault output, active low, asserted when 12A fault timer runs out
48	CT12A	I/O	12A fault timing capacitor

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DEVICE INFORMATION

DETAILED PIN DESCRIPTION

AGND Ground pin for the analog circuitry inside the TPS2358.

BLKx Gate drive pin for the 12x channel BLK FET. This pin sources 30 µA to turn the FET on. An internal clamp prevents this pin from rising more than 14.5 V above OUT12x. Setting the $\overline{\text{OREN}}$x pin high holds the BLKx pin low.

CTx A capacitor from CTx to GND sets the time the channel can remain in current limit before it shuts down and declares a fault. Current limit causes this pin to source 10 µA into the external capacitor (CT). When VCTx reaches 1.35 V, the TPS2358 shuts the channel off by pulling the PASSx pin low and declares an over-current fault by pulling the FLTx pin low.

$\overline{\text{EN12x}}$ Active low enable input. Pulling this pin high (or allowing it to float high) turns off channel 12x by pulling both BLKx and PASSx low. An internal 200-kΩ resistor pulls this pin up to VINT when disconnected.

$\overline{\text{EN3x}}$ Active low enable input. Pulling this pin high (or allowing it to float high) turns off channel 3x by pulling the gate of the internal pass FET to GND. An internal 200-kΩ resistor pulls this pin up to VINT when disconnected.

$\overline{\text{FLTx}}$ Active low open-drain output indicating that channel x has remained in current limit long enough to time out the fault timer and shut the channel down.

IN12x Supply pin for channel 12x internal circuitry.

IN3x Supply pin for channel 3x internal pass FET.

$\overline{\text{ORENx}}$ Active low input. Pulling this pin low allows the 12x channel ORing function to operate normally. Pulling this pin high (or allowing it to float high) disables the ORing function by pulling the BLKx pin low. An internal 200-kΩ resistor pulls this pin up to VINT when disconnected.

OUT12x Senses the output voltage of the channel 12x path. OUT12x is the return node for the BLKx pin clamp. This pin will source ~30 µA when the BLK FET is fully enhanced.

OUT3x Output of the channel 3x internal pass FET.

PASSx Gate drive pin for the 12x channel pass FET. This pin sources 30 µA to turn the FET on. An internal clamp prevents this pin from rising more than 14.5 V above IN12x.

$\overline{\text{PGx}}$ Active low open-drain output indicating that channel x output voltage is above the PG threshold, which nominally equals 2.85 V for the 3x channels and 10.5 V for the 12x channels.

SENMx Senses the voltage on the low side of the channel 12x current sense resistor.

SENPx Senses the voltage on the high side of the channel 12x current sense resistor.

SETx A resistor connected from this pin to SENPx sets the current limit level in conjunction with the current sense resistor and the resistor connected to the SUM12x pin, as described in 12-V thresholds – setting current limit and fast over current trip section.

SUMx A resistor connected from this pin to ground forms part of the channel x current limit. As the current delivered to the load increases, so does the voltage on this pin. When the voltage on this pin reaches a threshold of 675 mV, the current limit amplifier acts to prevent the current from further increasing.

VDD3x Supply pin for channel3x internal circuitry.

VINT This pin connects to the internal 2.35-V rail. A 0.1-µF capacitor must be connected from this pin to ground. Do not connect other external circuitry to this pin.

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TYPICAL CHARACTERISTICS

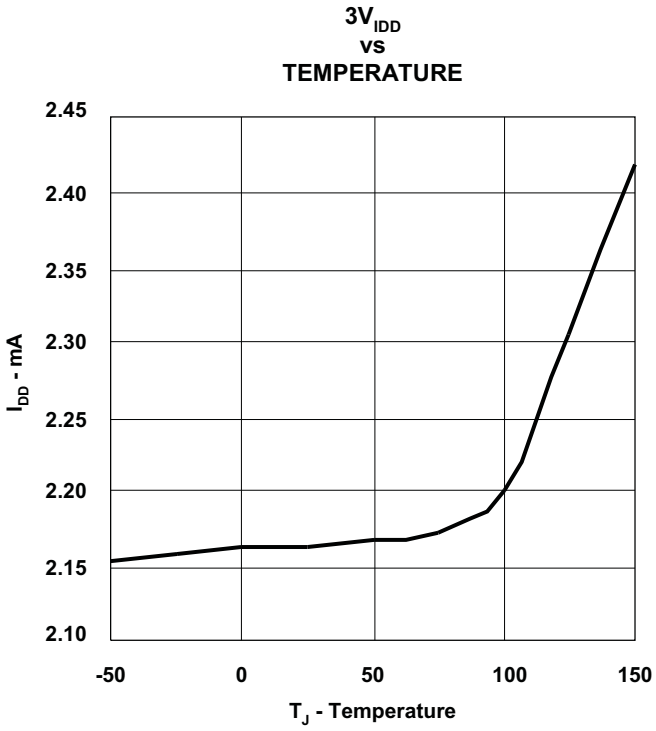


Figure 4.

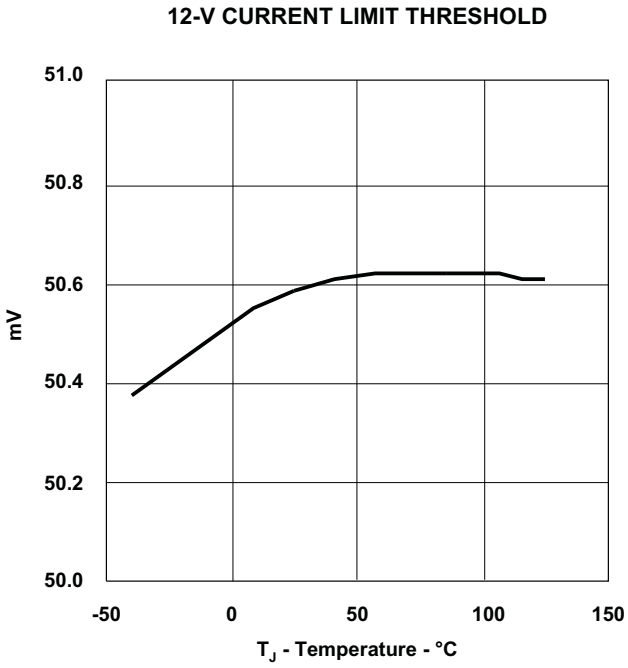


Figure 5.

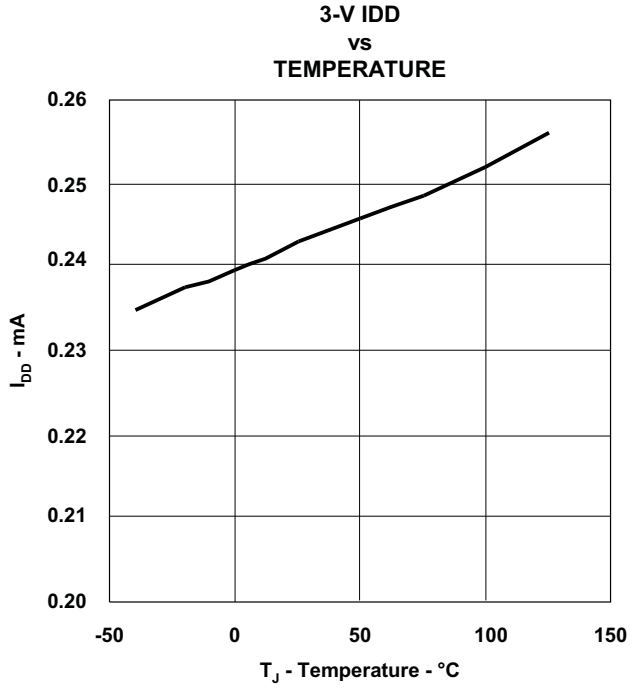


Figure 6.

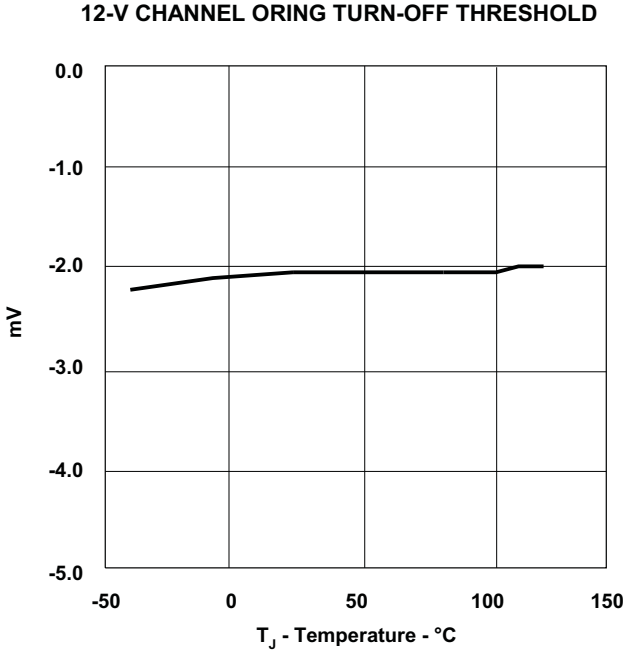


Figure 7.

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TYPICAL CHARACTERISTICS (continued)

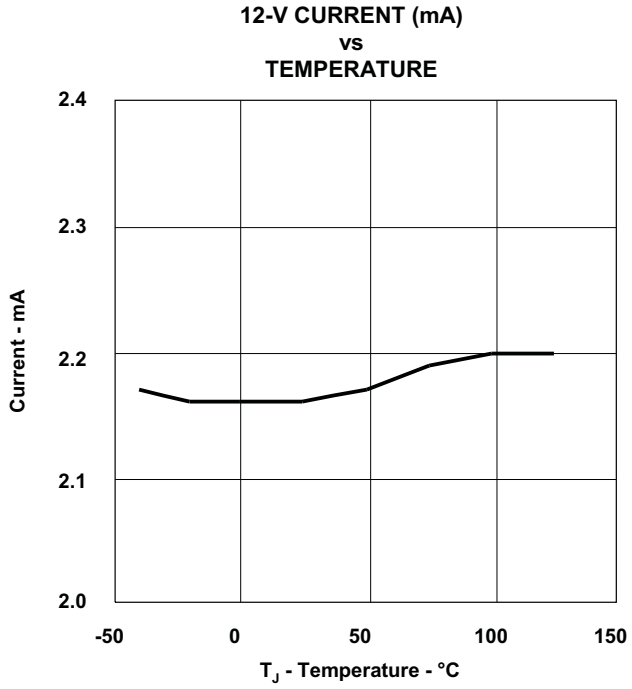


Figure 8.

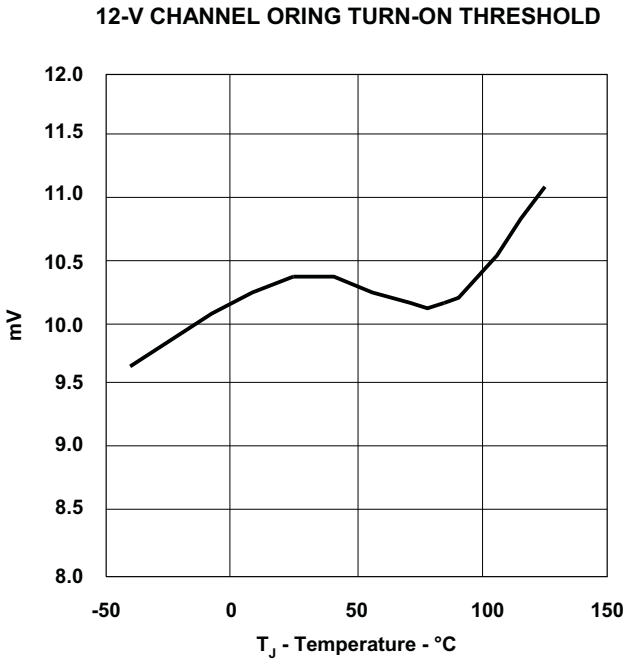


Figure 9.

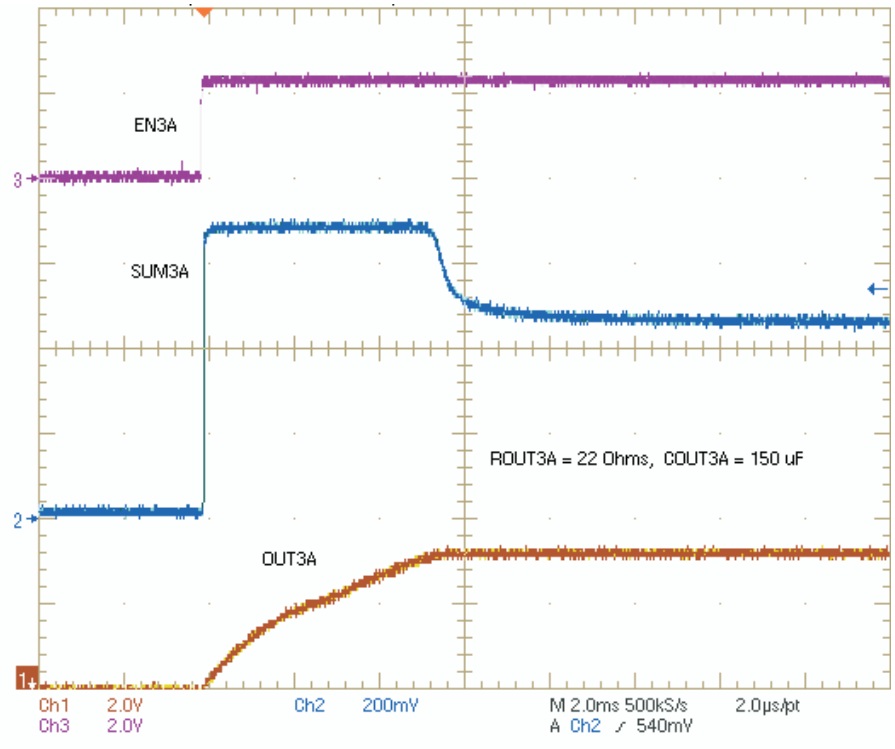


Figure 10. OUT3A Startup Into 22-Ω (150 mA) 150-µF Load

TYPICAL CHARACTERISTICS (continued)

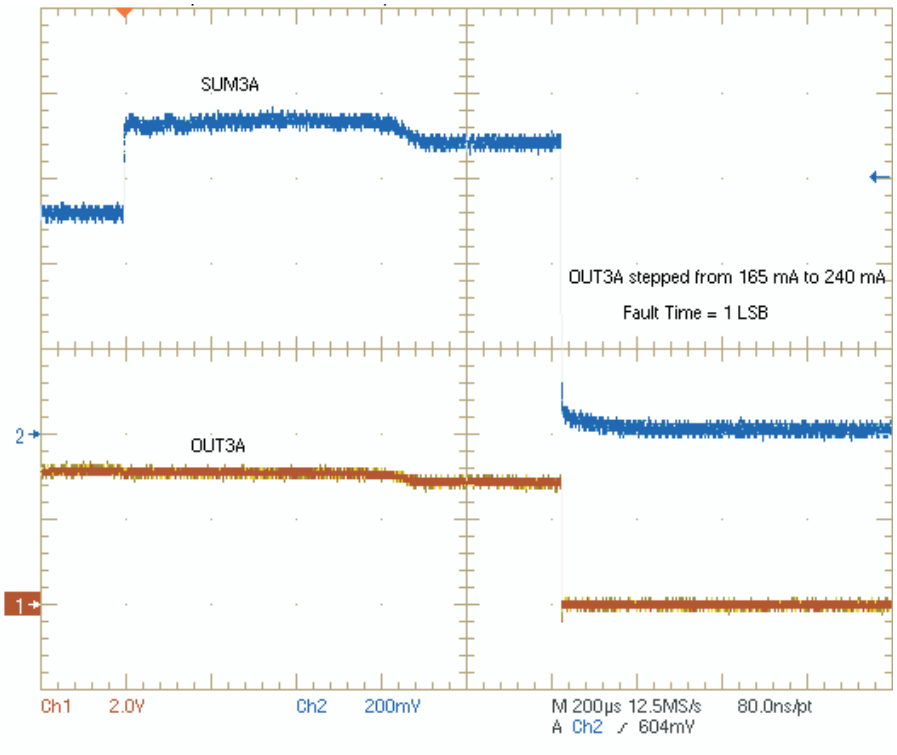


Figure 11. OUT3A Load Stepped from 165 mA to 240 mA

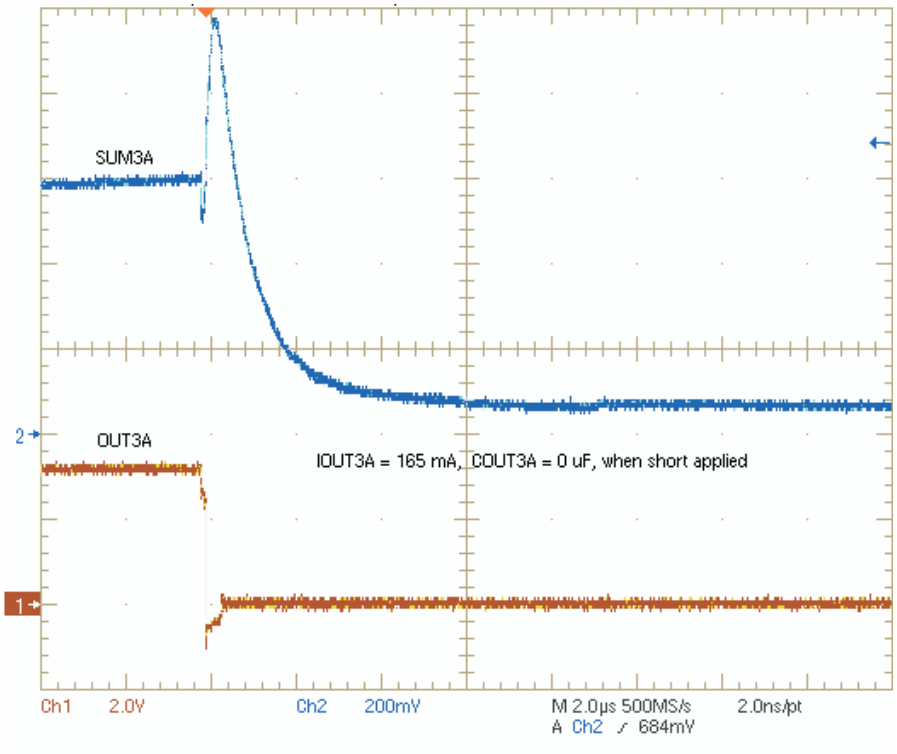


Figure 12. OUT3A Short Circuit under Full Load (165 mA) Zoom View

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TYPICAL CHARACTERISTICS (continued)

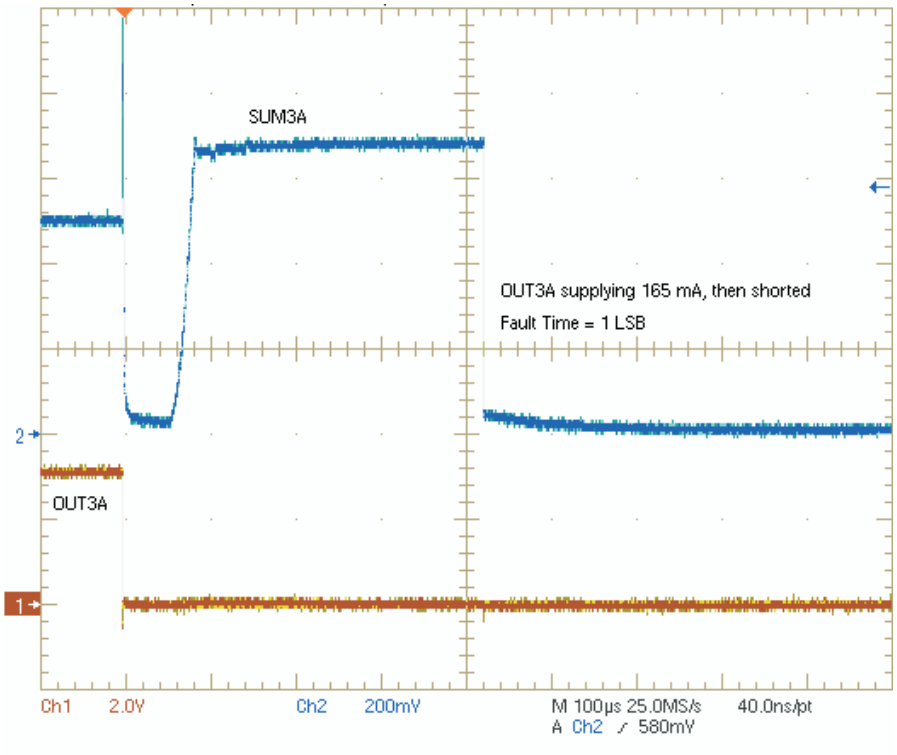


Figure 13. OUT3A Short Circuit Under Full Load (165 mA) Wide View

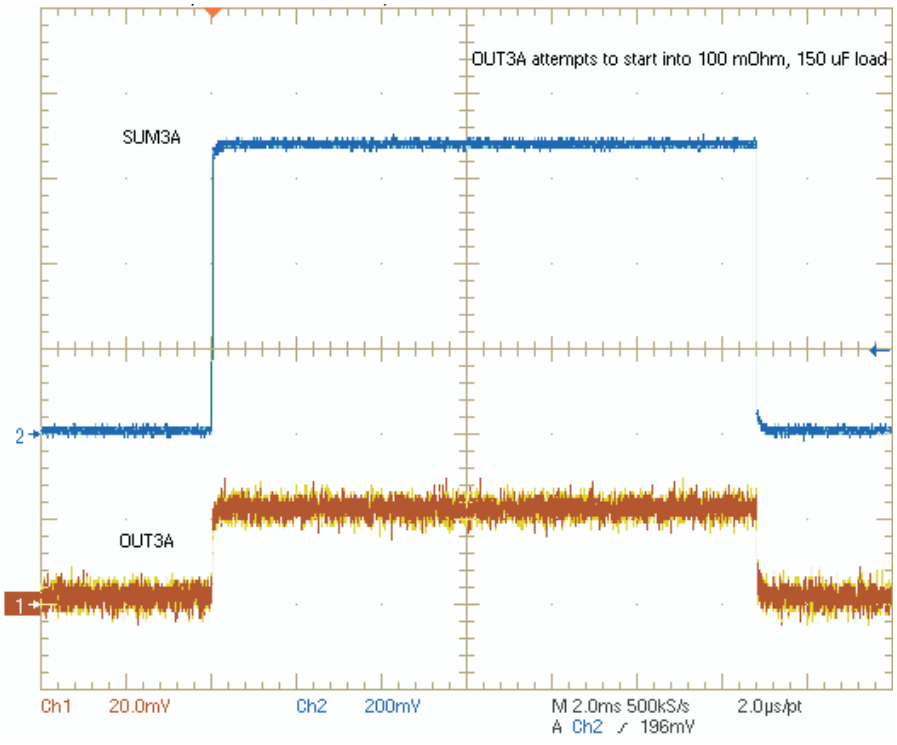


Figure 14. OUT3A Startup Into Short Circuit

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TYPICAL CHARACTERISTICS (continued)

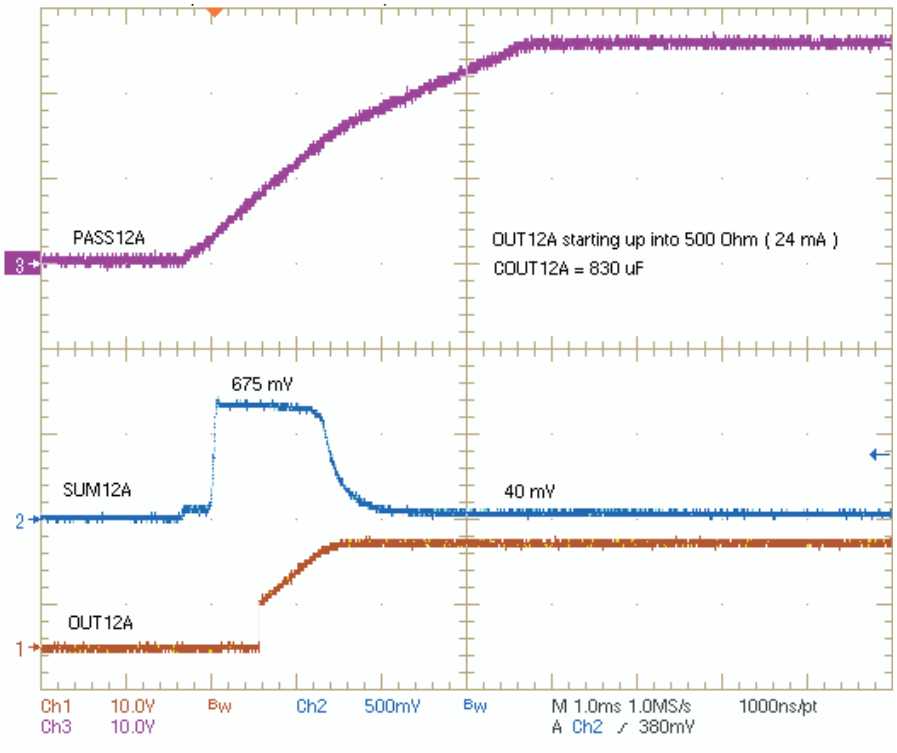


Figure 15. OUT12A Startup Into 500-Ω, 830-µF Load

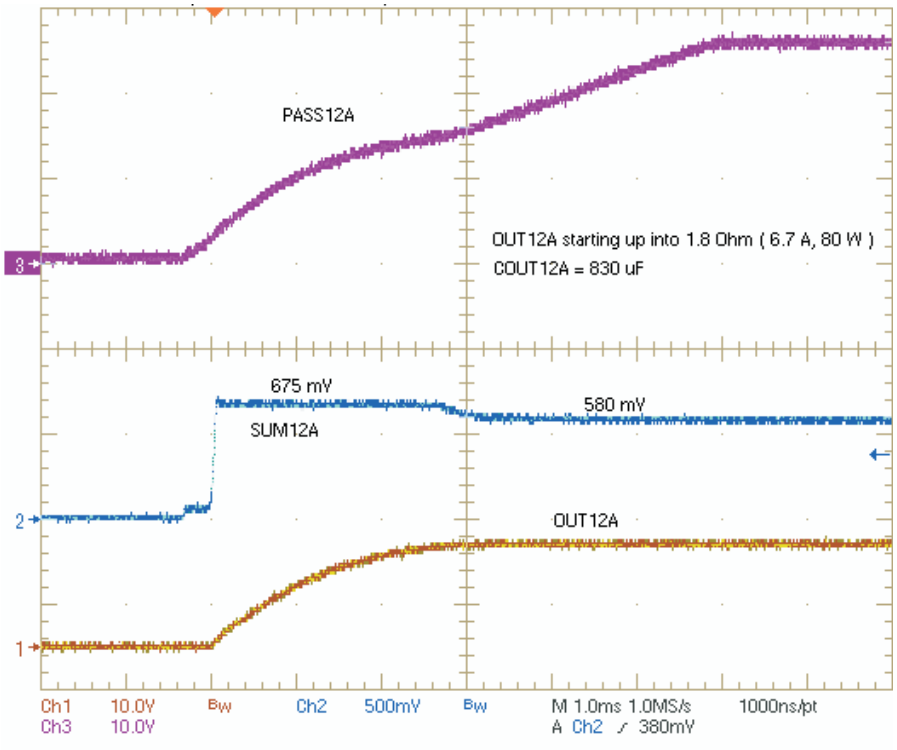


Figure 16. OUT12A Startup Into 80-Watt, 830-µF Load

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TYPICAL CHARACTERISTICS (continued)

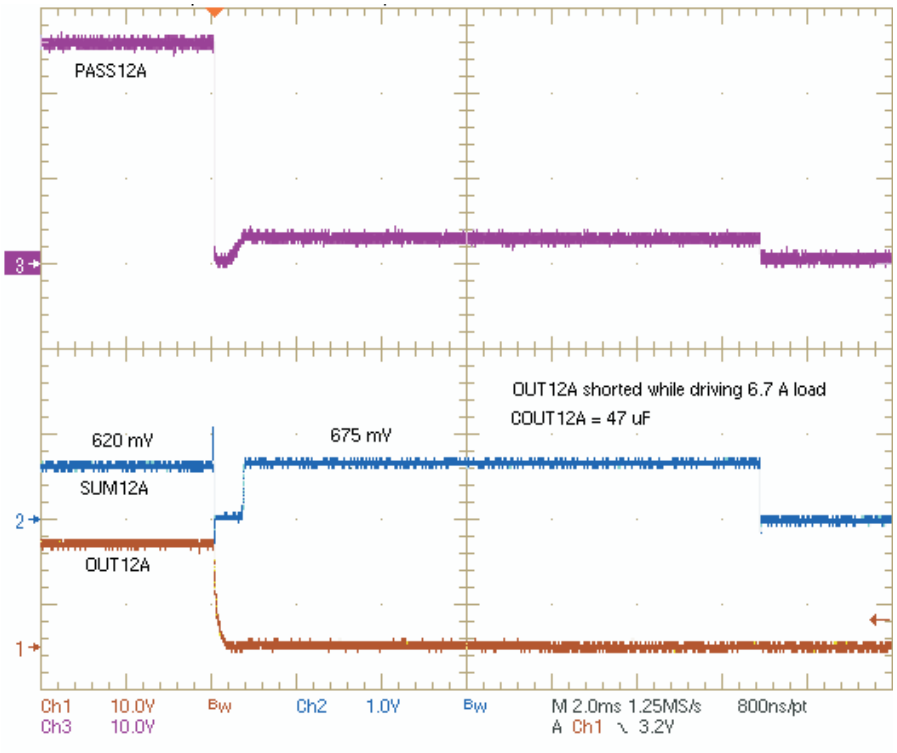


Figure 17. OUT12A Short Circuit Under Full Load (6.7 A) Wide View

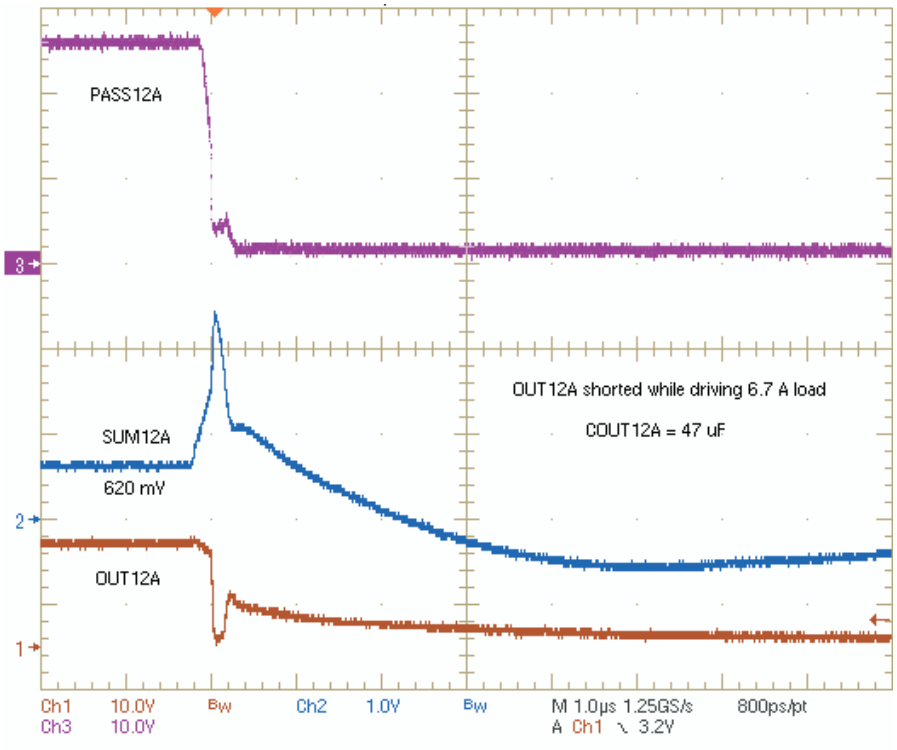


Figure 18. OUT12A Short Circuit Under Full Load (6.7 A) Zoom View

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TYPICAL CHARACTERISTICS (continued)

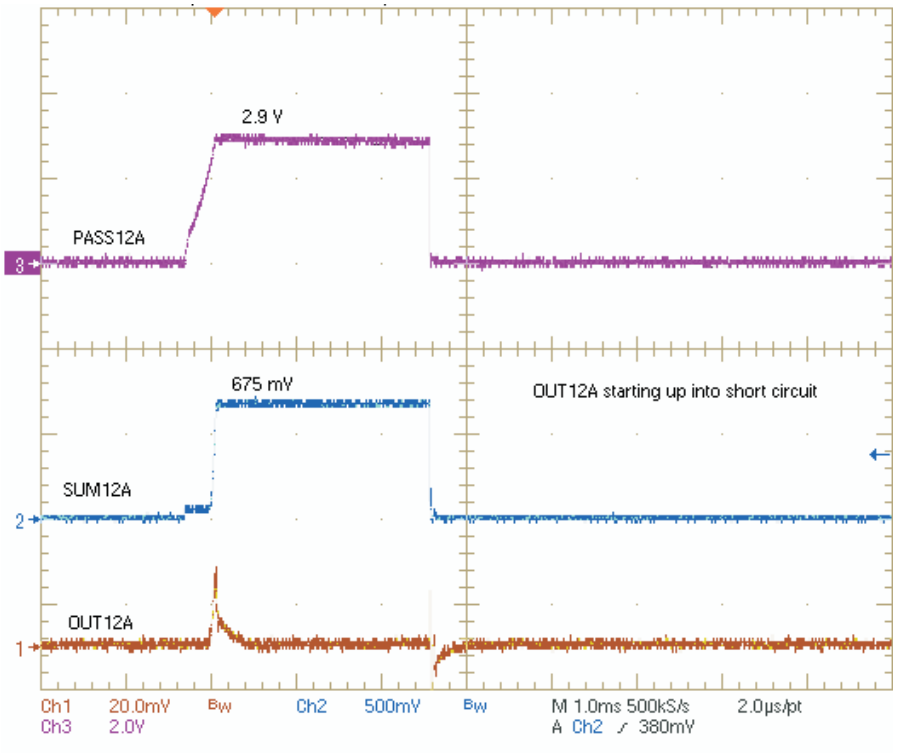


Figure 19. OUT12A Startup Into Short Circuit

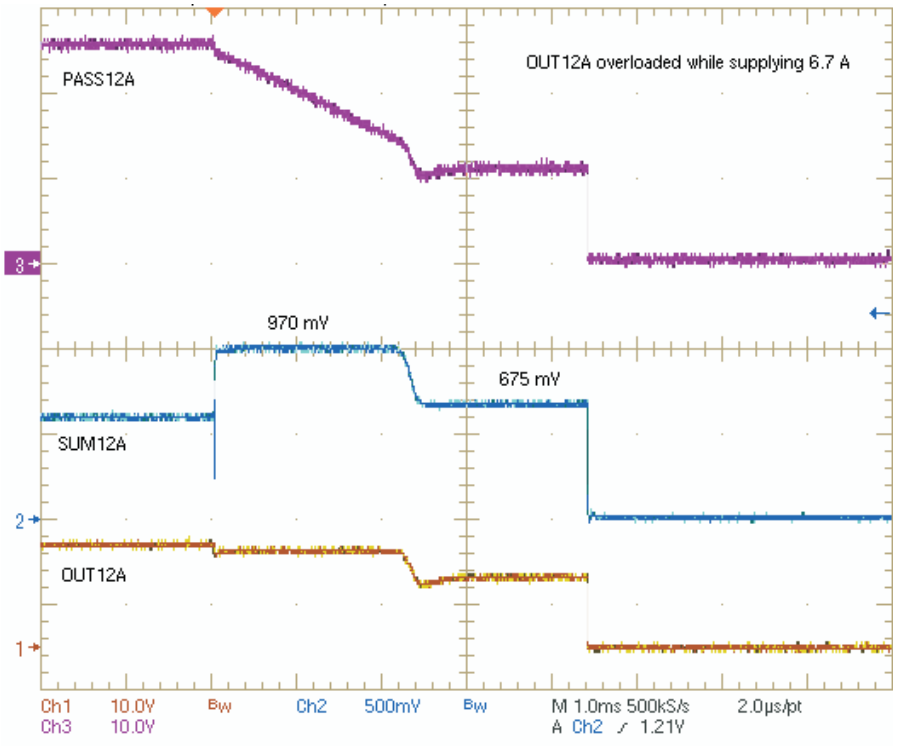


Figure 20. OUT12A Overloaded While Supplying 6.7 A

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REFERENCE INFORMATION

The TPS2358 has been designed to simplify compliance with the PICMG-AMC.R2.0 and PICMG-MTCA.0 specifications. These specifications were developed by the PCI Industrial Computer Manufacturers Group (PICMG). These two specifications are derivations of the PICMG-ATCA (Advanced Telecommunication Computing Architecture) specification originally released in December, 2002.

PICMG-AMC Highlights

- AMC – Advanced Mezzanine Cards
- Designed to Plug Into ATCA Carrier Boards
- AdvancedMC™ Focuses on Low Cost
- 1 to 8 AdvancedMC™ per ATCA Carrier Board
- 3.3-V Management Power (maximum current draw of 150 mA)
- 12-V Payload Power – (converted to required voltages on AMC)
- Maximum 80-W Dissipation per AdvancedMC™
- Hotswap and Current Limiting Must be Present on Carrier Board
- For Details,See www.picmg.org/v2internal/AdvancedMC.htm

PICMG-MTCA Highlights

- MTCA - MicroTelecommunications Computing Architecture
- Architecture for Using AMCs Without an ATCA Carrier Board
- Up to 12 AMCs Per System, Plus Two MCHs and Two CUs
- Focuses on Low Cost
- All Functions of ATCA Carrier Board Must be Provided
- MicroTCA is Also Known as MTCA, mTCA, or uTCA
- For Details, See www.picmg.org/v2internal/microTCA.htm

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SYSTEM OPERATION

Introduction

The TPS2358 controls two 12-V power paths and two 3.3-V power paths. Each power path can draw from a single common supply, or from two independent supplies. The TPS2358 is in a 48-pin QFN package. The following sections describe the main functions of the TPS2358 and provide guidance for designing systems around this device.

Control Logic and Power-On Reset

The TPS2358's circuitry draws power from an internal bus fed by a preregulator. A capacitor attached to the VINT pin provides decoupling and output filtering for this preregulator. It can draw power from any of four inputs (IN12A, IN12B, IN3A, or IN3B) or from any of four outputs (OUT12A, OUT12B, OUT3A, or OUT3B). This feature allows the internal circuitry to function regardless of which channels receive power, or from what source. The four external FET drive pins (PASSA, PASSB, BLKA, and BLKB) are held low during startup to ensure that the two 12-V channels remain off. The internal 3.3-V channels are also held off. When the voltage on the internal VINT rail exceeds approximately 1 V, the power-on reset circuit initializes the TPS2358.

Enable Functions

The TPS2358 provides three external enable pins for each of its two AdvancedMC™ slots. Pulling the $\overline{\text{EN3x}}$ low turns on the 3x channel. Pulling the $\overline{\text{EN12x}}$ pin turns on the 12x channel. If the $\overline{\text{EN12x}}$ pin goes high, the TPS2358 pulls both the PASSx and BLKx pins to ground. Pulling the $\overline{\text{ORENx}}$ pin low turns on the reverse blocking circuitry in the 12x channel. If the $\overline{\text{ORENx}}$ pin goes high, then the BLKx pin remains low. Each of the six enable pins has an internal 200-kΩ pullup resistor to VINT. To comply with AdvancedMC™ requirements, the 12-V Channels will not enable unless the associated 3.3 channel $\overline{\text{PG}}$ is asserted.

Power Good ($\overline{\text{PG}}$) Outputs

The TPS2358 provides four active-low open-drain outputs that monitor the status of the four output voltage rails. The power good output for each channel pulls low whenever the voltage on its OUTx pin exceeds the PG threshold. The 3.3-V channels have nominal thresholds of 2.85 V and the 12-V channels have nominal thresholds of 10.5 V.

Fault ($\overline{\text{FLT}}$) Outputs

The TPS2358 provides four active-low, open-drain fault outputs, one for each channel. A fault output pulls low when the channel has remained in current limit long enough to run out the fault timer. A channel experiencing a fault condition automatically shuts down. To clear the fault and re-enable the channel, turn the channel off and back on using the appropriate $\overline{\text{ENx}}$ pin.

Current Limit and Fast Trip Thresholds

All four channels monitor current by sensing the voltage across a resistor. The 3.3-V channels use internal sense resistors with a nominal value of 290 mΩ. The 12-V channels use external sense resistors that typically lie in the range of 4 - 10 mΩ. Each channel features two distinct thresholds: a current limit threshold and a fast trip threshold.

The current limit threshold sets the regulation point of a feedback loop. If the current flowing through the channel exceeds the current limit threshold, then this feedback loop reduces the gate-to-source voltage imposed on the pass FET. This causes the current flowing through the channel to settle to the value determined by the current limit threshold. For example, when a module first powers up, it draws an inrush current to charge its load capacitance. The current limit feedback loop ensures that this inrush current does not exceed the current limit threshold.

The current limit feedback loop has a finite response time. Serious faults such as shorted loads require a faster response in order to prevent damage to the pass FETs or voltage sags on the supply rails. A comparator monitors the current flowing through the sense resistor, and if it ever exceeds the fast trip threshold, then it immediately shuts off the channel. The channel turns back on slowly, allowing the current limit feedback loop time to respond. One normally sets the fast trip threshold some 2 to 5 times higher than the current limit.

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3.3-V Current Limiting

The 3.3-V management power channels include internal pass FETs and current sense resistors. The on-resistance of a management channel - including pass FET, sense resistor, metallization resistance, and bond wires - typically equals 290 mΩ and never exceeds 500 mΩ. The AdvancedMC™ specification allows a total of 1 Ω between the power source and the load. The TPS2358 never consumes more than half of this budget.

3.3-V Fast Trip Function

The 3.3-V fast trip function protects the channel against short-circuit events. If the current through the channel exceeds a nominal value of 300 mA, then the TPS2358 immediately disables the internal pass transistor and then allows it to slowly turn back on into current limiting.

3.3-V Current Limit Function

The 3.3-V current limit function internally limits the current to comply with the AdvancedMC™ and MicroTCA™ specifications. External resistor RSUM3x allows the user to adjust the current limit threshold. The nominal current limit threshold I_{LIMIT} equals:

$$I_{LIMIT} = \frac{650V}{R_{SUM3x}} \quad (1)$$

A 3320-Ω resistor gives a nominal current limit of I_{LIMIT} = 195 mA which complies with AdvancedMC™ and MicroTCA™ specifications. This resistance corresponds to an EIA 1% value. Alternatively, a 3.3-kΩ resistor will also suffice. Whenever a 3.3-V channel enters current limit, its fault timer begins to operate (see Fault Timer Programming section).

3.3-V Over-Temperature Shutdown

The 3.3-V over-temperature shutdown trips if a 3.3-V channel remains in current limit so long that the die temperature exceeds approximately 140°C. When this occurs, any 3.3-V channel operating in current limit turns off until the chip cools by approximately 10°C. This feature prevents a prolonged fault on one 3.3-V channel from disabling the other 3.3-V channel, or disabling either of the 12-V channels.

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12-V Fast Trip and Current Limiting

Figure 21 shows a simplified block diagram of the circuitry associated with the fast trip and current limit circuitry within a 12-V channel. Each 12-V channel requires an external N-channel pass FET and three external resistors. These resistors allow the user to independently set the fast trip threshold and the current limit threshold, as described below.

12-V Fast Trip Function

The 12-V fast trip function is designed to protect the channel against short-circuit events. If the voltage across R_{SENSE} exceeds a nominal threshold of 100 mV, the device immediately disables the pass transistor and declares a fault condition. The nominal fast current limit equals:

$$I_{FT} = \frac{100mV}{R_S} \tag{2}$$

12-V Current Limit Function

The 12-V current limit function regulates the PASSx pin voltage to prevent the current through the channel from exceeding I_{LIMIT}. The current limit circuitry includes two amplifiers, A_1 and A_2, as shown in Figure 21. Amplifier A_1 forces the voltage across external resistor R_{SET} to equal the voltage across external resistor R_{SENSE}. The current that flows through R_{SET} also flows through external resistor R_{SUM}, generating a voltage on the 12SUMx pin equal to:

$$V_{12SUMx} = \left(\frac{R_{SENSE} R_{SUM}}{R_{SET}} \right) I_{SENSE} \tag{3}$$

Amplifier A_2 senses the voltage on the 12SUMx pin. As long as this voltage is less than the reference voltage on its positive input (nominally 0.675 V), the amplifier sources current to PASSx. When the voltage on the 12SUMx pin exceeds the reference voltage, amplifier A_2 begins to sink current from PASSx. The gate-to-source voltage of pass FET M_{PASS} drops until the the voltages on the two inputs of amplifier A_2 balance. The current flowing through the channel then nominally equals:

$$I_{LIMIT} = \left(\frac{R_{SET}}{R_{SUM} R_{SENSE}} \right) \cdot 0.675V \tag{4}$$

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The recommended value of R_{SUM} is 6810 Ω. This resistor should never equal less than 675 Ω to prevent excessive currents from flowing through the internal circuitry. Using the recommended values of R_{SENSE} = 5 mΩ and R_{SUM} = 6810 Ω gives:

$$I_{LIMIT} = (0.0198A/\Omega) \cdot R_{SET} \quad (5)$$

A system capable of powering an 80-Watt AdvancedMC™ module consumes a maximum of 8.25 A according to MicroTCA™ specifications. The above equation suggests R_{SET} = 417 Ω. The nearest 1% EIA value equals 422 Ω. The selection of R_{SET} for MicroTCA™ power modules is described in the Redundant vs. Non-Redundant Inrush Current Limiting section.

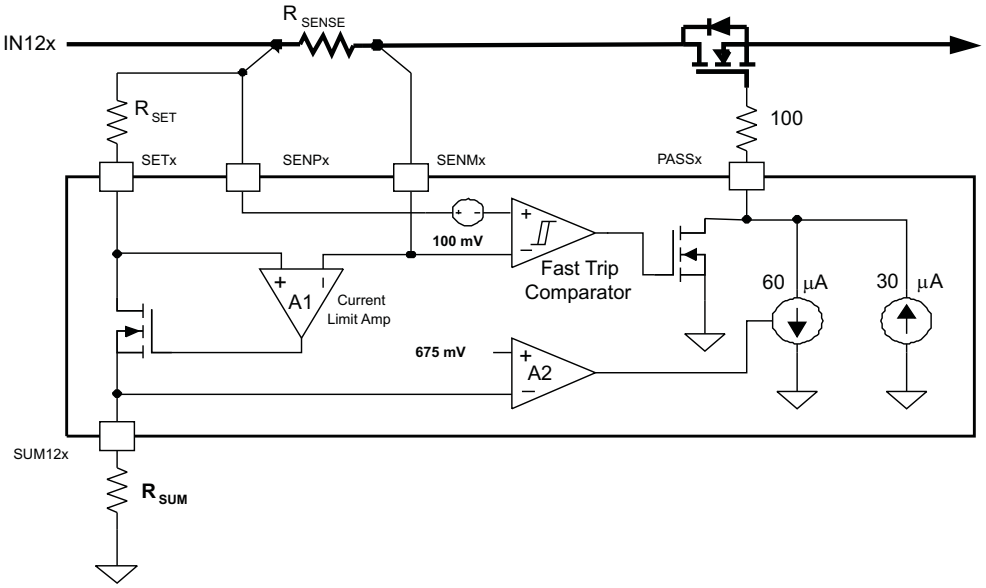


Figure 21. 12-V Channel Threshold Circuitry

Fault Timer Programming

The fault timers of the four channels in a TPS2358 use identical internal circuitry. Each channel requires an external capacitor C_T connected between the CTx pin and ground. Whenever the gate drive is less than 6 V the timer will be charging CT. When a channel goes into current limit, the TPS2358 injects 10 µA into the external capacitor. If the channel remains in current limit long enough for the voltage on the CTx pin to reach 1.35 V, then the TPS2358 shuts the channel down and pulls the $\overline{FLT}$x pin low to declare a fault. If the channel does not remain in current limit long enough to trip the timer, then the CTx capacitor is discharged through an internal 200-Ω pulldown resistor. The nominal fault time t_f equals:

$$t_f = \frac{1.35V}{10\mu A} C_T \quad (6)$$

$$C_T = 7.4 \times 10^{-6} \times T_F \quad (7)$$

The user should select capacitors that provide the shortest fault times sufficient to allow down-stream loads and bulk capacitors to charge. Shorter fault times reduce the stresses imposed on the pass FETs under fault conditions. This consideration may allow the use of smaller and less expensive FETs for the 12-V channels.

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Multiswap Operation in Redundant Systems

TheTPS2358 features an additional mode of operation called Multiswap redundancy. This technique does not require a microcontroller, making it simpler and faster than the redundancy schemes described in the MicroTCA™ standard. Multiswap is especially attractive for AdvancedMC™ applications that require redundancy but need not comply with the MicroTCA™ power module standard.

In order to implement Multiswap redundancy, connect the SUM pins of the redundant supplies together and tie a single R_{SUM} resistor from this node to ground. The current limit thresholds now apply to the sum of the currents delivered by the redundant supplies. When implementing multiswap redundancy on 12-V channels, all of the channels must use the same values of resistors for R_{SENSE} and R_{SET}.

Figure 22 compares the redundancy technique advocated by the MicroTCA™ specification to multiswap redundancy. MicroTCA™ redundancy independently limits the current delivered by each power source. The current drawn by the load cannot exceed the sum of the current limits of the individual power sources. Multiswap redundancy limits the current drawn by the load to a fixed value regardless of the number of operational power sources. Removing or inserting power sources within a multiswap system does not affect the current limit seen by the load.

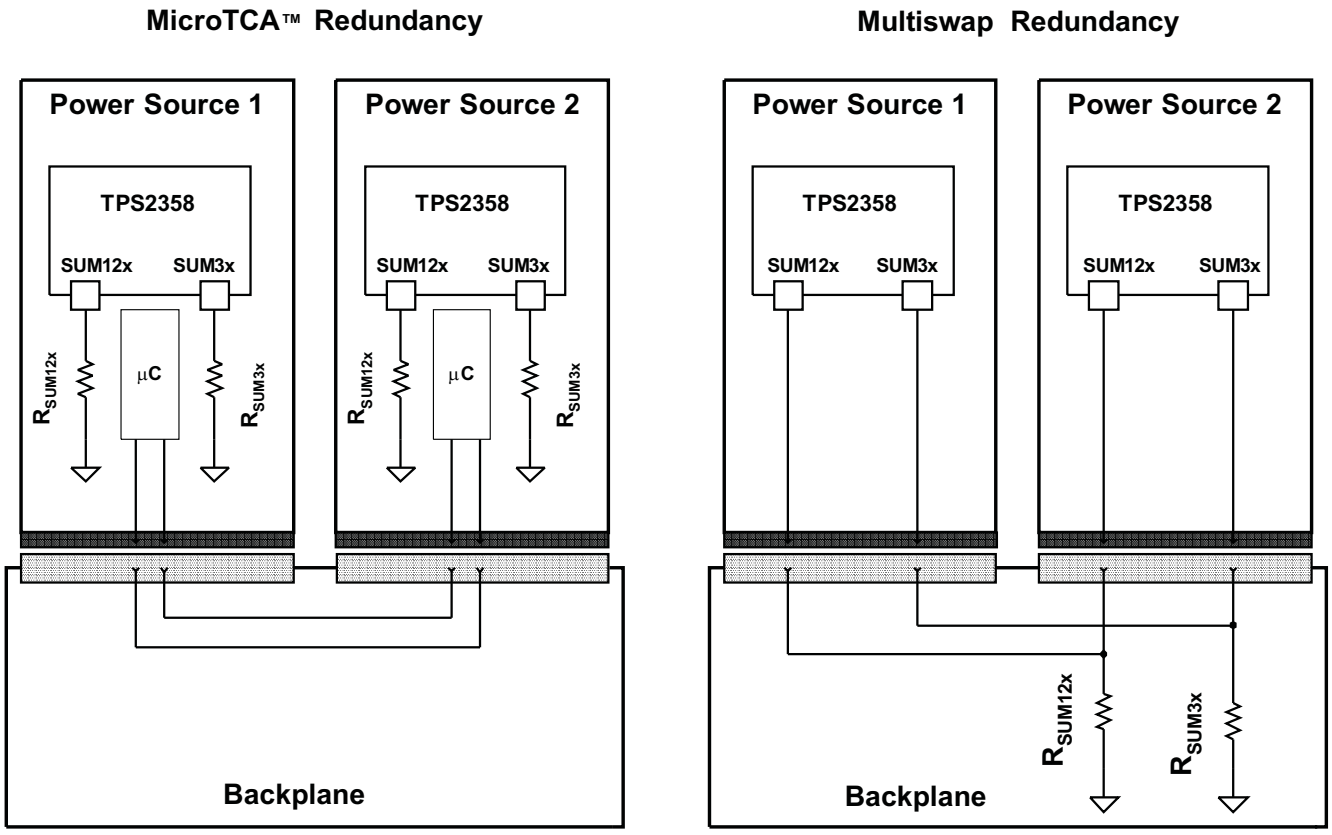


Figure 22. MicroTCA™ Redundancy vs. Multiswap Redundancy

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12-V Inrush Slew Rate Control

As normally configured, the turn-on slew rate of the 12-V channel output voltage V_{OUT} equals:

$$\frac{dV_{out}}{dt} \cong \frac{I_{src}}{C_g} \quad (8)$$

where I_{SRC} equals the current sourced by the PASSx pin (nominally 30 µA) and C_g equals the effective gate capacitance. For purposes of this computation, one can assume that the effective gate capacitance approximately equals the reverse transfer capacitance, C_{RSS}. To reduce the slew rate, increase C_g by connecting additional capacitance from PASSx to ground. Place a resistor of at least 1000 Ω in series with the additional capacitance to prevent it from interfering with the fast turn off of the FET. Due to the current limit function at start up it is unlikely that slew rate control will be required.

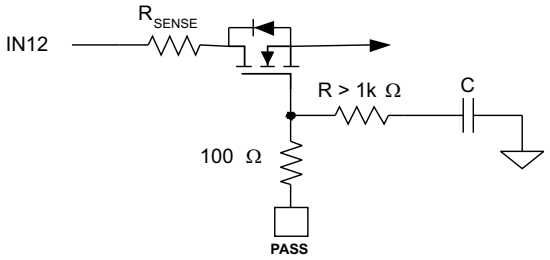


Figure 23. RC Slew Rate Control

12-V ORing Operation for Redundant Systems

The 12-V channels use external pass FETs to provide reverse blocking. The TPS2358 pulls the BLKx pin high when the input-to-output differential voltage VIN12x-OUT12x exceeds a nominal value of 10 mV, and it pulls the pin low when this differential falls below a nominal value of -3 mV. These thresholds provide a nominal 13 mV of hysteresis to help prevent false triggering (Figure 24).

The source of the blocking FET connects to the source of the pass FET, and the drain of the blocking FET connects to the load. This orients the body diode of the blocking FET such that it conducts forward current and blocks reverse current. The body diode of the blocking FET does not normally conduct current because the FET turns on when the voltage differential across it exceeds 10 mV.

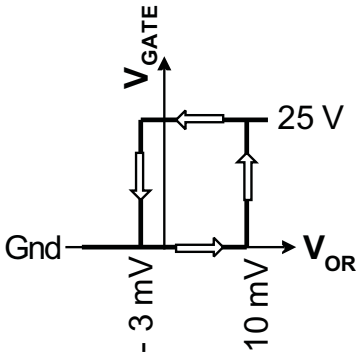


Figure 24. ORing Thresholds

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Using the TPS2358 to Control Two AdvancedMC™ Slots

The TPS2358 has been designed for use on ATCA Carrier boards with a minimum number of external components. Carrier boards do not usually have redundant 3.3-V or 12-V supplies, so it is not necessary to provide ORing functions in the power supply feeds. Consequently, the external 12-V ORing FETs have been omitted and the BLKx pins are left unconnected.

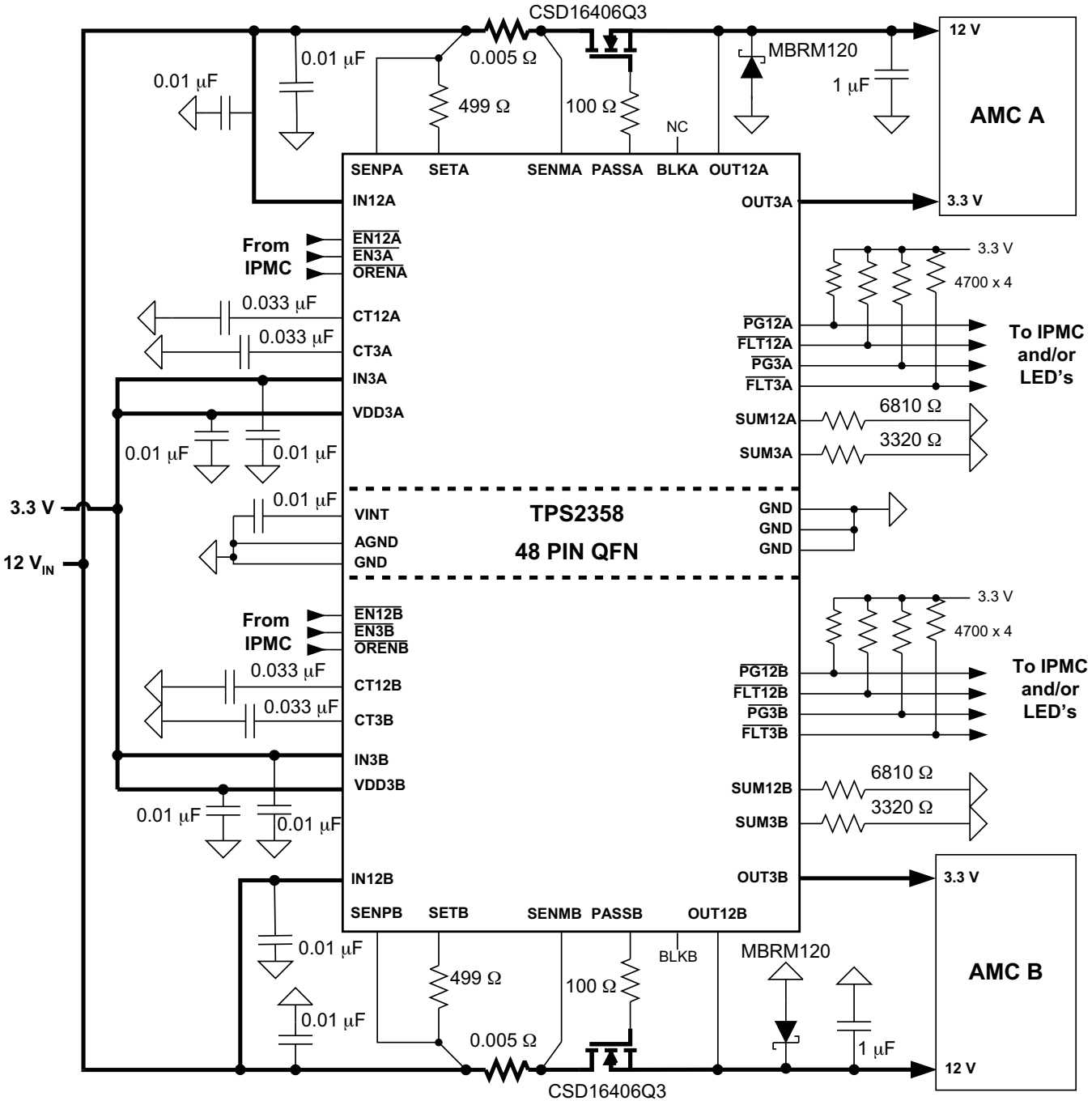


Figure 25. Block Diagram of TPS2358 In a Non-Redundant System

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Layout Considerations

TPS2358 applications require layout attention to ensure proper performance and minimize susceptibility to transients and noise. In general, all runs should be as short as possible but the list below deserves first consideration.

1. Decoupling capacitors on IN12A, IN12B, IN3A, and IN3B should have minimal length to the pin and to GND.
2. SENMx and SENPx runs must be short and run side by side to maximize common mode rejection. Kelvin connections should be used at the points of contact with R_{SENSE} (Figure 26).
3. SETx runs need to be short on both sides of R_{SET}.
4. These runs should be as short as possible and sized to carry at least 20 Amps, more if possible.
   (a) Runs on both side of R_{SENSE}.
   (b) Runs from the drains and sources of the external FETs.
5. Runs from the BLK FETs to OUT12x should be as short as possible.
6. Runs connecting to IN3x and OUT3x should be sized for 1 Amp or more.
7. Connections to GND and SUMx pins should be minimized after the runs above have been placed.
8. The device dissipates low to average power so soldering the powerpad to the board is not a requirement. However, doing so will improve thermal performance and reduce susceptibility to noise.

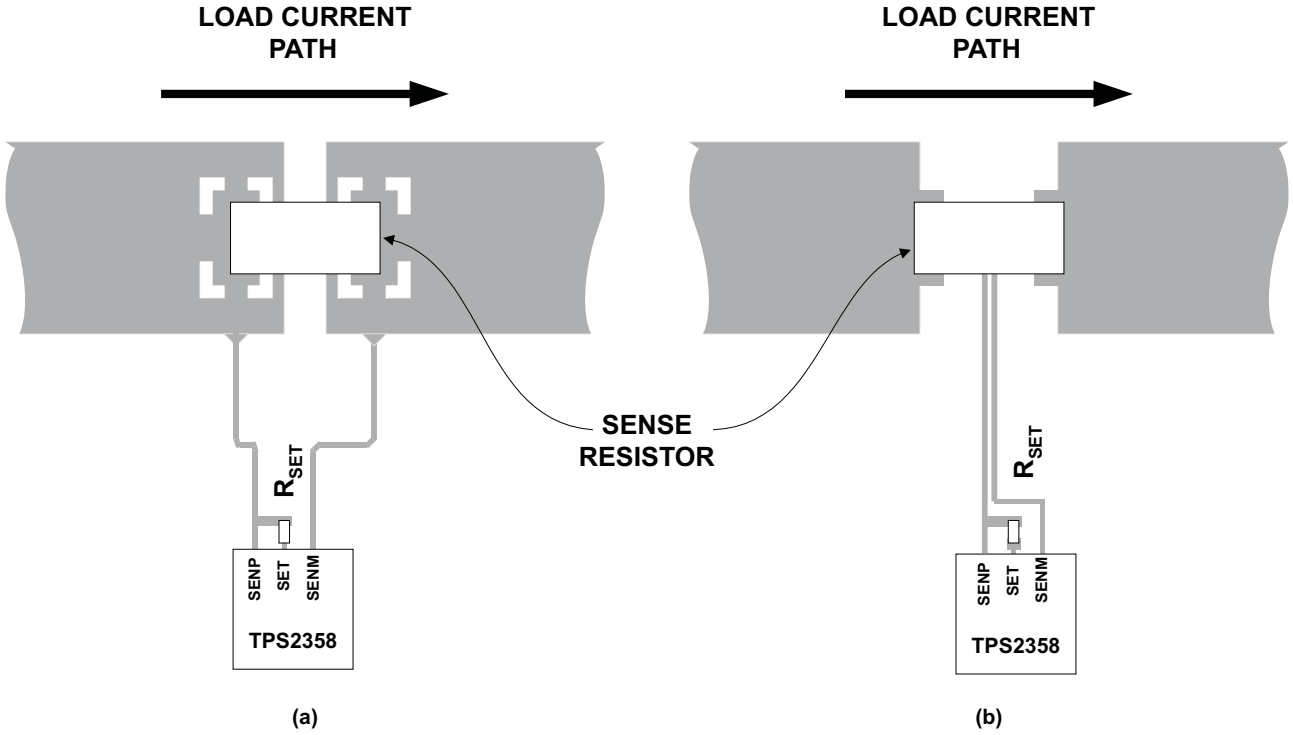


Figure 26. Recommended R_{SENSE} Layout

NOTE

Additional details omitted for clarity.

Transient Protection

TPS2358 devices in deployed systems are not likely to have long, inductive feeds or long load wires. However, it is always advised that an analysis be performed to determine the need for transient protection. When the TPS2358 interrupts current flow, any inductance on the input will tend to cause a positive voltage spike on the input, and any inductance on the output will tend to cause a negative voltage spike on the output. The following equations allow the designer to make a reasonably accurate prediction of the voltage spike due to interruptions in current.

$$V_{SPIKE} = V_{NOM} + I_{LOAD}\sqrt{L/C} \tag{9}$$

where:

- V_{NOM} = nominal voltage at terminal being analyzed
- L = combined inductance of feed and R_{TN} lines
- C = capacitance at point of disconnect
- I_{LOAD} = current through terminal at $T_{DISCONNECT}$
- $$L_{STRAIGHTWIRE} \sim \left[0.2 \times length \times ln\left(\frac{4 \times length}{diameter}\right) - 0.75\right] \; nH$$

This equation can be used to calculate the capacitance required to limit the voltage spike to a desired level above the nominal voltage:

$$C = \frac{LI^2}{(V_{SPIKE} - V_{NOM})^2} \tag{10}$$

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Output Protection Considerations for MicroTCA Power Systems

MicroTCA Power systems have particular transient protection requirements because of the basic power architecture. Traditional protection methods must be adjusted to accommodate these systems where the supplies are OR'ed together after the inrush control and current limit circuits. However, minor changes to some standard techniques will yield very good results.

Unlike systems which have hotswap/inrush control at the load, uTCA power modules and their hot swap circuitry are often a significant distance (up to 1 m of trace length, two way) from the load module. Even with the best designed backplanes this distance results in stray inductance which will store energy while current is being delivered to the load. The inductive energy can cause large negative voltage spikes at the power module output when the current is switched off under load. The spikes become especially severe when the channel shuts off due to a short circuit, which drives the current well above normal levels at shut off.

The lowest voltage allowed on the device pins is -0.3 V. If a transient makes a pin more negative than -0.3 V the internal ESD diode attached to the pin will become forward biased and current will be conducted across the substrate to the ground pins. This current may disrupt normal operation or, if large enough, damage the silicon. Typical protection solutions involve capacitors, TVSs (Transient Voltage Suppressors) and/or a Schottky diode to absorb the energy which appears at the power module output in the form of a large negative voltage spike.

The Risk With Output Capacitors

Putting transient filter capacitors at the output of a uTCA power module can cause nuisance trips when that power module is plugged into an active bus. If there is no series resistance with the capacitor and the bus is low impedance an inrush surge can cause the active supply to "detect" a short circuit and shut down. One possible solution is to put a few Ohms of resistance in series with the cap to limit inrush below the fast trip level. A better solution is to put a Schottky diode across the output to clamp the transient energy and shunt it to ground as shown in Figure 27. Although the Schottky diode will absorb most of the energy, the extremely fast di/dt at shutoff allows some of the leading edge energy to couple through the parasitic capacitances of the hotswap FET and the ORing FET, (C_{DS}, C_{GS}, C_{GD}) and into the BLK and GATE pins. Protection for these pins is provided by 100-Ω GATE resistors which have little effect on normal operation but provide good isolation during transient events.

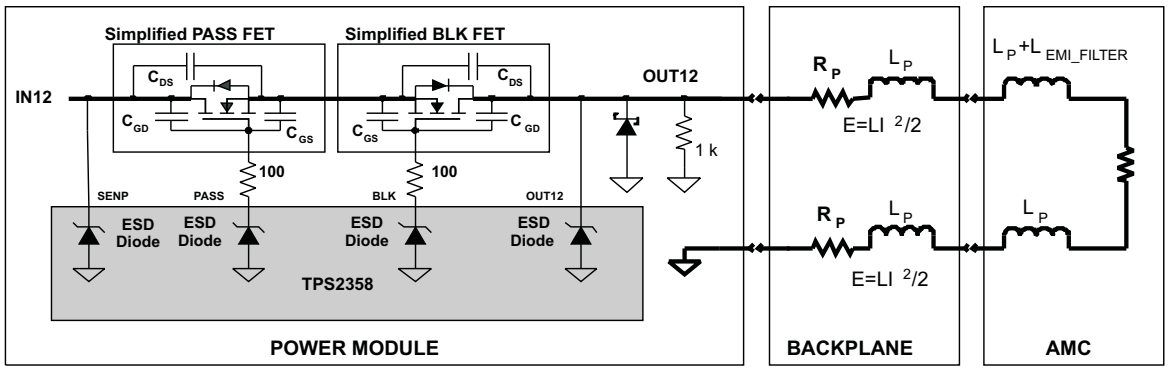


Figure 27. Figure 32 Parasitic Inductance and Transient Protection

Output Bleed Down Resistance

When the TPS2358 commands the 12-V channel off there is a small leakage current sourced by the OUT12 pin. If this leakage is ignored it can eventually charge any external capacitance to approximately 6 V. In some systems this may be acceptable but, if not, the leakage can be bled to GND by a 1-kΩ resistor from OUT12 to GND will suffice. Maximum leakage is around 23 µA and can be modeled as a 6-V source in series with a 280-kΩ resistor.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2358RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS2358	Samples
TPS2358RGZRG4	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS2358	Samples
TPS2358RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS2358	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

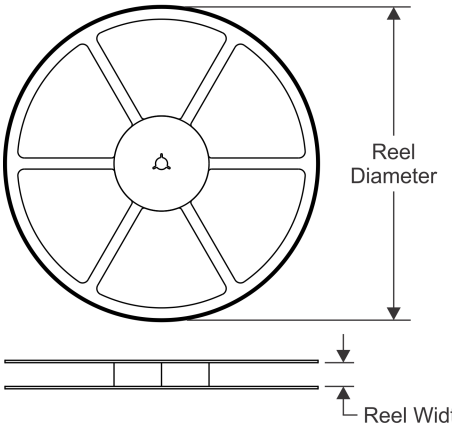
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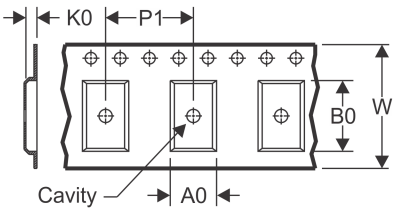
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

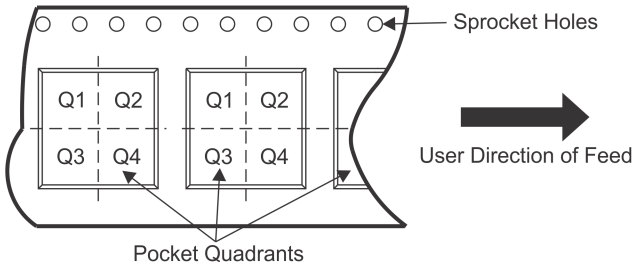


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

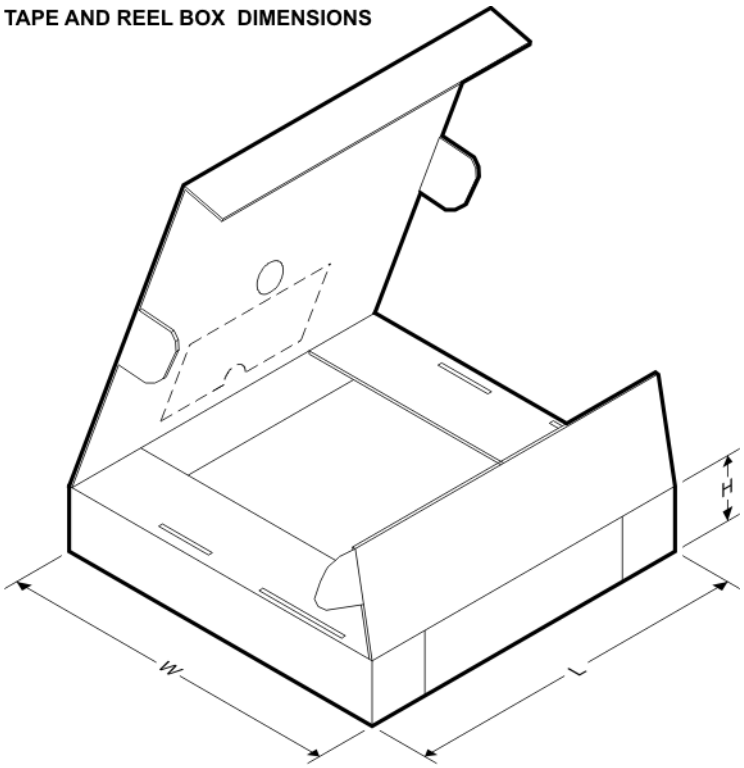
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2358RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
TPS2358RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

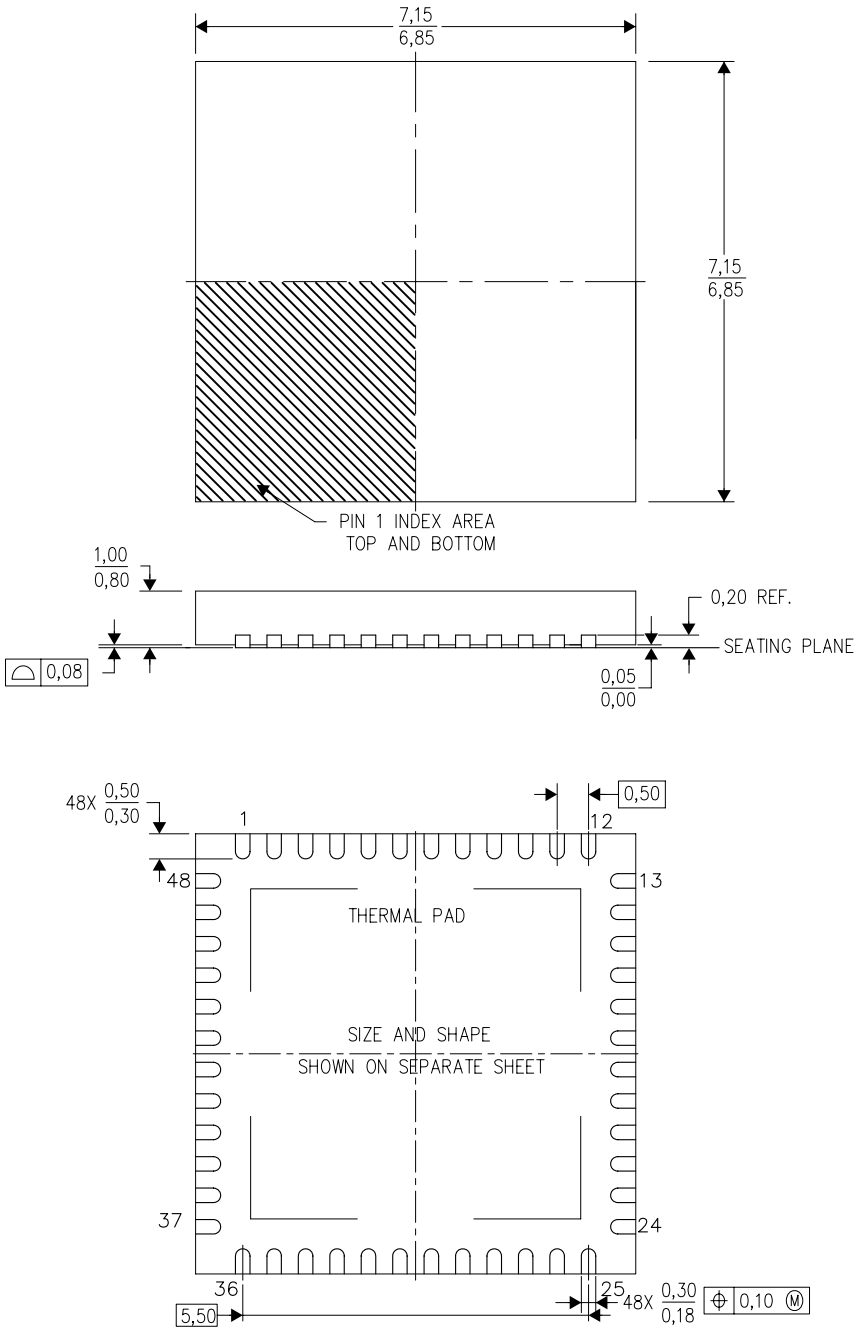
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2358RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
TPS2358RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

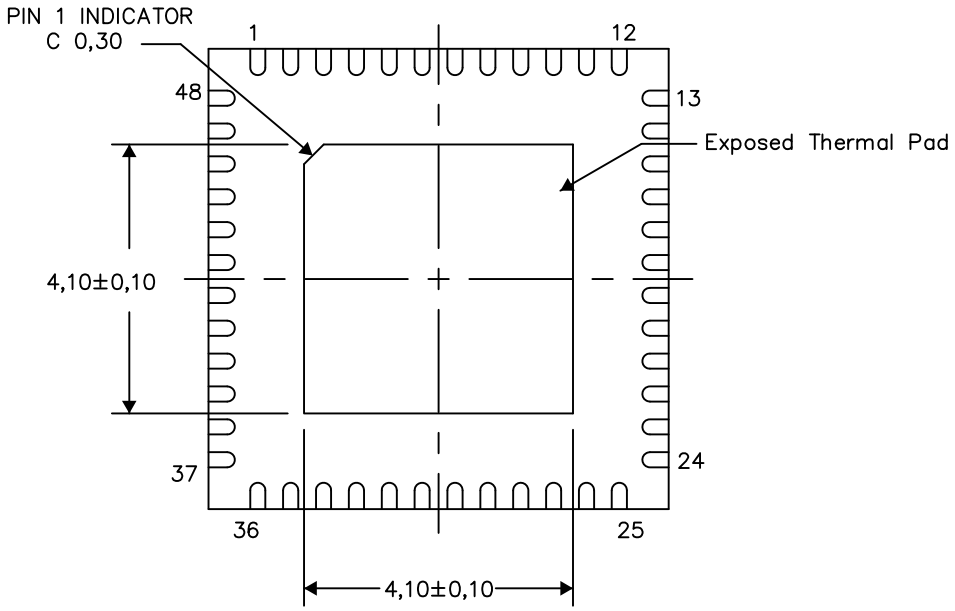
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



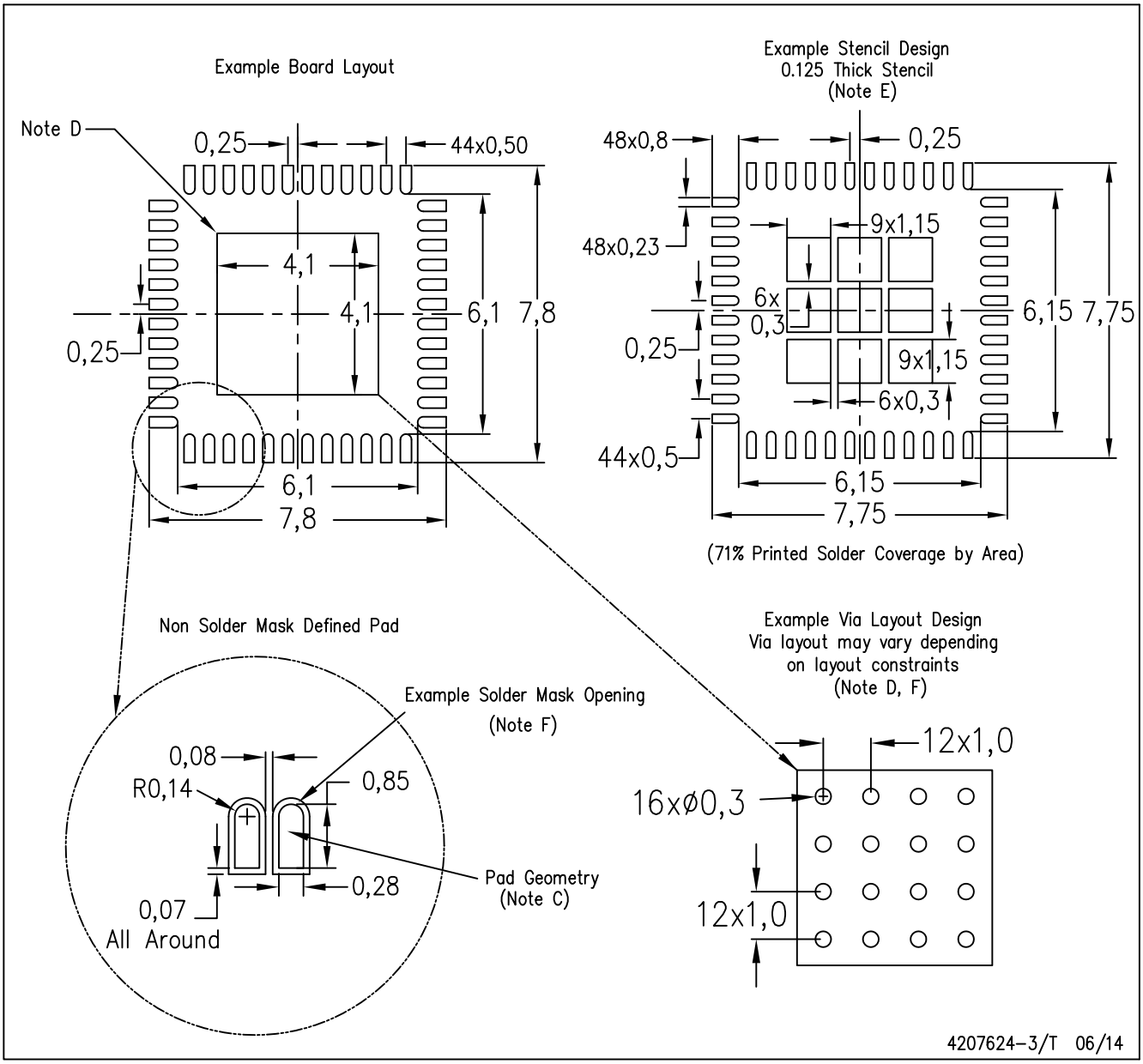
Bottom View

Exposed Thermal Pad Dimensions

4206354–3/Z 03/15

NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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