STL8N6LF3-VB Datasheet

N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	60
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.024
$R_{DS(on)}$ (Ω) at V_{GS} = 4.5 V	0.028
Q_g typ. (nC)	5.2
I_D (A)	15[a, g]
Configuration	Single

FEATURES

- **Halogen-free According to IEC 61249-2-21 Available**
- Trench Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested

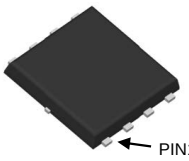
Pb-free
RoHS
COMPLIANT

APPLICATIONS

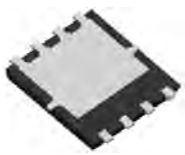
- Battery Switch
- DC/DC Converter

DFN5X6

Top View

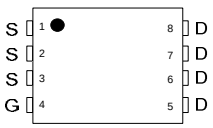


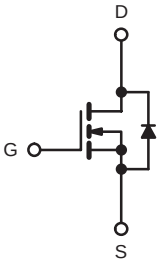
Bottom View



PIN1

Top View





N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-source voltage		V_{DS}	60	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	15 [a]	A
	T_C = 70 °C		9[a]	
	T_A = 25 °C		10.3 [b, c]	
	T_A = 70 °C		8.1 [b, c]	
Pulsed drain current (t = 100 µs)		I_{DM}	40	
Continuous source-drain diode current	T_C = 25 °C	I_S	12 [a]	
	T_A = 25 °C		3 [b, c]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	15	
Single pulse avalanche energy		E_{AS}	11.3	mJ
Maximum power dissipation	T_C = 25 °C	P_D	35.7	W
	T_C = 70 °C		22.9	
	T_A = 25 °C		3.6 [b, c]	
	T_A = 70 °C		2.3 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [c]			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		**SYMBOL**	**TYPICAL**	**MAXIMUM**	**UNIT**
Maximum junction-to-ambient [b]	t ≤ 10 s	R_{thJA}	25	35	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	2.7	3.5	

Notes
a. Package limited
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s

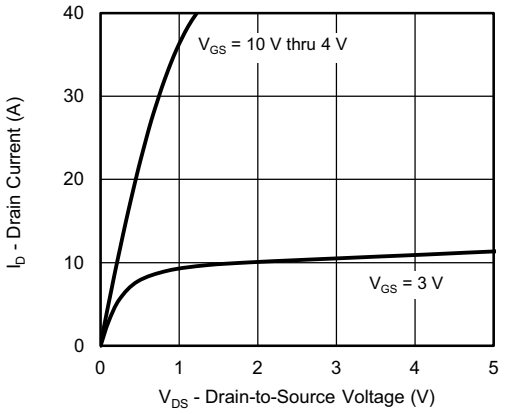
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	60	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	-	33	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	-4.8	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1	-	2.8	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 70 °C	-	-	10	
On-state drain current [a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} =10 V	10	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} =10 V, I_D = 10 A	-	0.024	-	Ω
		V_{GS} = 4.5 V, I_D = 5 A	-	0.028	-	
Forward transconductance [a]	g_{fs}	V_{DS} = 10 V, I_D = 10 A	-	39	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = 30 V, V_{GS} = 0 V, f = 1 MHz	-	790	-	pF
Output capacitance	C_{oss}		-	330	-	
Reverse transfer capacitance	C_{rss}		-	14	-	
Total gate charge	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 5 A	-	11.1	17	nC
		V_{DS} = 30 V, V_{GS} = 4.5 V, I_D = 5 A	-	5.2	8	
Gate-source charge	Q_{gs}		-	2.2	-	
Gate-drain charge	Q_{gd}		-	1.1	-	
Gate resistance	R_g	f = 1 MHz	0.1	0.6	1.2	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 6 Ω, I_D ≅ 5 A, V_{GEN} = 10 V, R_g = 1 Ω	-	7	15	ns
Rise time	t_r		-	21	40	
Turn-off delay time	$t_{d(off)}$		-	10	20	
Fall time	t_f		-	10	20	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 6 Ω, I_D ≅ 5 A, V_{GEN} = 4.5 V, R_g = 1 Ω	-	13	25	
Rise time	t_r		-	25	50	
Turn-off delay time	$t_{d(off)}$		-	10	20	
Fall time	t_f		-	22	45	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	15	-	A
Pulse diode forward current	I_{SM}		-	-	40	
Body diode voltage	V_{SD}	I_S = 5 A, V_{GS} = 0 V	-	0.79	1.2	V
Body diode reverse recovery time	t_{rr}	I_F = 5 A, di/dt = 100 A/µs, T_J = 25 °C	-	30	60	ns
Body diode reverse recovery charge	Q_{rr}		-	60	120	nC
Reverse recovery fall time	t_a		-	15	-	ns
Reverse recovery rise time	t_b		-	15	-	

Notes

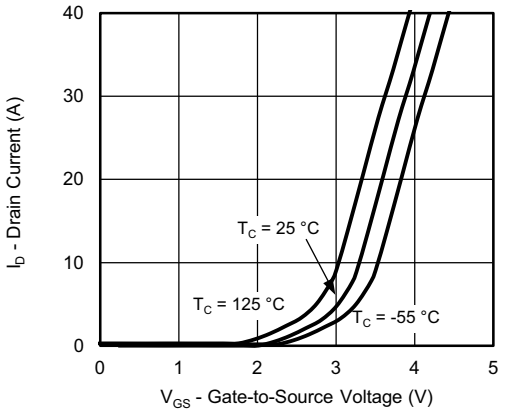
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

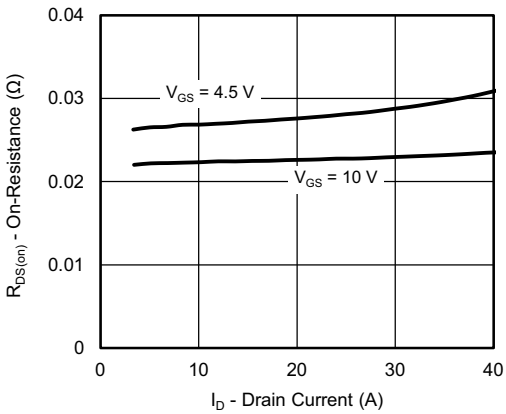
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



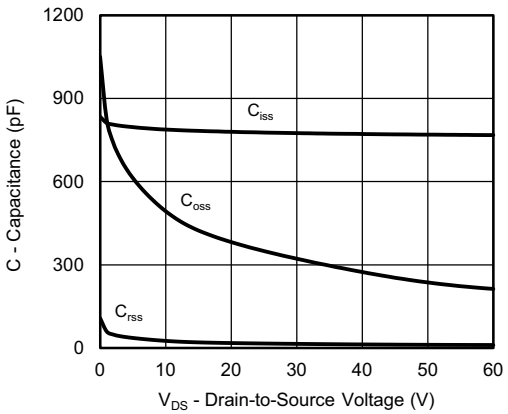
Output Characteristics



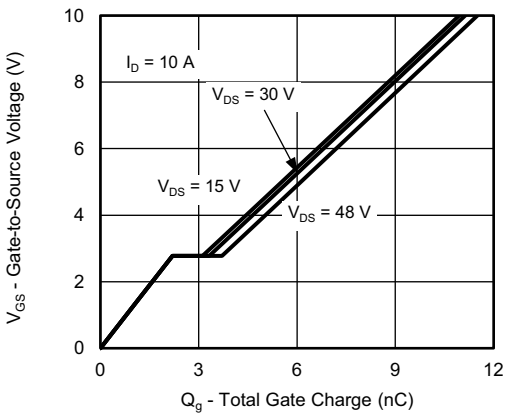
Transfer Characteristics



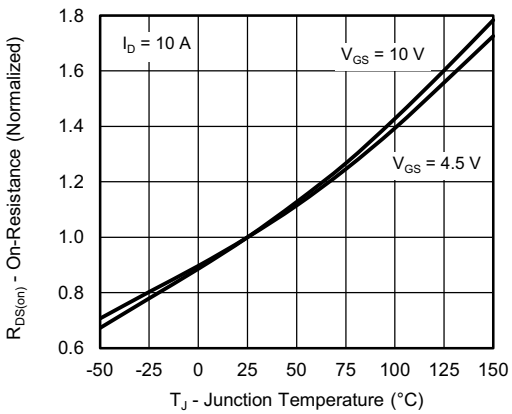
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

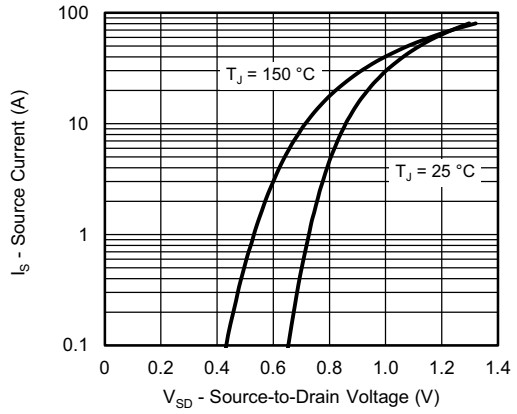


Gate Charge

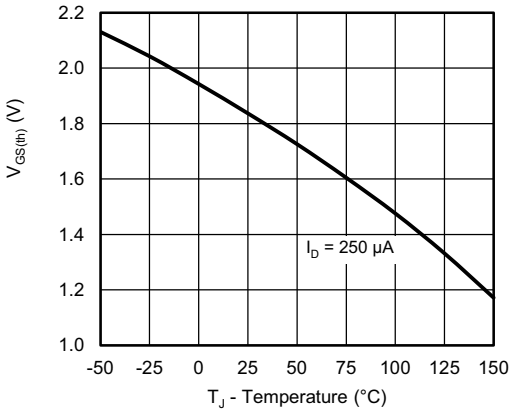


On-Resistance vs. Junction Temperature

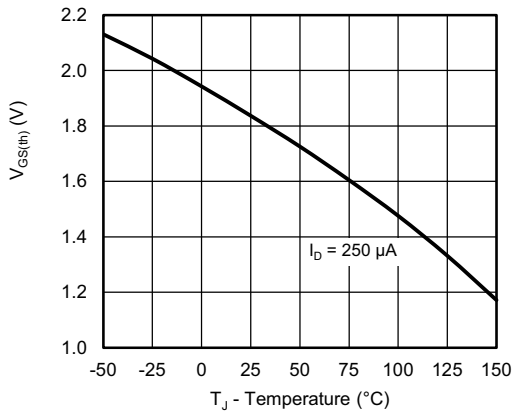
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



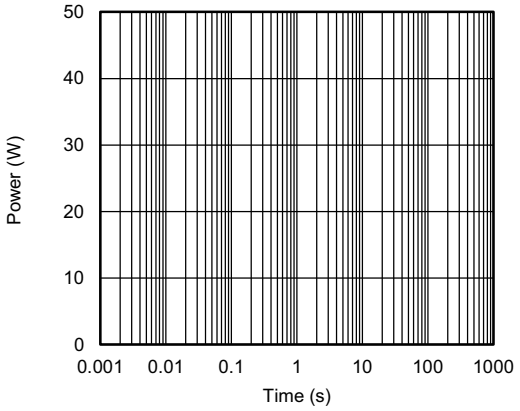
Source-Drain Diode Forward Voltage



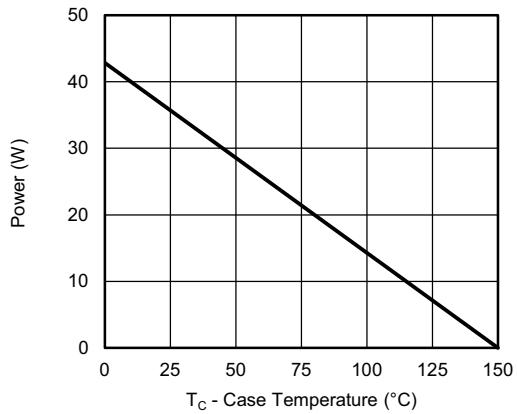
Threshold Voltage



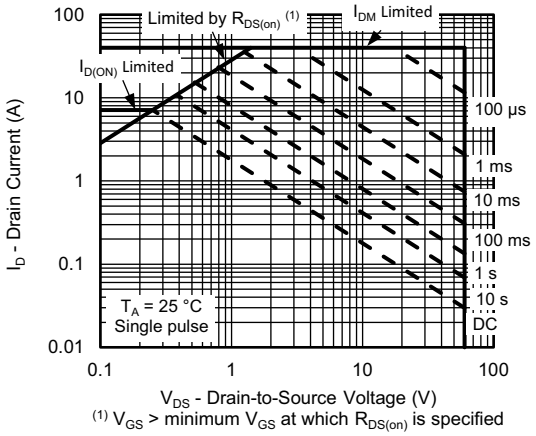
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

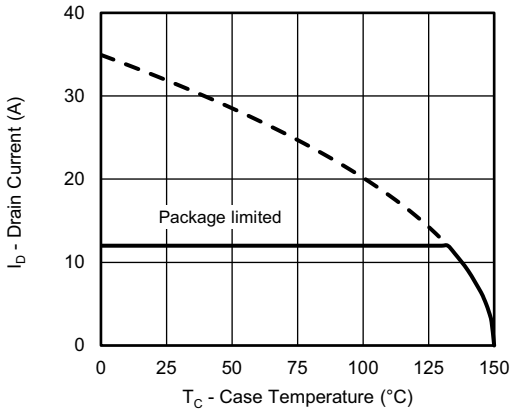


Power, Junction-to-Case



Safe Operating Area, Junction-to-Ambient

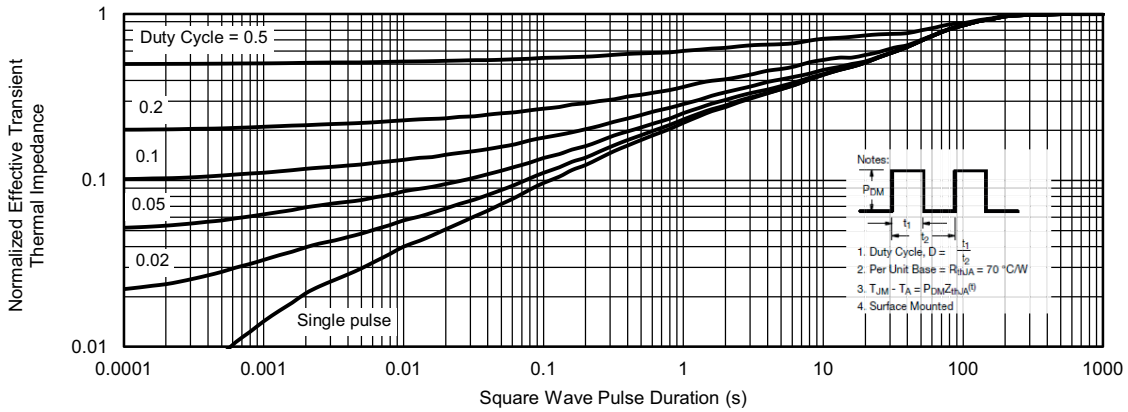
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



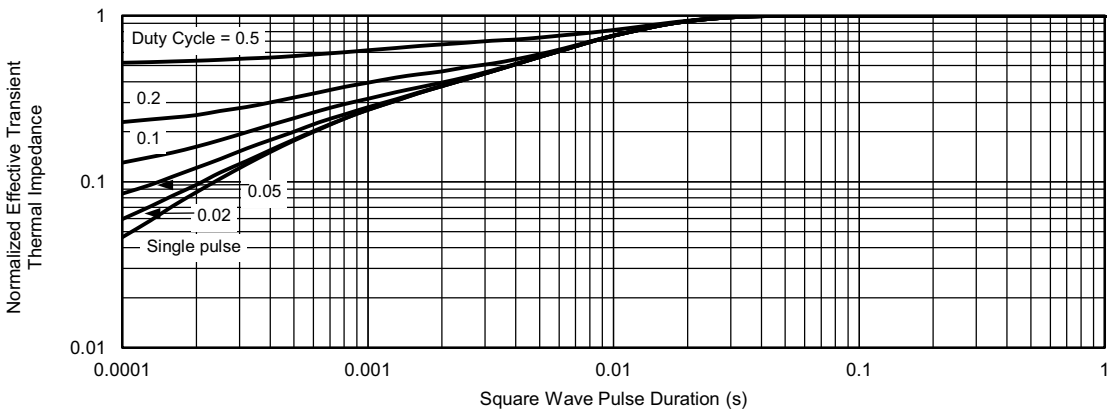
Current Derating [a]

Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

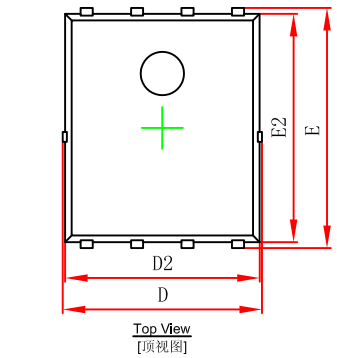


Normalized Thermal Transient Impedance, Junction-to-Ambient

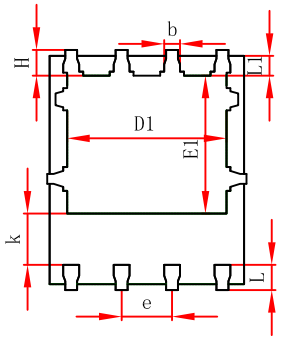


Normalized Thermal Transient Impedance, Junction-to-Foot

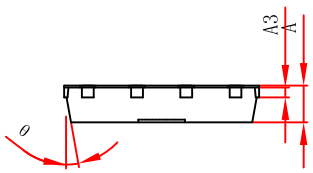
PDFNWB5x6-8L Package Outline Dimensions



Top View
[顶视图]



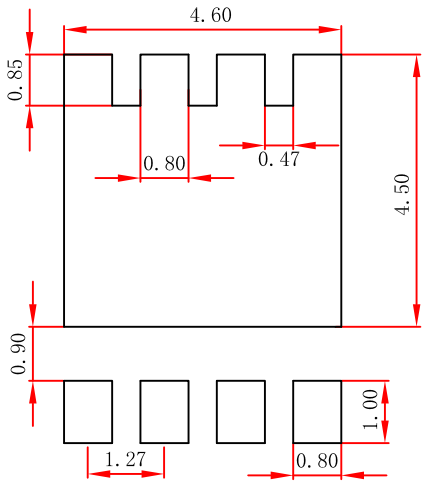
Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.	0.	0.	0.
L1	5590.	7110.	0220.	0280.
H	4240.	5760.	0170.	0230.
θ	574	726	023	029
	10°	12°	10°	12°

PDFNWB5x6-8L Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

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