TSM9926DCS RL-VB Datasheet

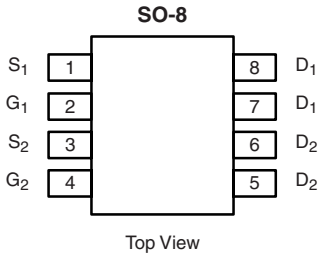
Dual N-Channel 20-V (D-S) MOSFET

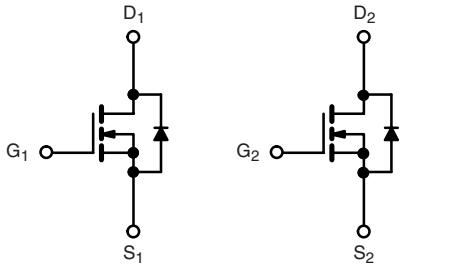
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
20	0.019 at V_{GS} = 4.5 V	7.1
	0.026 at V_{GS} = 2.5 V	6.0

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- Trench Power MOSFET
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available





ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	7.1	A
	T_A = 70 °C		5.7	
Pulsed Drain Current (10 µs Pulse Width)		I_{DM}	40	
Continuous Source Current (Diode Conduction)[a]		I_S	1.7	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	2	W
	T_A = 70 °C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS			
Parameter	**Symbol**	**Limit**	**Unit**
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

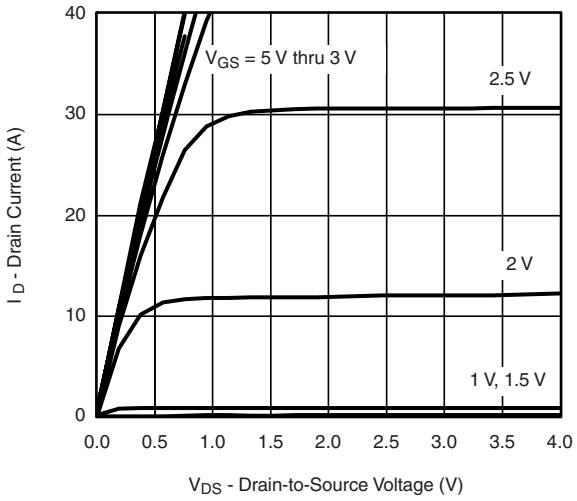
Notes:
a. Surface Mounted on FR4 board, t ≤ 10 s.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.6		1.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55 °C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 4.5 V	20			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 7.1 A		0.019		Ω
		V_{GS} = 2.5 V, I_D = 6.0 A		0.026		
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 7.1 A		27		S
Diode Forward Voltage[a]	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V			1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 7.1 A		9.5		nC
Gate-Source Charge	Q_{gs}			1.5		
Gate-Drain Charge	Q_{gd}			2.5		
Gate Resistance	R_g	f = 1 MHz		1.6	2.7	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_g = 10Ω		10		ns
Rise Time	t_r			15		
Turn-Off Delay Time	$t_{d(off)}$			38		
Fall Time	t_f			25		
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.7 A, dI/dt = 100 A/µs		26		

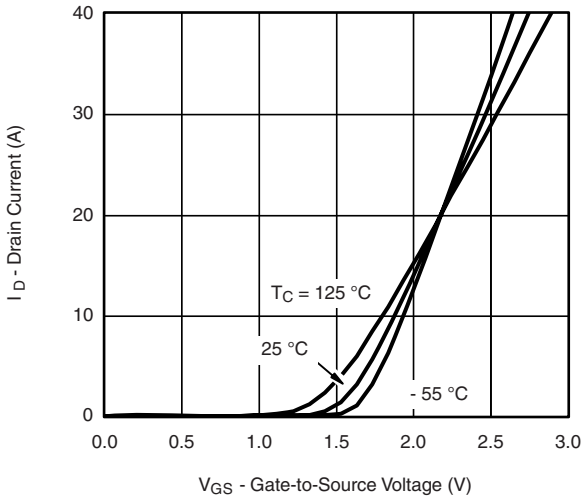
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

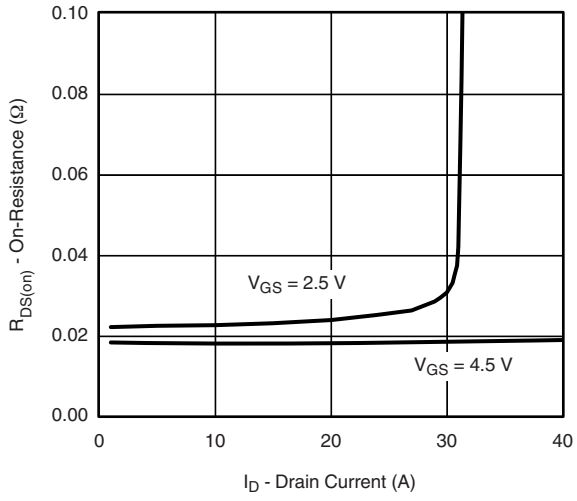
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



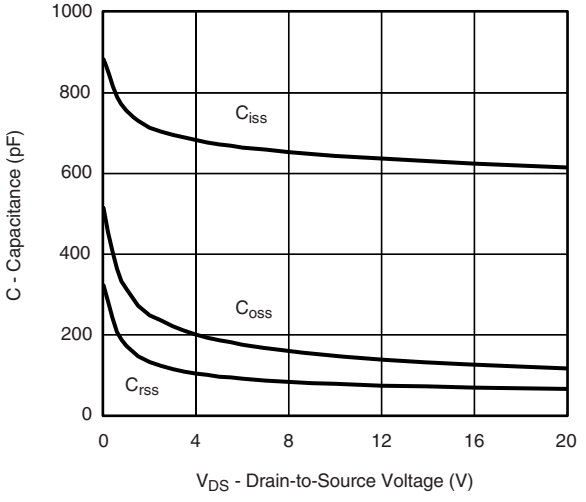
Output Characteristics



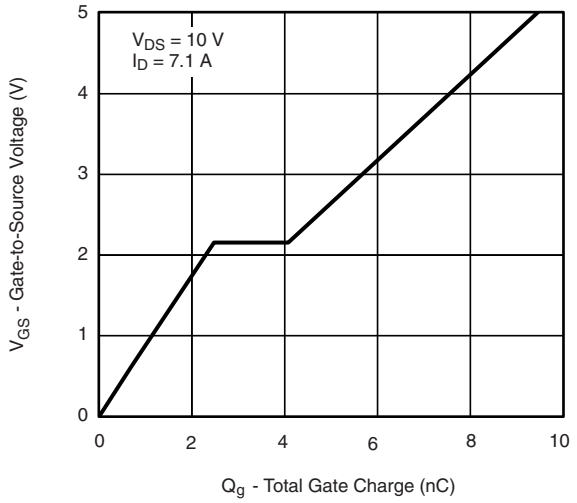
Transfer Characteristics



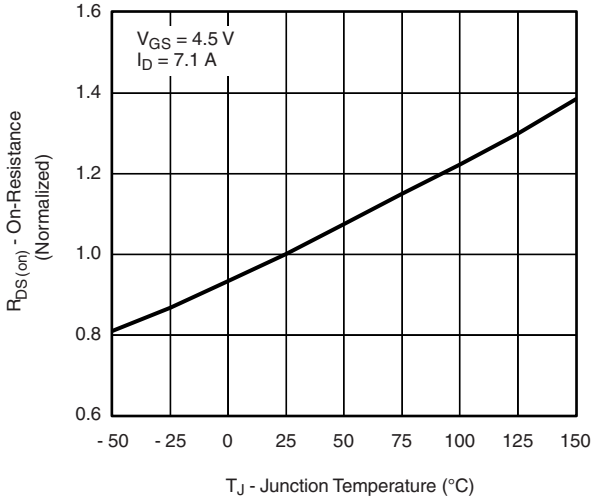
On-Resistance vs. Drain Current



Capacitance

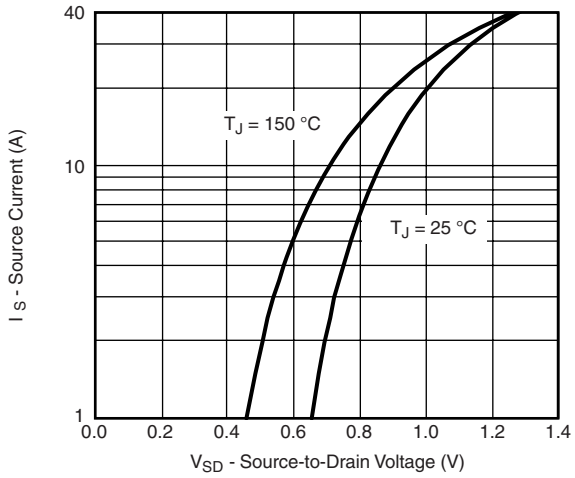


Gate Charge

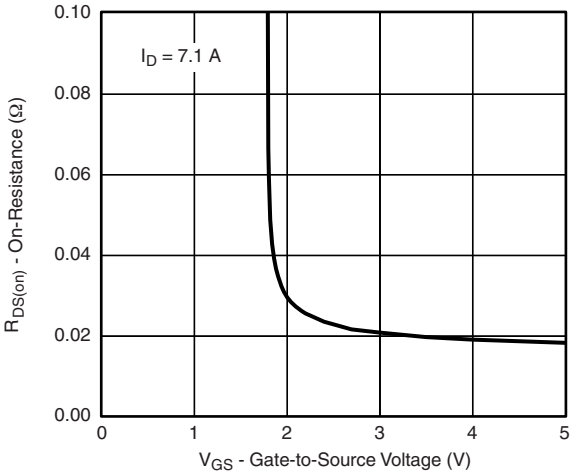


On-Resistance vs. Junction Temperature

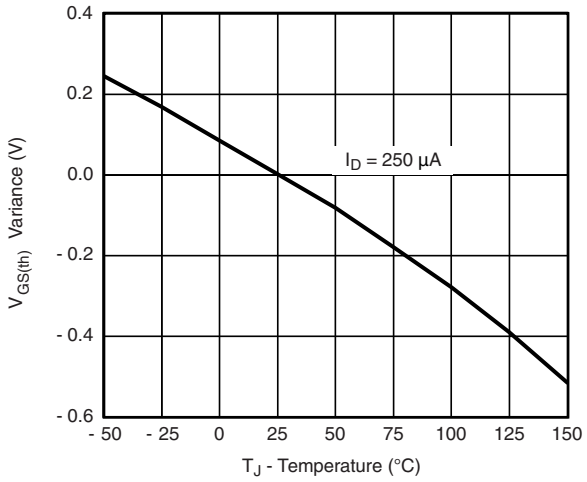
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



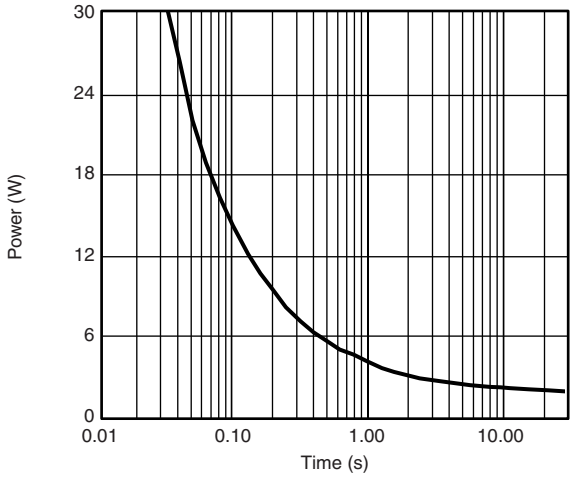
Source-Drain Diode Forward Voltage



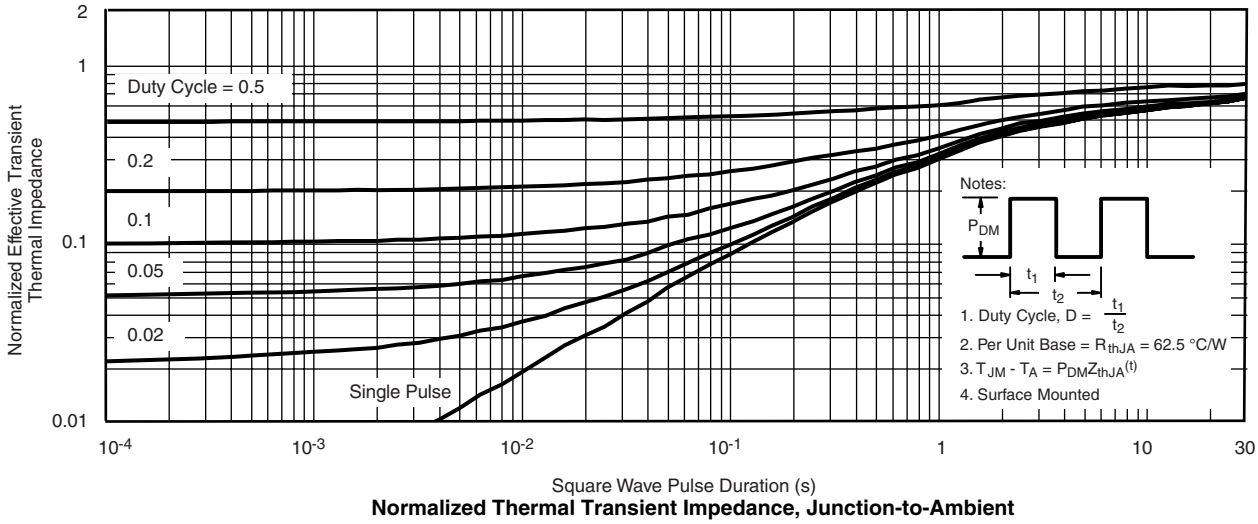
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

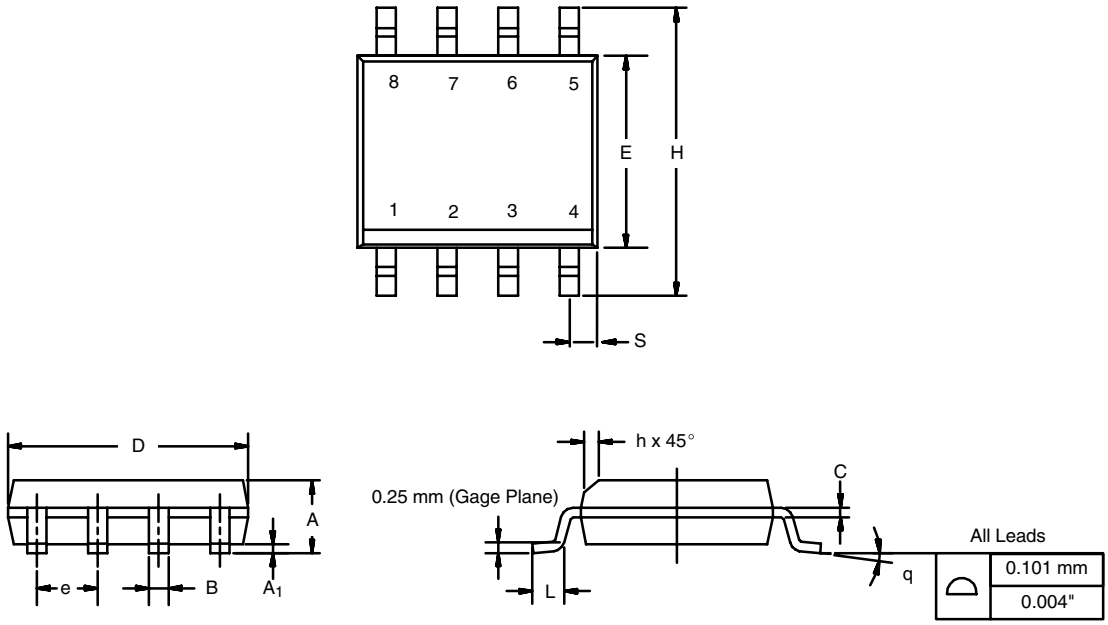


Single Pulse Power



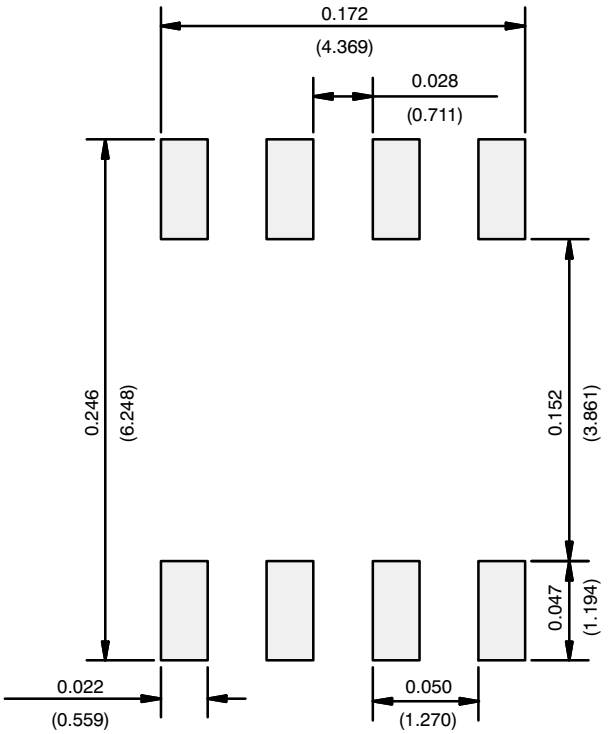
Normalized Thermal Transient Impedance, Junction-to-Ambient

SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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