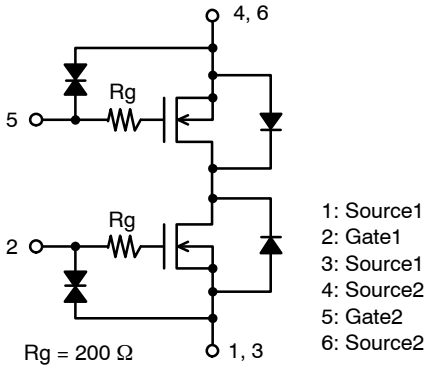
MOSFET – Power, Dual, N-Channel, for 1-2 Cells Lithium-ion Battery Protection

20 V, 4.7 mΩ, 23 A

EFC3J018NUZ

V_{SSS}	$R_{SS(ON)}$ MAX	I_S MAX
20 V	4.7 mΩ @ 4.5 V	23 A
	4.75 mΩ @ 4.0 V	
	4.9 mΩ @ 3.8 V	
	5.4 mΩ @ 3.1 V	
	9.0 mΩ @ 2.5 V	

ELECTRICAL CONNECTION

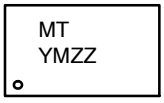


N-Channel



WLCSP6, 1.77 × 3.05
CASE 567KS

MARKING DIAGRAM



MT = Specific Device Code
Y = Year
M = Month
ZZ = Assembly Lot Number

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

Introduction

This Power MOSFET features a low on−state resistance. This device is suitable for applications such as power switches of portable machines. Best suited for 1−2 cells lithium−ion battery applications.

Features

- 2.5 V Drive
- 2 kV ESD HBM
- Common-Drain Type
- ESD Diode-Protected Gate
- This Device is Pb-Free and Halide Free

Applications

- 1-2 Cells Lithium-ion Battery Charging and Discharging Switch

Specifications

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Value	Unit
Source to Source Voltage	V_{SSS}	20	V
Gate to Source Voltage	V_{GSS}	±12	V
Maximum Operating Gate to Source Voltage (Note 1)	$V_{GSS(OP)}$	±8	V
Source Current (DC)	I_S	23	A
Source Current (Pulse) PW ≤ 100 μs, duty cycle ≤ 1%	I_{SP}	100	A
Total Dissipation (Note 2)	P_T	2.5	W
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Functional operation above the stresses listed in the recommended operating ranges is not implied. Extended exposure to stresses beyond the recommended operating ranges limits may affect device reliability.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction to Ambient (Note 2)	$R_{\theta JA}$	50	°C/W

2. Surface mounted on ceramic substrate (5000 $mm^2 \times 0.8$ mm).

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ELECTRICAL CHARACTERISTICS (T_A = 25°C) (Note 3)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source to Source Breakdown Voltage	$V_{(BR)SSS}$	I_S = 1 mA, V_{GS} = 0 V (Figure 1)	20	–	–	V
Zero-Gate Voltage Source Current	I_{SSS}	V_{SS} = 20 V, V_{GS} = 0 V (Figure 1)	–	–	1	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±8 V, V_{SS} = 0 V (Figure 2)	–	–	±1	μA
Gate Threshold Voltage	V_{GS}(th)	V_{SS} = 10 V, I_S = 1 mA (Figure 3)	0.5	–	1.3	V
Static Source to Source On-State Resistance	R_{SS}(on)	I_S = 5 A, V_{GS} = 4.5 V (Figure 4)	2.5	3.6	4.7	mΩ
		I_S = 5 A, V_{GS} = 4.0 V (Figure 4)	2.56	3.65	4.75	mΩ
		I_S = 5 A, V_{GS} = 3.8 V (Figure 4)	2.6	3.75	4.9	mΩ
		I_S = 5 A, V_{GS} = 3.1 V (Figure 4)	2.9	4.15	5.4	mΩ
		I_S = 5 A, V_{GS} = 2.5 V (Figure 4)	3.3	4.75	9.0	mΩ
Turn-ON Delay Time	t_d(on)	V_{SS} = 10 V, V_{GS} = 4.5 V, I_S = 3 A (Figure 5)	–	280	–	ns
Rise Time	t_r		–	890	–	ns
Turn-OFF Delay Time	t_d(off)		–	4100	–	ns
Fall Time	t_f		–	2800	–	ns
Total Gate Charge	Qg	V_{SS} = 10 V, V_{GS} = 4.5 V, I_S = 23 A (Figure 6)	–	75	–	nC
Forward Source to Source Voltage	$V_{F(S-S)}$	I_S = 3 A, V_{GS} = 0 V (Figure 7)	–	0.74	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Refer to the JIS 7030 measuring methods for transistors for measuring.

Test Circuits are Example of Measuring FET1 Side

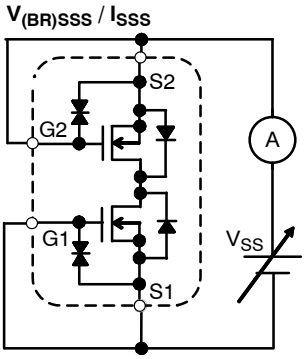
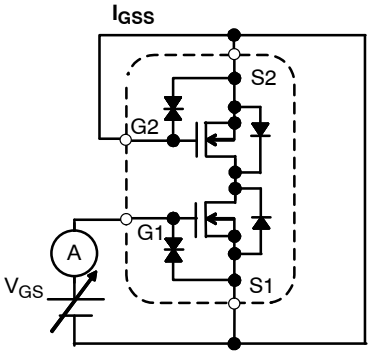
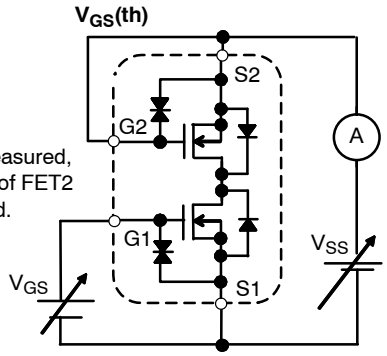


Figure 1. Test Circuit 1



When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 2. Test Circuit 2



When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 3. Test Circuit 3

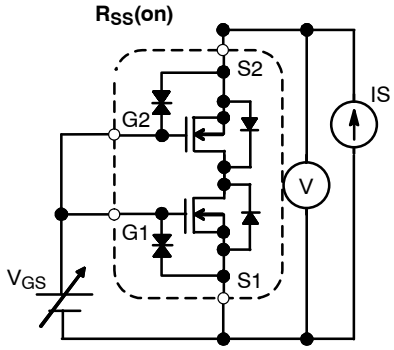
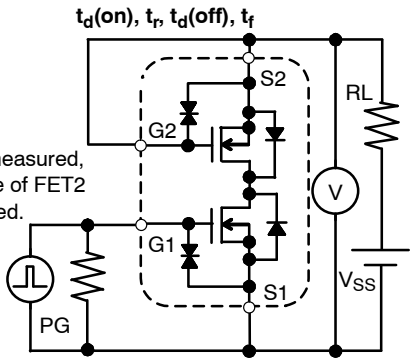
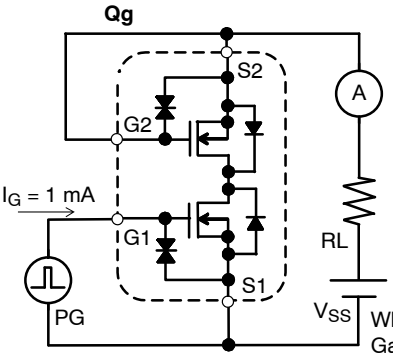


Figure 4. Test Circuit 4



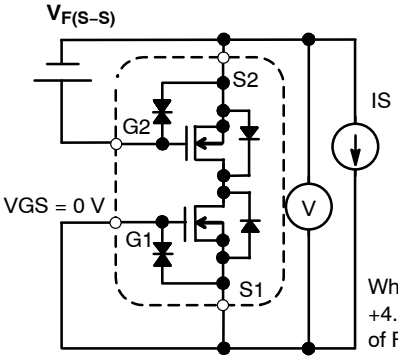
When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 5. Test Circuit 5



When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 6. Test Circuit 6



When FET1 is measured, +4.5 V is added to V_{GS} of FET2.

Figure 7. Test Circuit 7

NOTE: When FET2 is measured, the position of FET1 and FET2 is switched.

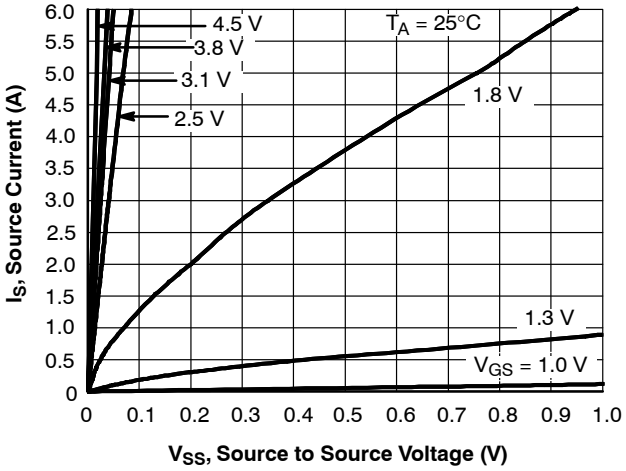


Figure 8. $I_S - V_{SS}$

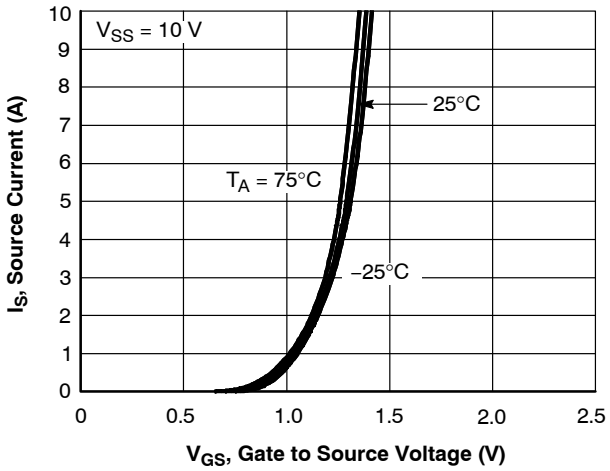


Figure 9. $I_S - V_{GS}$

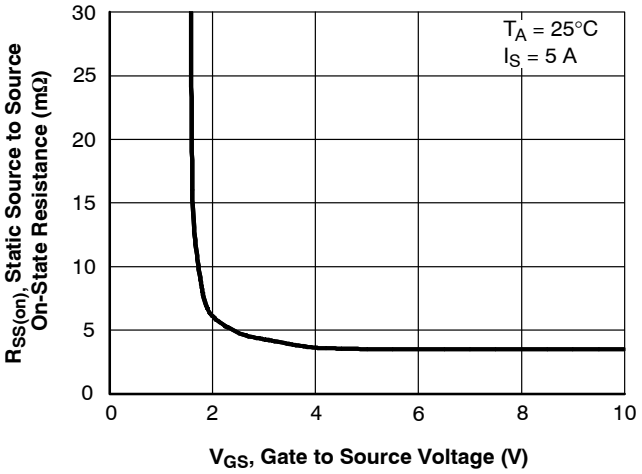


Figure 10. $R_{SS(on)} - V_{GS}$

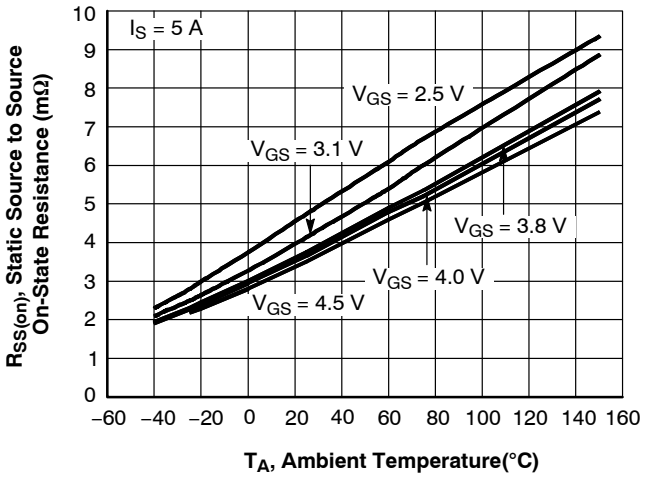


Figure 11. $R_{SS(on)}$ – Ta

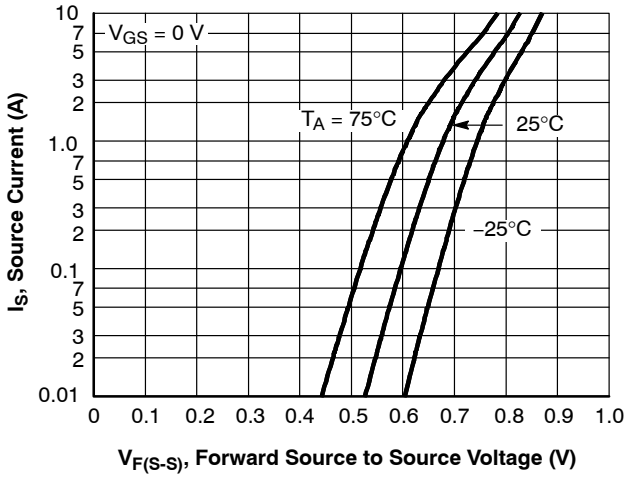


Figure 12. $I_S - V_{F(S-S)}$

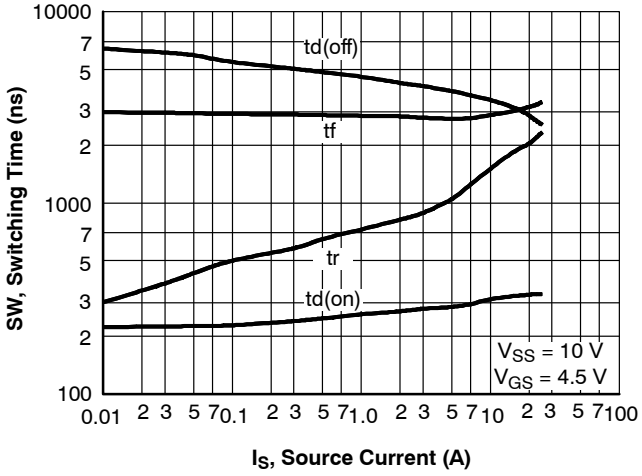


Figure 13. SW Time – I_S

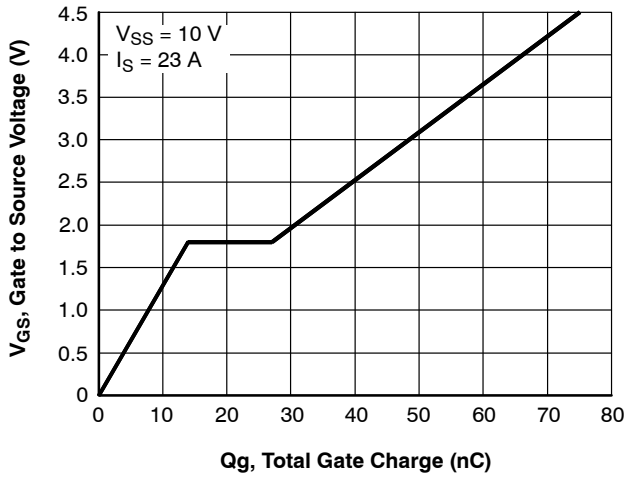


Figure 14. V_{GS} – Qg

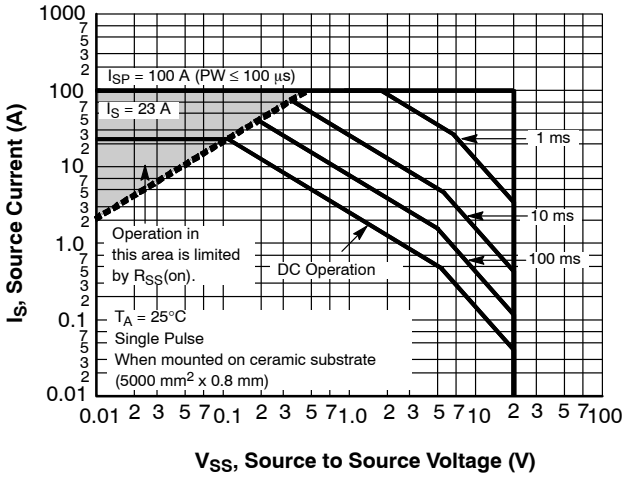


Figure 15. SOA

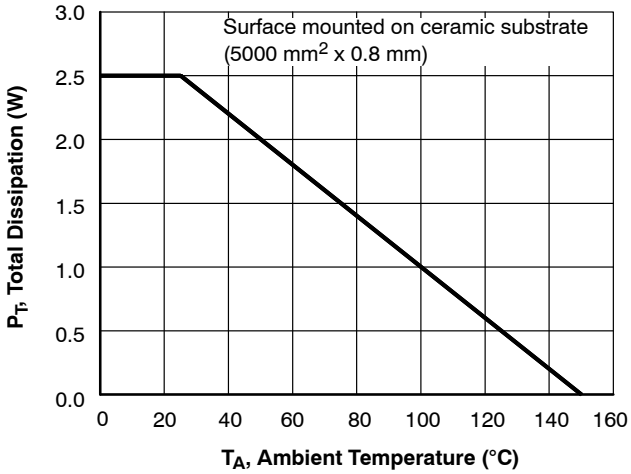


Figure 16. P_T – Ta

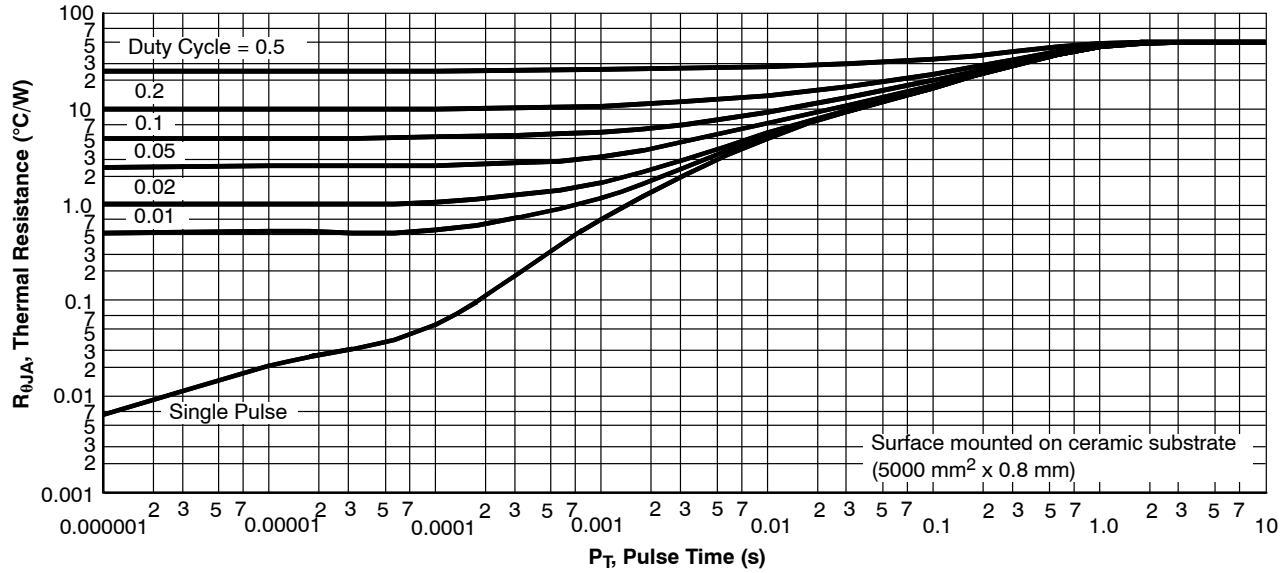


Figure 17. $R_{\theta JA}$ – Pulse Time

ORDERING INFORMATION

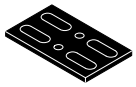
Device	Marking	Package	Shipping† (Qty / Packing)
EFC3J018NUZTDG	MT	WLCSP6, 1.77 × 3.05 (Pb-Free / Halide Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Note on usage: Since the EFC3J018NUZ is a MOSFET product, please avoid using this device in the vicinity of highly charged objects. Please contact sales for use except the designated application.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

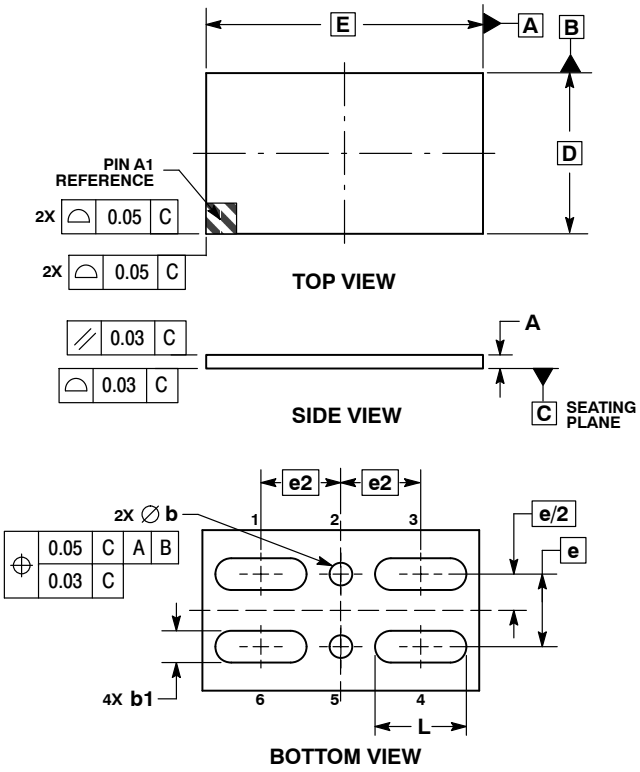
ON Semiconductor®



SCALE 4:1

WLCSP6, 1.77x3.05
CASE 567KS
ISSUE O

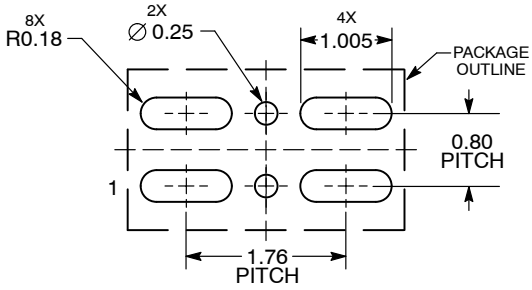
DATE 29 OCT 2014



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.145
b	0.22	0.28
b1	0.32	0.38
D	1.77 BSC	
E	3.05 BSC	
e	0.80 BSC	
e2	0.8775 BSC	
L	0.975	1.035

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**WLCSP6, 1.77X3.05**		**PAGE 1 OF 1**

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