SN74ALS29841, SN74ALS29842
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D3078, JUNE 1988

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
- **Buffered Control Inputs to Reduce DC Loading**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 10-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

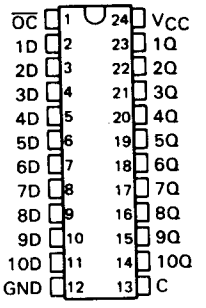
The ten latches are transparent D-type. The 'ALS29841 has noninverting data (D) inputs. The 'ALS29842 has inverting $\overline{D}$ inputs.

A buffered output control ($\overline{OC}$) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

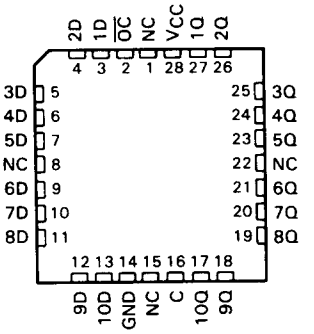
The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN74ALS29841 and SN74ALS29842 are characterized for operation from 0°C to 70°C.

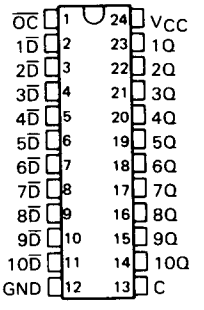
SN74ALS29841 . . . DW OR NT PACKAGE
(TOP VIEW)



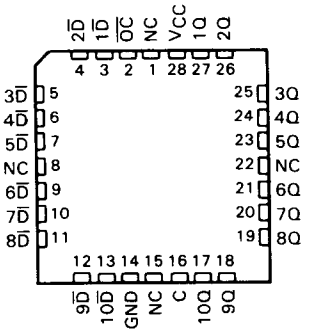
SN74ALS29841 . . . FN PACKAGE
(TOP VIEW)



SN74ALS29842 . . . DW OR NT PACKAGE
(TOP VIEW)



SN74ALS29842 . . . FN PACKAGE
(TOP VIEW)



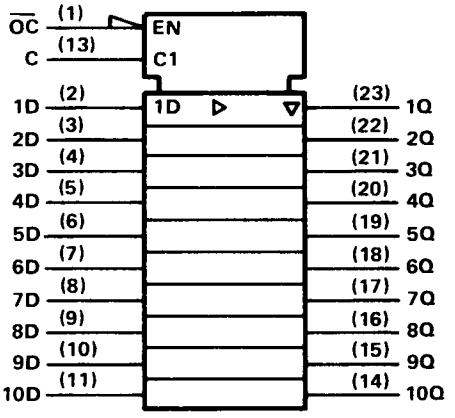
NC—No internal connection

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'ALS29841 logic symbol†



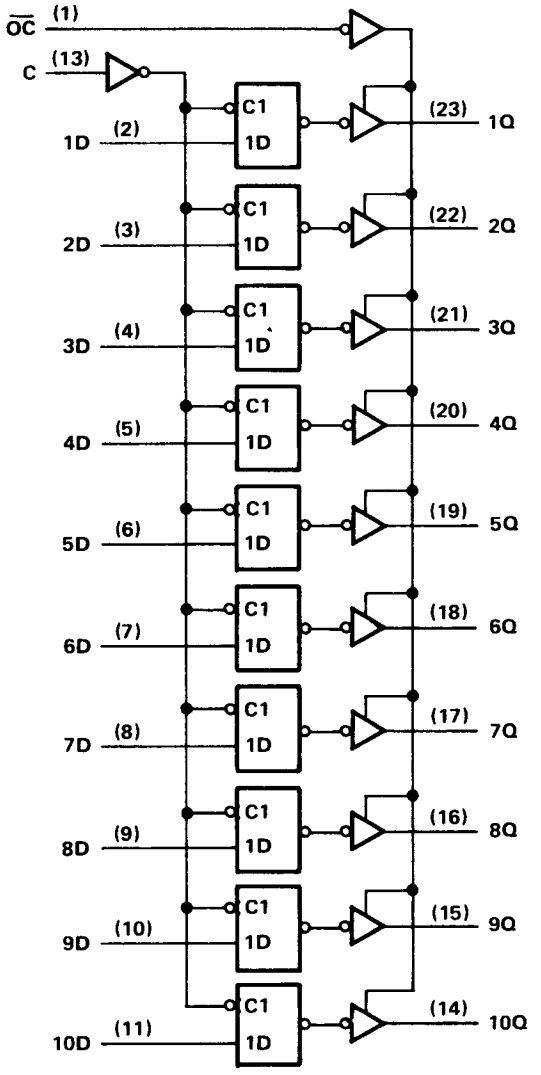
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

'ALS29841

INPUTS			OUTPUT
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

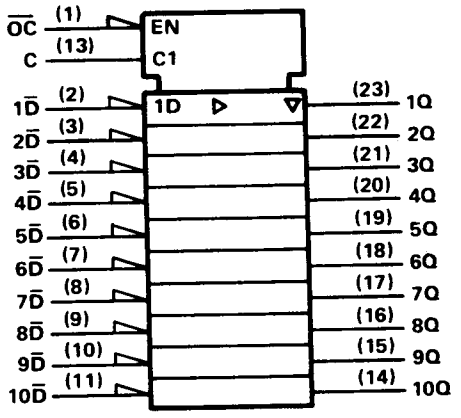
'ALS29841 logic diagram (positive logic)



Pin numbers shown are for DW and NT packages.

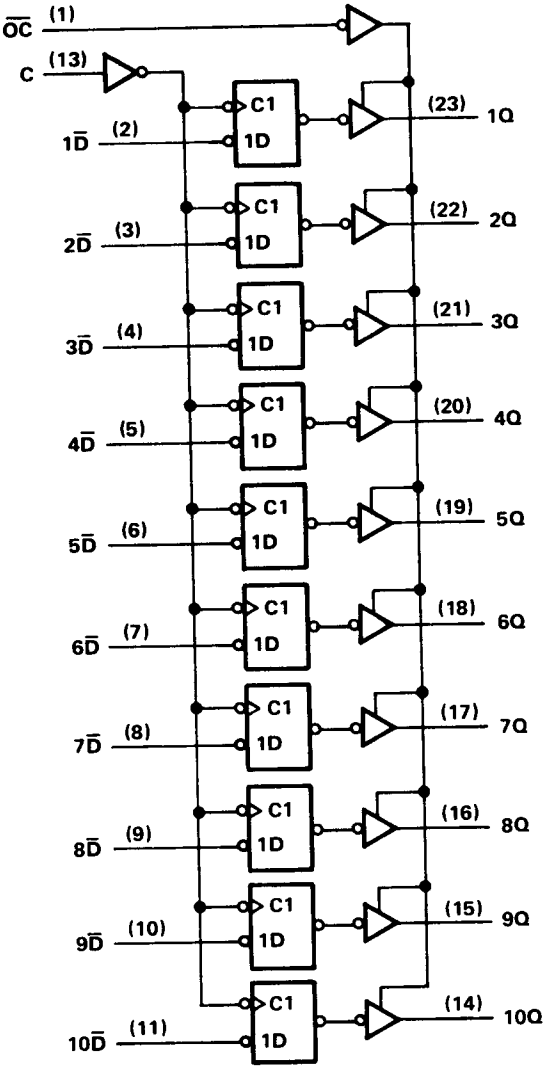
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'ALS29842 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'ALS29842 logic diagram (positive logic)



FUNCTION TABLE

'ALS29842

INPUTS			OUTPUT
$\overline{OC}$	C	$\overline{D}$	Q
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

Pin numbers shown are for DW and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		5		4.75	5	5.25	V
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
I_{OH}	High-level output current						−24	mA
I_{OL}	Low-level output current						48	mA
t_w	Pulse duration, enable C high	4			6			ns
t_{su}	Setup time, data before enable C↓	2.5			2.5			ns
t_h	Hold time, data after enable C↓	4.5			4.5			ns
T_A	Operating free-air temperature		25		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −15 mA	2.4	3.3		V
	V_{CC} = 4.75 V,	I_{OH} = −24 mA	2	3.1		
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 48 mA		0.35	0.5	
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4			−20	μA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.4 V			−0.2	mA
I_{OS}‡	V_{CC} = 5.25 V,	V_O = 0	−75		−250	mA
I_{CC}	V_{CC} = 5.25 V,	Outputs low		55	85	mA

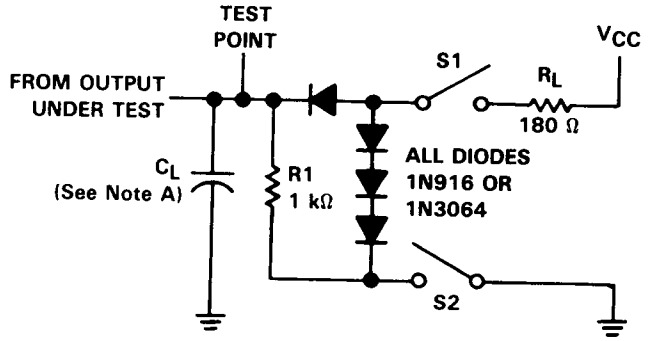
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 5 V, T_A = 25°C			V_{CC} = MIN TO MAX,† T_A = MIN TO MAX†		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Any Q	C_L = 50 pF	2	5.7	8	2	9.5	ns
t_{PHL}				2	6.2	8	2	9.5	
t_{PLH}			C_L = 300 pF		10	12.5		14	
t_{PHL}					10	14		14	
t_{PLH}	C	Any Q	C_L = 50 pF		8	10.5		12	ns
t_{PHL}					7.5	10		12	
t_{PLH}			C_L = 300 pF			15		16	
t_{PHL}						15		16	
t_{PZH}	$\overline{OC}$	Any Q	C_L = 50 pF		7.3	12		14	ns
t_{PZL}					9.7	12		14	
t_{PZH}			C_L = 300 pF			17		20	
t_{PZL}						21		23	
t_{PHZ}	$\overline{OC}$	Any Q	C_L = 50 pF		10.4	14		15	ns
t_{PLZ}					4.7	11		12	
t_{PHZ}			C_L = 5 pF		3.4	8		9	
t_{PLZ}					3.8	8		9	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

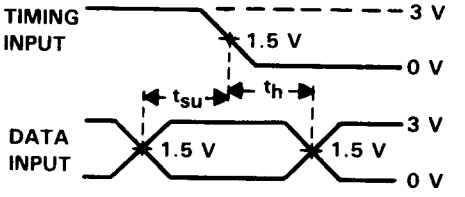
PARAMETER MEASUREMENT INFORMATION



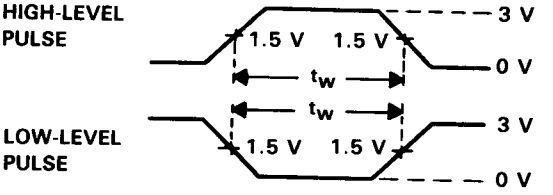
LOAD CIRCUIT

SWITCH POSITION TABLE

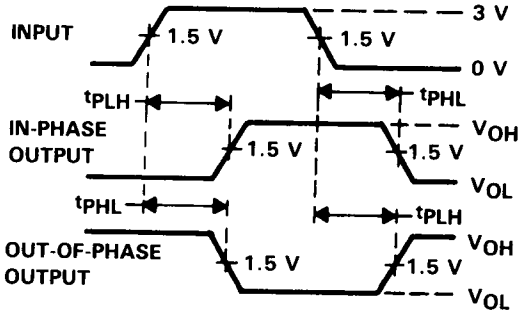
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



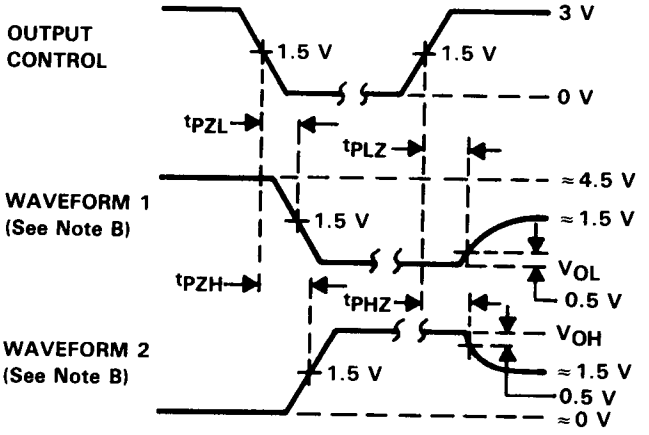
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1

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