FDMA410NZT-F130-VB Datasheet
N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ.)
20	0.010 at V_{GS}= 10 V	12	7.2 nC
	0.012 at V_{GS} = 4.5 V	10	

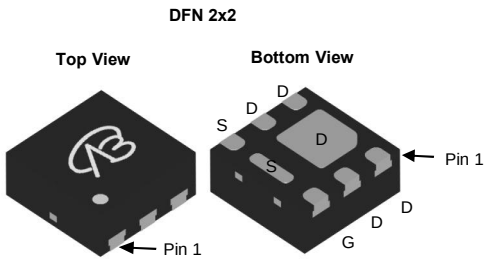
FEATURES

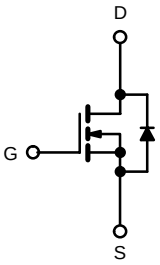
- **Halogen-free**
- Trench Power MOSFET
- Optimized for High-Side Synchronous Rectifier Operation
- 100 % R_g Tested
- 100 % UIS Tested

RoHS COMPLIANT

APPLICATIONS

- Notebook CPU Core
  - High-Side Switch





N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	12	A
	T_C = 70 °C		10	
	T_A = 25 °C		5.0[b, c]	
	T_A = 70 °C		3.0[b, c]	
Pulsed Drain Current		I_{DM}	48	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	3.7	
	T_A = 25 °C		2.0[b, c]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	20	
Avalanche Energy		E_{AS}	21	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	4.1	W
	T_C = 70 °C		2.5	
	T_A = 25 °C		2.2[b, c]	
	T_A = 70 °C		1.3[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, d]	t ≤ 10 s	R_{thJA}	39	55	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	25	29	

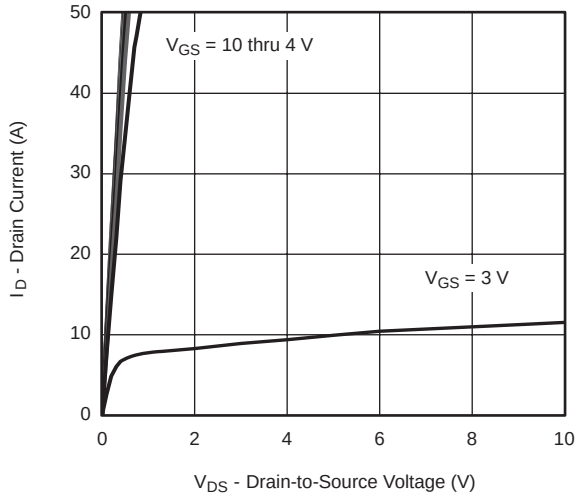
Notes:
a. Base on T_C = 25 °C.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. Maximum under Steady State conditions is 85 °C/W.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		26		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.5		1.5	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V			1	µA
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A		0.010		Ω
		V_{GS} = 4.5 V, I_D = 9 A		0.012		
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 10 A		50		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 16 V, V_{GS} = 0 V, f = 1 MHz		1080		pF
Output Capacitance	C_{oss}			40		
Reverse Transfer Capacitance	C_{rss}			35		
Total Gate Charge	Q_g	V_{DS} = 16 V, V_{GS} = 10 V, I_D = 6 A		15	23	nC
		V_{DS} = 16 V, V_{GS} = 5 V, I_D = 6 A		6.8	10.2	
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			2.3		
Gate Resistance	R_g	f = 1 MHz	0.36	1.8	3.6	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 16 V, R_L = 1.4 Ω $I_D \cong$ 6 A, V_{GEN} = 4.5 V, R_g = 1 Ω		16	23	ns
Rise Time	t_r			12	16	
Turn-Off Delay Time	$t_{d(off)}$			16	22	
Fall Time	t_f			10	18	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 16 V, R_L = 1.4 Ω $I_D \cong$ 6 A, V_{GEN} = 10 V, R_g = 1 Ω		8	16	
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			16	22	
Fall Time	t_f			8	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			12	A
Pulse Diode Forward Current[a]	I_{SM}				48	
Body Diode Voltage	V_{SD}	I_S = 6 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 6 A, dI/dt = 100 A/µs, T_J = 25 °C		15	30	ns
Body Diode Reverse Recovery Charge	Q_{rr}			6	12	nC
Reverse Recovery Fall Time	t_a			8		ns
Reverse Recovery Rise Time	t_b			7		

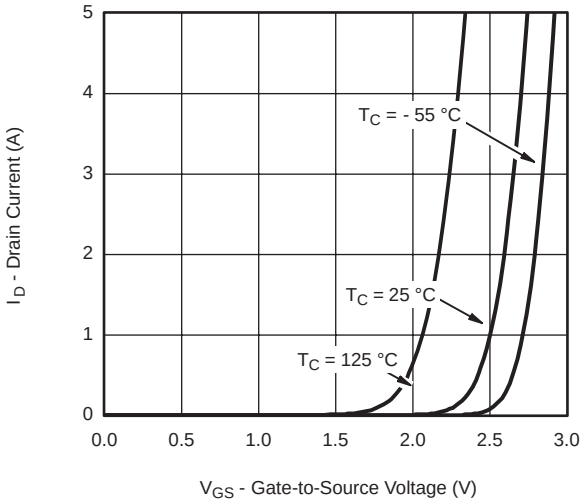
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

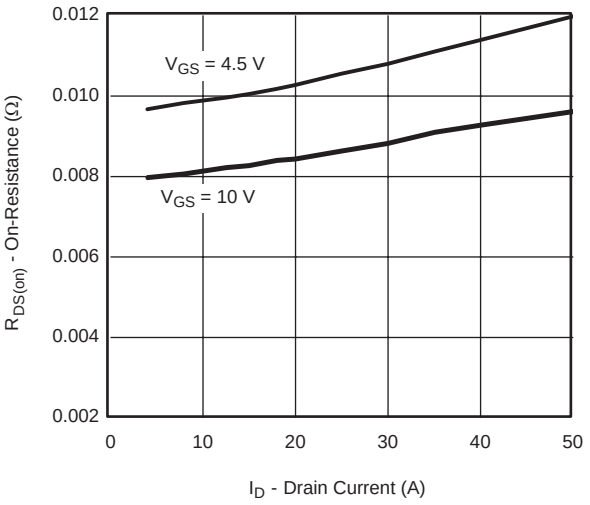
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



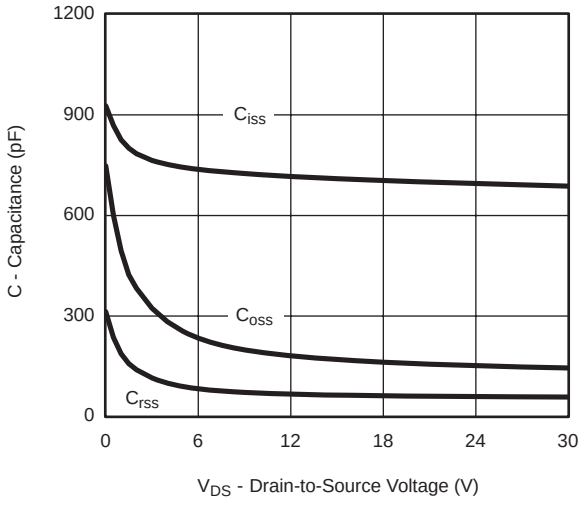
Output Characteristics



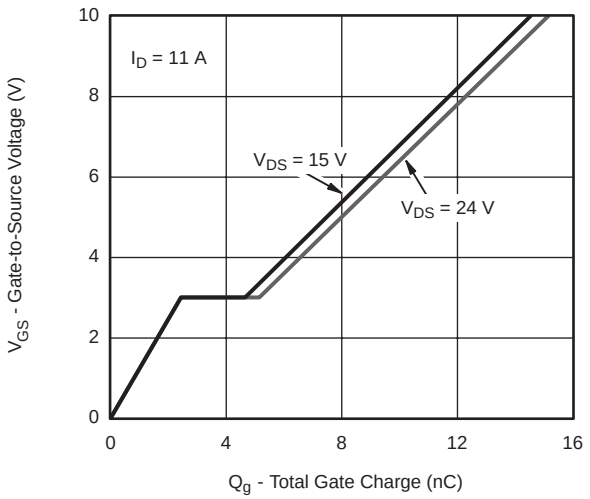
Transfer Characteristics



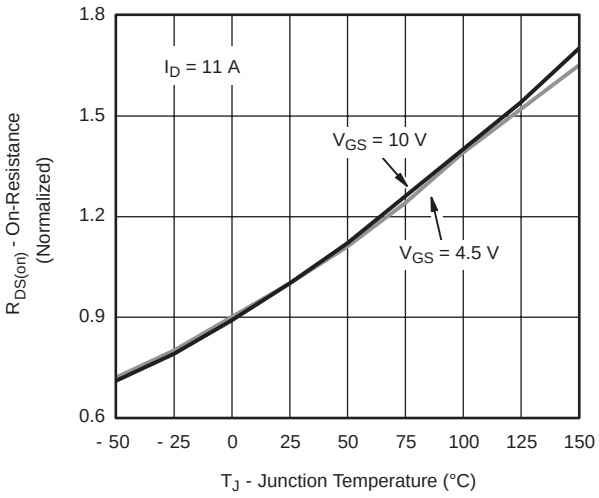
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

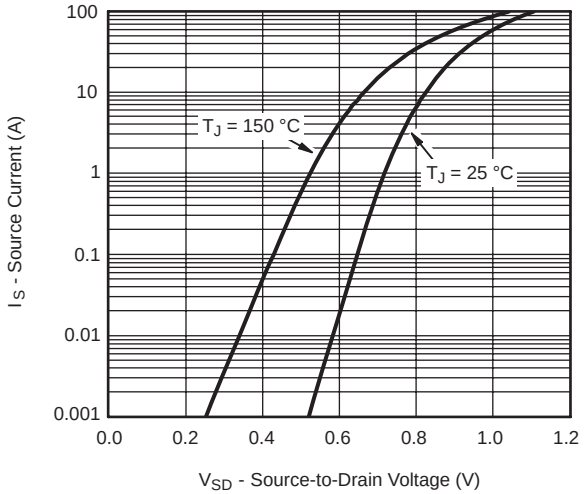


Gate Charge

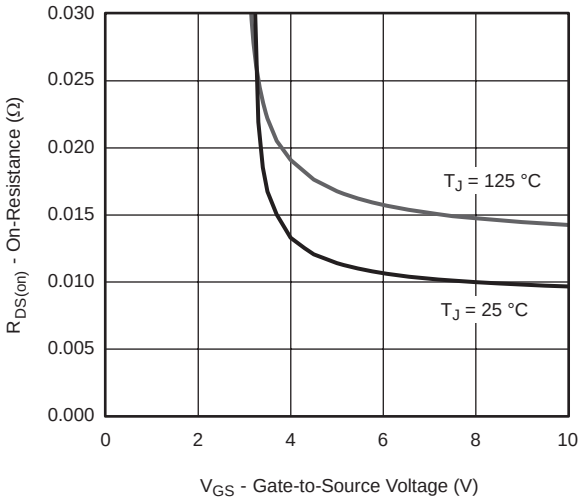


On-Resistance vs. Junction Temperature

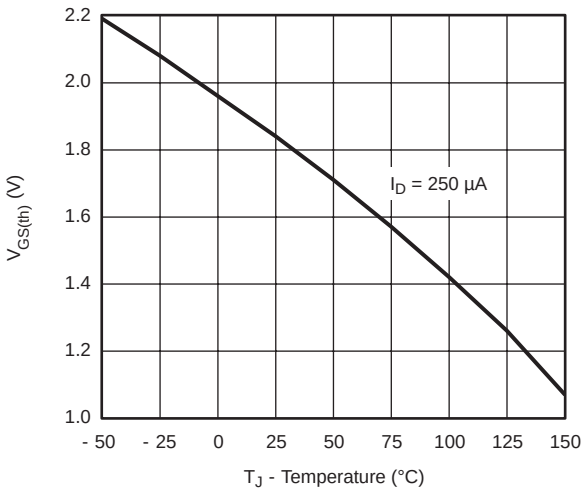
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



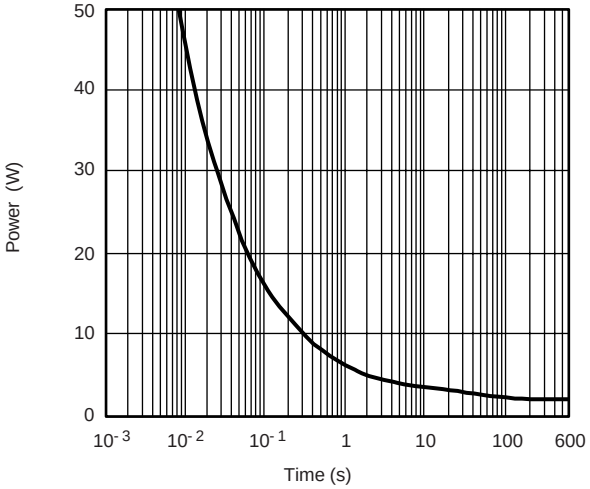
Source-Drain Diode Forward Voltage



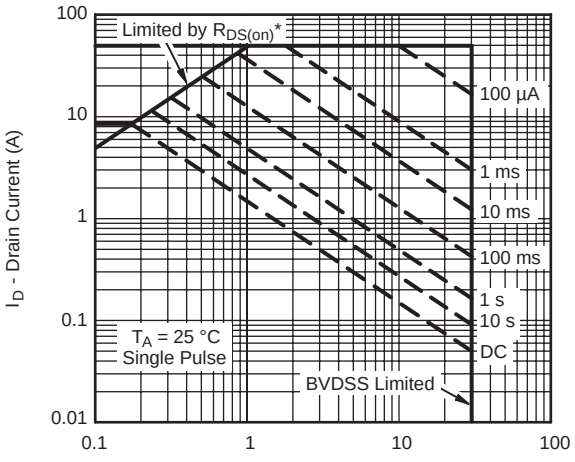
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



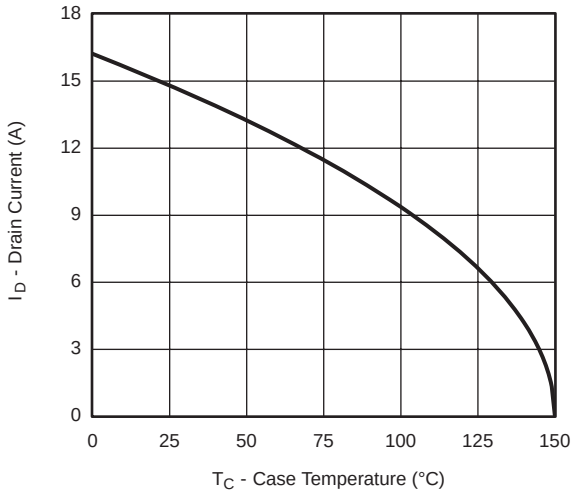
Single Pulse Power, Junction-to-Ambient



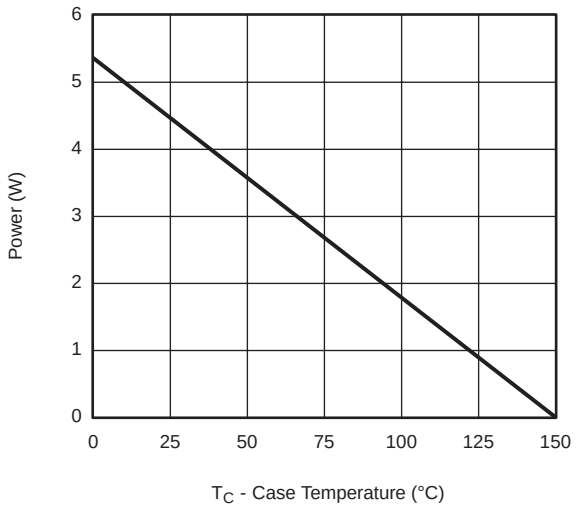
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

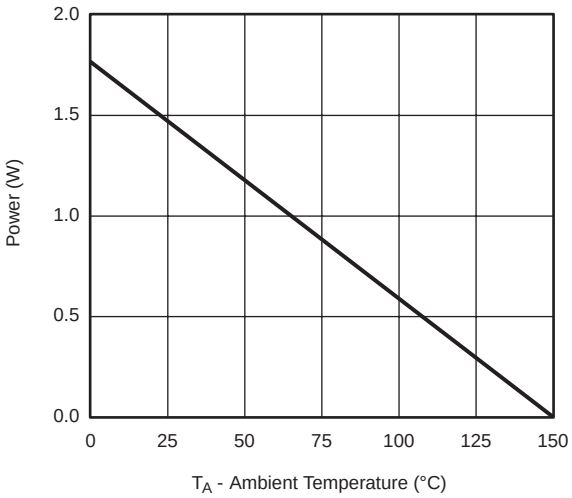
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



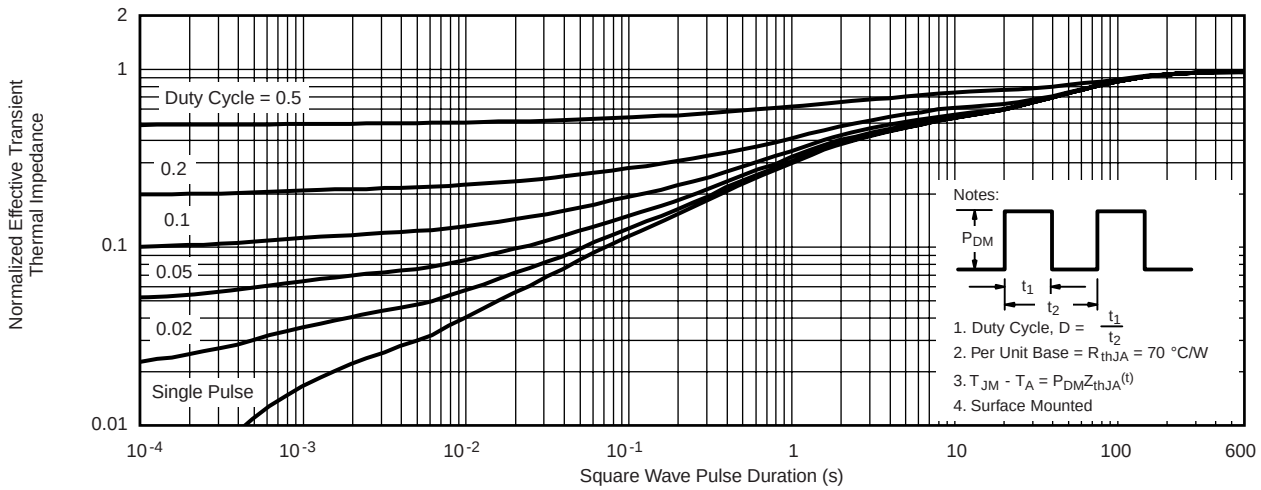
Power Derating, Junction-to-Foot



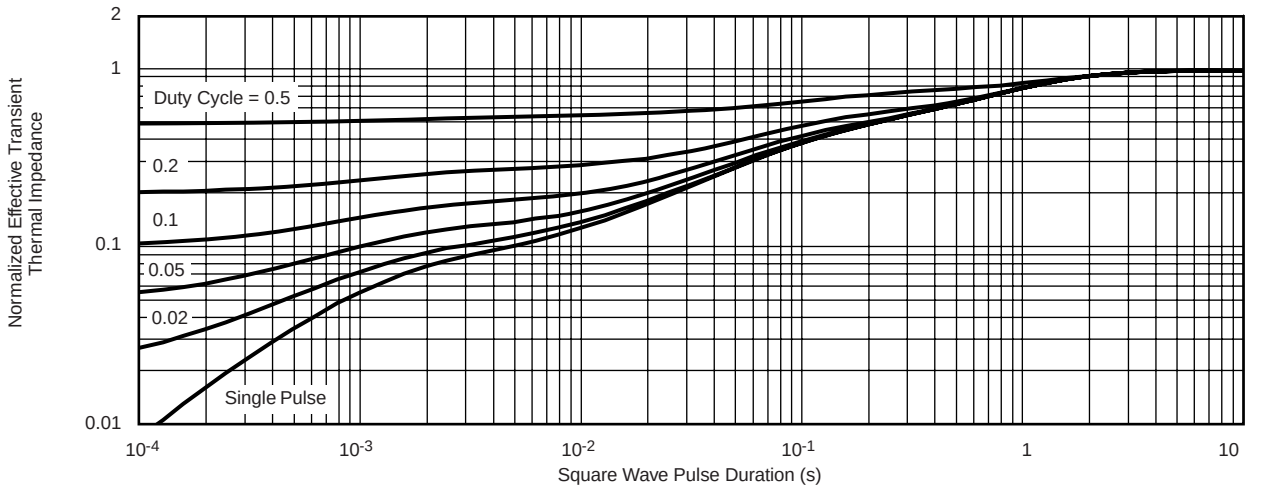
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

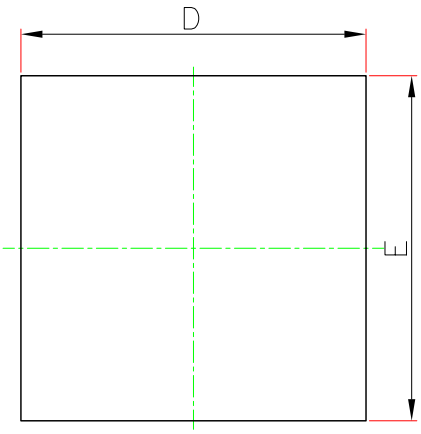


Normalized Thermal Transient Impedance, Junction-to-Ambient

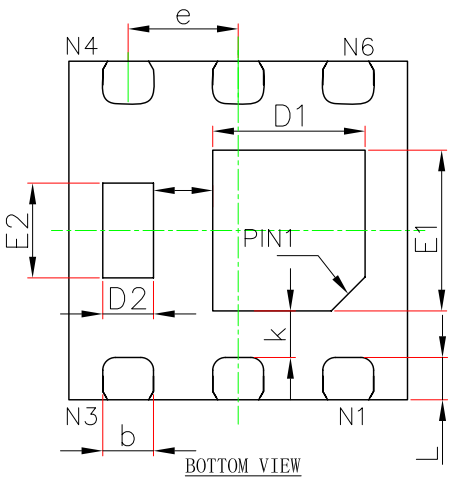


Normalized Thermal Transient Impedance, Junction-to-Foot

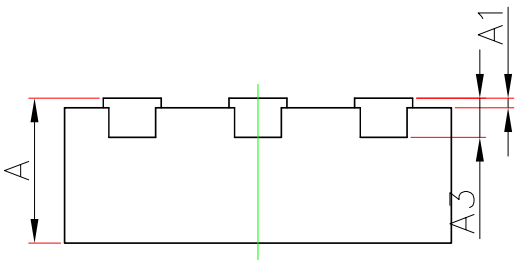
DFN2×2 Package Outline Dimensions



TOP VIEW
[顶视图]



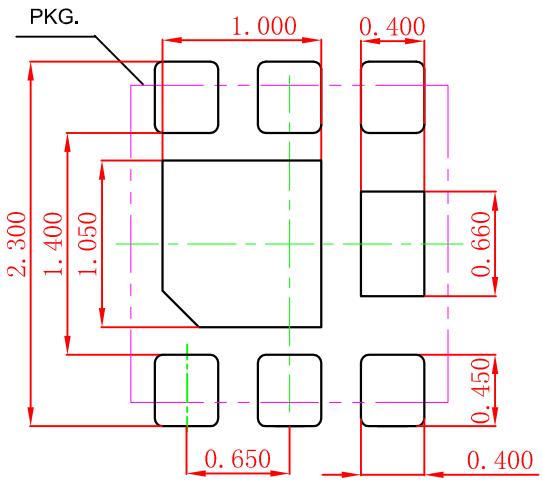
BOTTOM VIEW
[背视图]



SIDE VIEW
[侧视图]

Symbols	Dimensions in Milimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.152REF.		0.006REF.	
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D1	0.800	1.000	0.031	0.039
E1	0.850	1.050	0.033	0.041
D2	0.200	0.400	0.008	0.016
E2	0.460	0.660	0.018	0.026
b	0.250	0.350	0.010	0.014
e	0.650BSC.		0.026BSC.	
k	0.275REF.		0.011REF.	
k1	0.350REF.		0.014REF.	
L	0.200	0.300	0.007	0.012

DFN2×2 Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.050mm.
3.The pad layout is for reference purposes only.

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