# SN74LV541A Octal Buffers/Drivers With 3-State Outputs

## 1 Features

- Operation of 2-V to 5.5-V $V_{CC}$
- Max $t_{pd}$ of 6 ns at 5 V
- Typical $V_{OLP}$ (output ground bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Typical $V_{OHV}$ (output $V_{OH}$ undershoot) > 2.3 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Support mixed-mode voltage operation on all ports
- $I_{off}$ supports partial-power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 17

## 2 Applications

- Smart grids
- TVs
- Set-top-boxes
- Audio
- Servers
- Surveillance cameras
- Network switches
- Infotainment

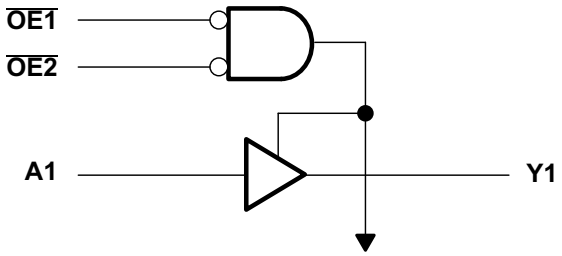
## 3 Description

The SN74LV541A device is an octal buffer/driver designed for 2-V to 5.5-V $V_{CC}$ operation.

**Package Information**

| PART NUMBER | PACKAGE[1] | PACKAGE SIZE[2] |
|---|---|---|
| SN74LV244A | DB (SSOP, 20) | 7.2 mm × 7.8 mm |
| | DW (SOIC, 20) | 12.80 mm × 10.3 mm |
| | NS (SO, 20) | 12.60 mm × 5.30 mm |
| | PW (TSSOP, 20) | 6.50 mm × 7.8 mm |
| | RGY (VQFN, 20) | 4.5 mm × 3.50 mm |
| | RKS (VQFN, 20) | 4.50 mm × 2.50 mm |
| | DGS (VSSOP, 20) | 5.10 mm × 4.9 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Simplified Schematic**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

# Table of Contents

**1 Features**....1
**2 Applications**....1
**3 Description**....1
**4 Revision History**....2
**5 Pin Configuration and Functions**....3
**6 Specifications**....4
6.1 Absolute Maximum Ratings....4
6.2 ESD Ratings....4
6.3 Recommended Operating Conditions....5
6.4 Thermal Information....5
6.5 Electrical Characteristics....6
6.6 Switching Characteristics, $V_{CC}$ = 2.5 V ± 0.2 V....6
6.7 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V....6
6.8 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V....7
6.9 Noise Characteristics....7
6.10 Operating Characteristics....7
6.11 Typical Characteristics....8
**7 Parameter Measurement Information**....10
**8 Detailed Description**....11
8.1 Overview....11
8.2 Functional Block Diagram....11
8.3 Feature Description....11
8.4 Device Functional Modes....12
**9 Application and Implementation**....13
9.1 Application Information....13
9.2 Typical Application....13
9.3 Power Supply Recommendations....15
9.4 Layout....15
**10 Device and Documentation Support**....17
10.1 Documentation Support....17
10.2 Receiving Notification of Documentation Updates....17
10.3 Support Resources....17
10.4 Trademarks....17
10.5 Glossary....17
10.6 Electrostatic Discharge Caution....17
10.7 Glossary....17
**11 Mechanical, Packaging, and Orderable Information**....17

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision M (March 2023) to Revision N (August 2023) | Page |
|---|---|
| • Deleted *DGV* from *Package Information* table and ESD rating from *Features* section | 1 |
| • Updated thermal values for PW package from RθJA = 102.8 to 128.2, RθJC(top) = 36.8 to 70.5, RθJB = 53.8 to 79.3, ΨJT = 2.5 to 23.4, ΨJB = 53.3 to 78.9, all values in °C/W | 5 |

| Changes from Revision L (January 2023) to Revision M (March 2023) | Page |
|---|---|
| • Updated thermal values for DB package from RθJA = 96.0 to 118.2, RθJC(top) = 56.7 to 77.2, RθJB = 51.2 to 73, ΨJT = 19.4 to 42.2, ΨJB = 50.8 to 72.6, all values in °C/W | 5 |
| • Updated thermal values for NS package from RθJA = 77.1 to 108.1, RθJC(top) = 43.6 to 73.9, RθJB = 44.6 to 73.1, ΨJT = 17.2 to 44.1, ΨJB = 44.2 to 72.8, all values in °C/W | 5 |


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## 5 Pin Configuration and Functions

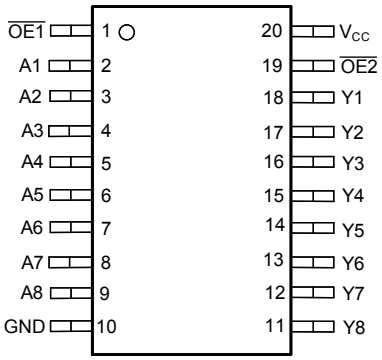



**Figure 5-1. DB, DGV, DW, NS, PW or DGS Package, 20-Pin SSOP, TVSOP, SOIC, SO, TSSOP or VSSOP (Top View)**

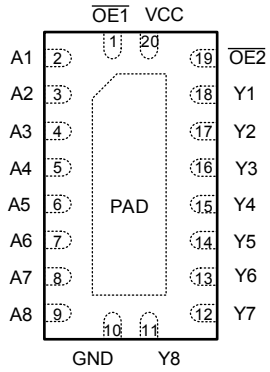



**Figure 5-2. RGY and RKS Package, 20-Pin VQFN with (Exposed Thermal Pad Top View)**

**Table 5-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $\overline{OE1}$ | 1 | I | Output enable input 1, active low |
| A1 | 2 | I | Input for channel 1 |
| A2 | 3 | I | Input for channel 2 |
| A3 | 4 | I | Input for channel 3 |
| A4 | 5 | I | Input for channel 4 |
| A5 | 6 | I | Input for channel 5 |
| A6 | 7 | I | Input for channel 6 |
| A7 | 8 | I | Input for channel 7 |
| A8 | 9 | I | Input for channel 8 |
| GND | 10 | G | Ground |
| Y8 | 11 | O | Output for channel 8 |
| Y7 | 12 | O | Output for channel 7 |
| Y6 | 13 | O | Output for channel 6 |
| Y5 | 14 | O | Output for channel 5 |
| Y4 | 15 | O | Output for channel 4 |
| Y3 | 16 | O | Output for channel 3 |
| Y2 | 17 | O | Output for channel 2 |
| Y1 | 18 | O | Output for channel 1 |
| $\overline{OE2}$ | 19 | I | Output enable input 2, active low |
| $V_{CC}$ | 20 | P | Postive supply |
| Thermal Pad[2] | | — | The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply. |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.
(2) RKS package only

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 7 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 7 | V |
| $V_O$ | Output voltage range applied in the high or low state(2) (3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±35 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±70 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Section 6.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5-V maximum.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±3000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2) | ±2000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.


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## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | SN74LV541A | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC}$ × 0.7 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $V_{CC}$ × 0.3 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | High or low state | 0 | $V_{CC}$ | V |
| | | 3-state | 0 | 5.5 | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | μA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | –2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | –8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | –16 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | μA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | 8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 16 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 2.3 V to 2.7 V | | 200 | ns/V |
| | | $V_{CC}$ = 3 V to 3.6 V | | 100 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74LV541A | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | DB | DGV | DW | NS | PW | RGY | RKS | DGS | |
| | | 20 PINS | | | | | | | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 118.2 | 116.1 | 79.8 | 108.1 | 128.2 | 35.1 | 75.2 | 125.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 77.2 | 31.3 | 45.8 | 73.9 | 70.5 | 43.3 | 79.4 | 80.0 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 73 | 57.6 | 47.4 | 73.1 | 79.3 | 12.9 | 47.8 | 63.8 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 42.2 | 1.0 | 18.5 | 44.1 | 23.4 | 0.9 | 14.6 | 8.4 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 72.6 | 56.9 | 47.0 | 72.8 | 78.9 | 12.9 | 47.8 | 79.9 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | N/A | 7.9 | 31.5 | N/A | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

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## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 2 V to 5.5 V | $V_{CC}$ – 0.1 | | | $V_{CC}$ – 0.1 | | $V_{CC}$ – 0.1 | | V |
| | $I_{OH}$ = –2 mA | 2.3 V | 2 | | | 2 | | 2 | | |
| | $I_{OH}$= –8 mA | 3 V | 2.48 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –16 mA | 4.5 V | 3.8 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 2 V to 5.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 2 mA | 2.3 V | | | 0.4 | | 0.4 | | 0.4 | |
| | $I_{OL}$ = 8 mA | 3 V | | | 0.44 | | 0.44 | | 0.44 | |
| | $I_{OL}$ = 16 mA | 4.5 V | | | 0.55 | | 0.55 | | 0.55 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 to 5.5 V | | | ±1 | | ±1 | | ±1 | µA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±5 | | ±5 | | ±5 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 20 | | 20 | | 20 | µA |
| $I_{off}$ | $V_I$ or $V_O$ = 0 to 5.5 V | 0 | | | 5 | | 5 | | 5 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 2 | | | | | | pF |

## 6.6 Switching Characteristics, $V_{CC}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | $C_L$ = 15 pF | | 6.7 | 11.3 | 1 | 13.5 | 1 | 13.5 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 8.5 | 16.6 | 1 | 19.5 | 1 | 19.5 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 8.4 | 13.1 | 1 | 15 | 1 | 15 | |
| $t_{pd}$ | A | Y | $C_L$ = 50 pF | | 8.7 | 15.9 | 1 | 18.5 | 1 | 18.5 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 10.5 | 20.7 | 1 | 24 | 1 | 24 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 12.3 | 17.9 | 1 | 20 | 1 | 20 | |
| $t_{sk(o)}$ | | | | | | 2 | | 2 | | 2 | |

## 6.7 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | $C_L$ = 15 pF | | 4.8 | 7 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 6.1 | 10.5 | 1 | 12.5 | 1 | 12.5 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 5.8 | 11 | 1 | 12 | 1 | 12 | |
| $t_{pd}$ | A | Y | $C_L$ = 50 pF | | 6.1 | 10.5 | 1 | 12 | 1 | 12 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 7.4 | 14 | 1 | 16 | 1 | 16 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 8.8 | 15.4 | 1 | 17.5 | 1 | 17.5 | |
| $t_{sk(o)}$ | | | | | | 1.5 | | 1.5 | | 1.5 | |


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## 6.8 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | $C_L$ = 15 pF | | 3.5 | 5 | 1 | 6 | 1 | 6 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 4.3 | 7.2 | 1 | 8.5 | 1 | 8.5 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 3.9 | 7.5 | 1 | 8 | 1 | 8 | |
| $t_{pd}$ | A | Y | $C_L$ = 50 pF | | 4.3 | 7 | 1 | 8 | 1 | 8 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 5.3 | 9.2 | 1 | 10.5 | 1 | 10.5 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 5.6 | 8.8 | 1 | 10 | 1 | 10 | |
| $t_{sk(o)}$ | | | | | | 1 | | 1 | | 1 | |

## 6.9 Noise Characteristics

$V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C(1)

| PARAMETER | | SN74LV541A | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.5 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.4 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 2.9 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.99 | V |

(1) Characteristics are for surface-mount packages only.

## 6.10 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 50 pF, | f = 10 MHz | 3.3 V | 16.3 | pF |
| | | | | | 5 V | 17.8 | |

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## 6.11 Typical Characteristics

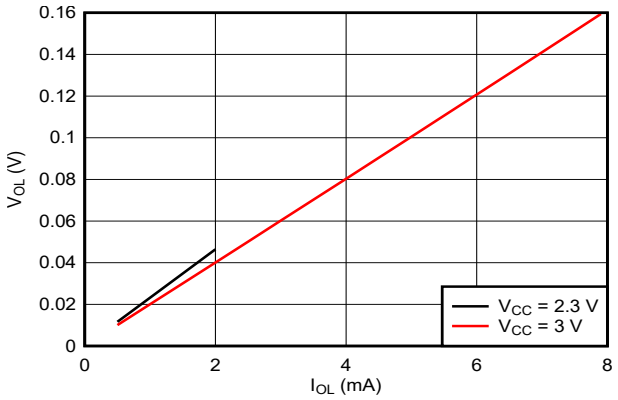



**Figure 6-1. Output Voltage in LOW State, 2.3- and 3-V Supply**

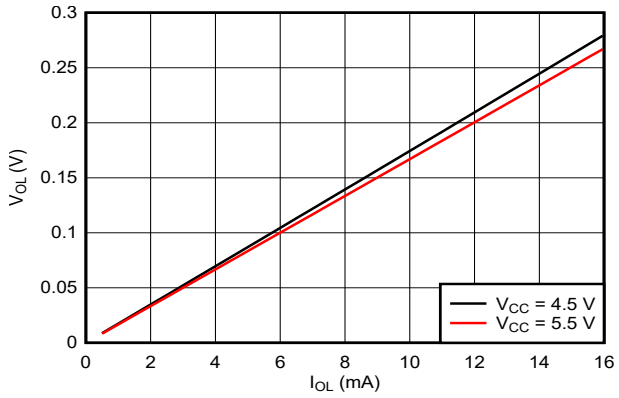



**Figure 6-2. Output Voltage in LOW State, 4.5- and 5.5-V Supply**

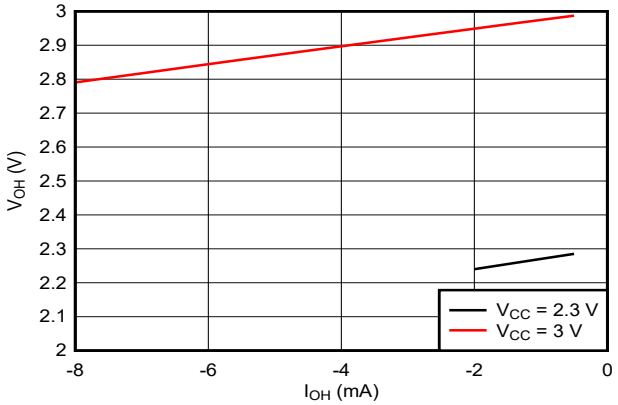



**Figure 6-3. Output Voltage in HIGH State, 2.3- and 3-V Supply**

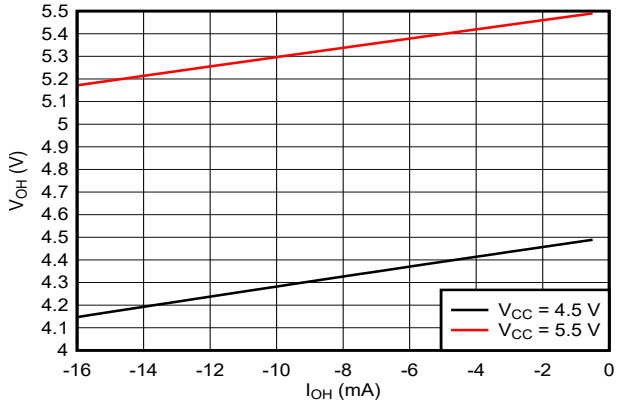



**Figure 6-4. Output Voltage in HIGH State, 4.5- and 5.5-V Supply**

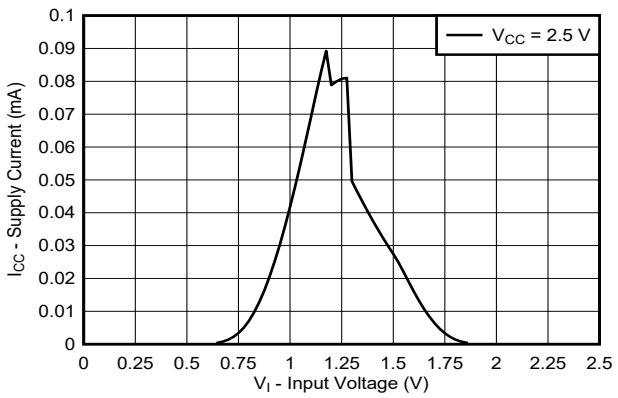



**Figure 6-5. Supply Current Across Input Voltage, 2.5-V Supply**

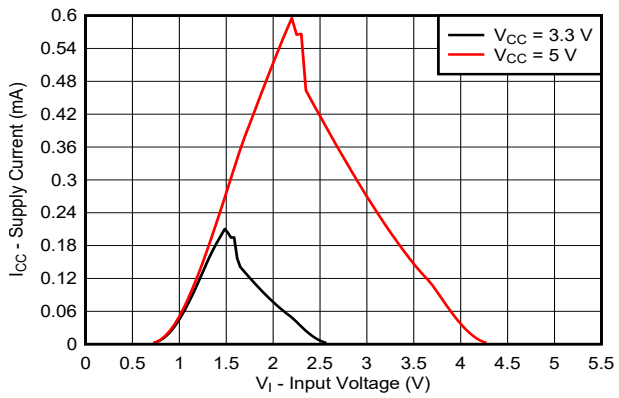



**Figure 6-6. Supply Current Across Input Voltage, 3.3- and 5-V Supply**


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## 6.11 Typical Characteristics (continued)

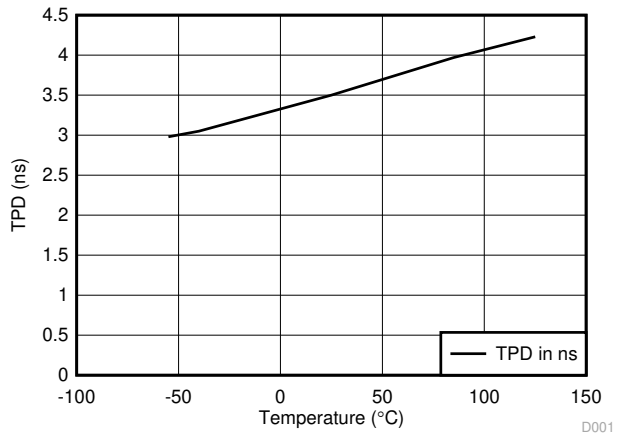



**Figure 6-7. TPD vs Temperature**

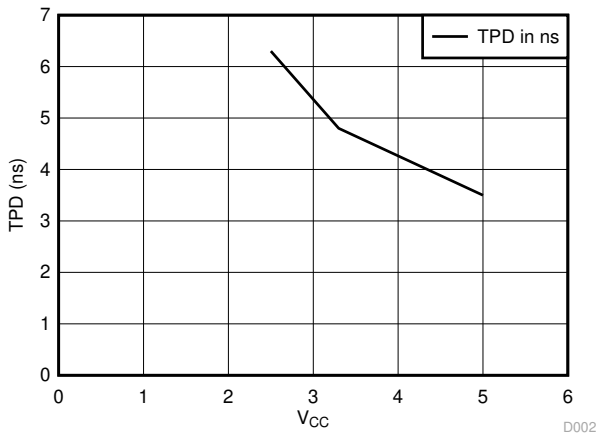
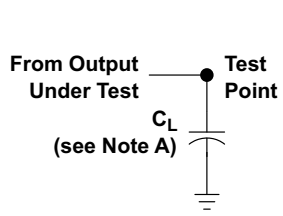


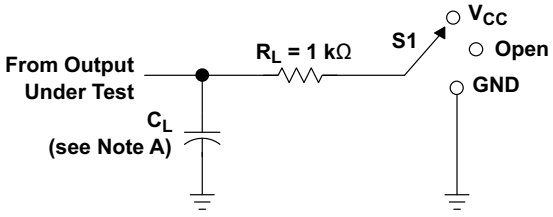

**Figure 6-8. TPD vs $V_{CC}$ at 25°C**

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## 7 Parameter Measurement Information

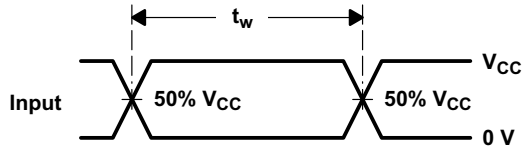



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

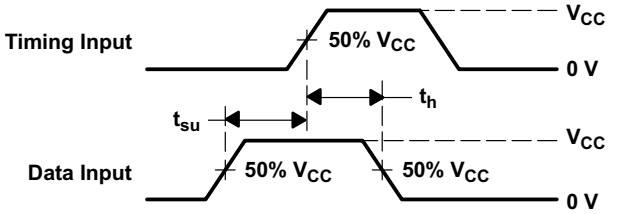



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |

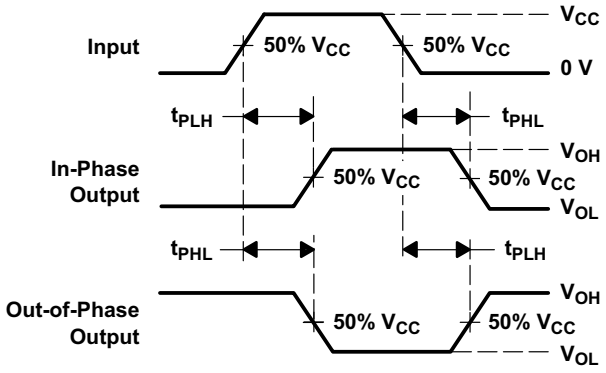
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



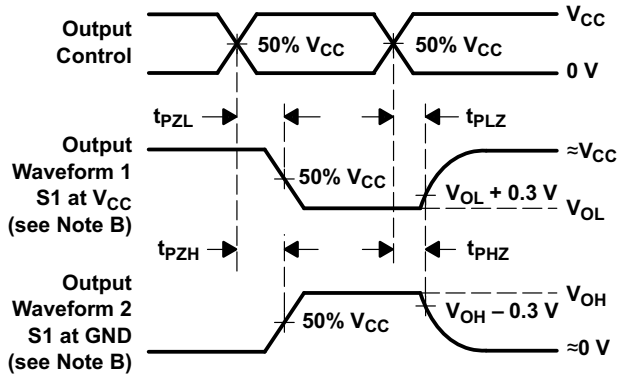

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 7-1. Load Circuit and Voltage Waveforms**


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# 8 Detailed Description

## 8.1 Overview

The SN74LV541A device is an octal buffers/driver designed for 2-V to 5.5-V $V_{CC}$ operation.

The SN74LV541A device is ideal for driving bus lines or buffer memory address registers. It features inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide non-inverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down, both $\overline{OE}$ should be tied to $V_{CC}$ through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LV541A device are fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

## 8.2 Functional Block Diagram

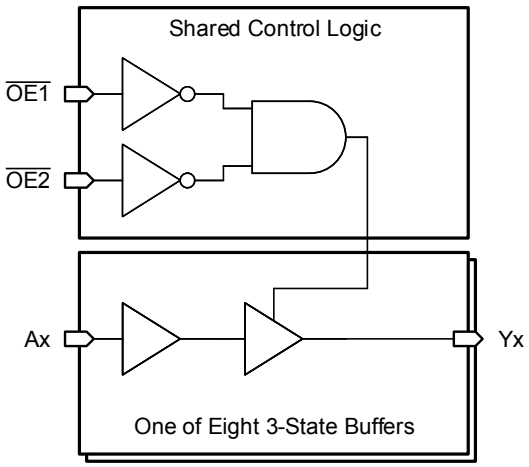



**Figure 8-1. Logic Diagram (Positive Logic)**

## 8.3 Feature Description

### 8.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

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### 8.3.2 Partial Power Down ($I_{off}$)

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the $I_{off}$ specification in the *Electrical Characteristics* table.

### 8.3.3 Clamp Diode Structure

Figure 8-2 shows the inputs and outputs to this device have negative clamping diodes only.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

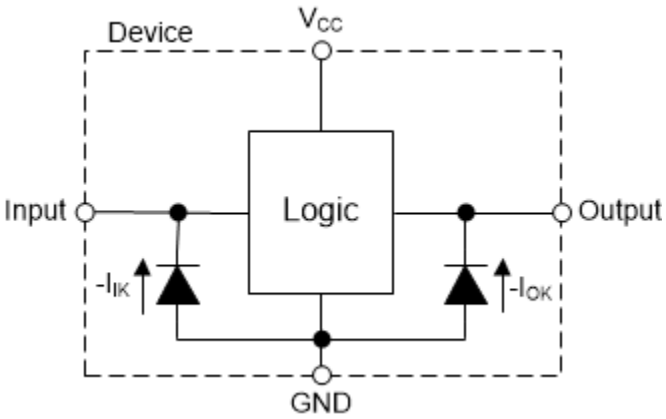



**Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output**

## 8.4 Device Functional Modes

**Table 8-1. Function Table (Each Buffer or Driver)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |


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# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74LV541A can be used to drive signals over relatively long traces or transmission lines. In order to reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver, a series damping resistor placed in series with the transmitter's output can be used. The figure in the Application Curve section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

## 9.2 Typical Application

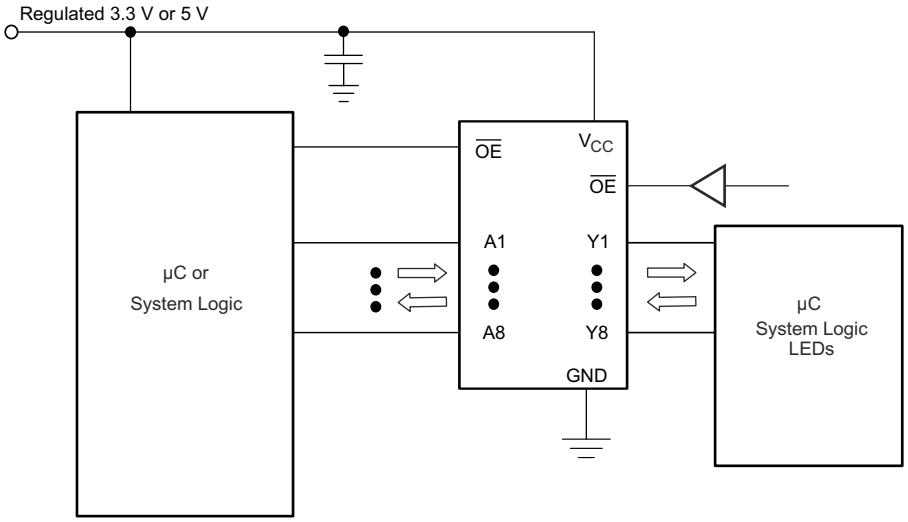



**Figure 9-1. Typical Application Schematic**

### 9.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV541A plus the maximum static supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through $V_{CC}$ listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV541A plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV541A can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

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The SN74LV541A can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OH}$ and $V_{OL}$. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

**CAUTION**

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 9.2.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV541A (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

The SN74LV541A has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

### 9.2.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### 9.2.4 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV541A to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than ($V_{CC} / I_{O(max)}$) Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.


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4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

### 9.2.5 Application Curves

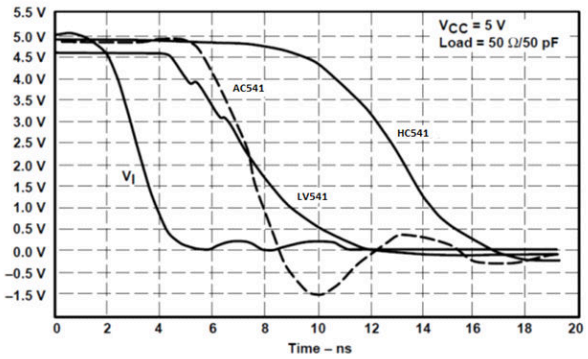



**Figure 9-2. Switching Characteristics Comparison**

## 9.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple $V_{CC}$ pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 9.4 Layout

### 9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 9-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

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### 9.4.2 Layout Example

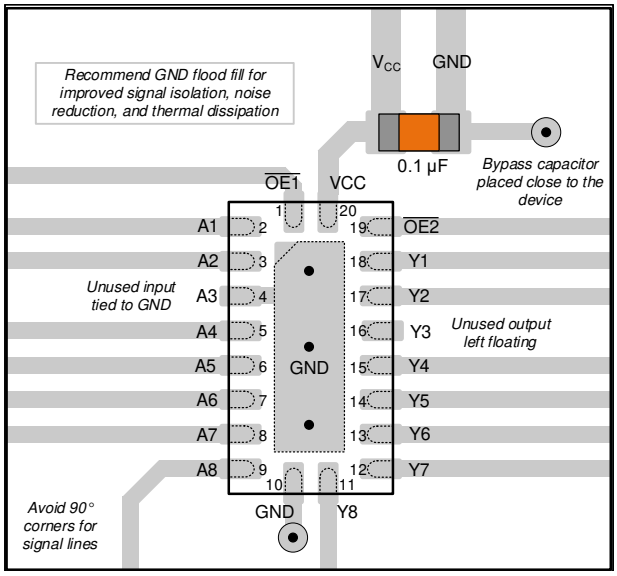



**Figure 9-3. Layout Example for the SN74LV541A in the RKS package**


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# 10 Device and Documentation Support

## 10.1 Documentation Support

### 10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation*
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application notes
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*

## 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 10.4 Trademarks

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## 10.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

## 10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV541ADBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV541A | Samples |
| SN74LV541ADBRE4 | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV541A | Samples |
| SN74LV541ADGSR | ACTIVE | VSSOP | DGS | 20 | 5000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | L541A | Samples |
| SN74LV541ADW | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | -40 to 125 | LV541A | |
| SN74LV541ADWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV541A | Samples |
| SN74LV541ANSR | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 74LV541A | Samples |
| SN74LV541APWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV541A | Samples |
| SN74LV541APWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV541A | Samples |
| SN74LV541ARGYR | ACTIVE | VQFN | RGY | 20 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LV541A | Samples |
| SN74LV541ARKSR | ACTIVE | VQFN | RKS | 20 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV541A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LV541A :**

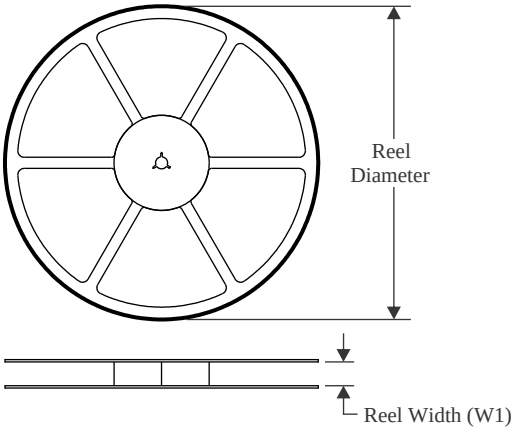
- Automotive : SN74LV541A-Q1

NOTE: Qualified Version Definitions:

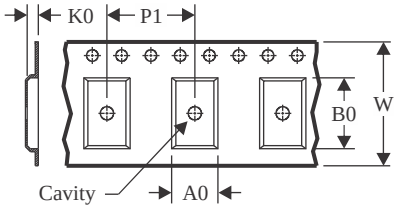
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

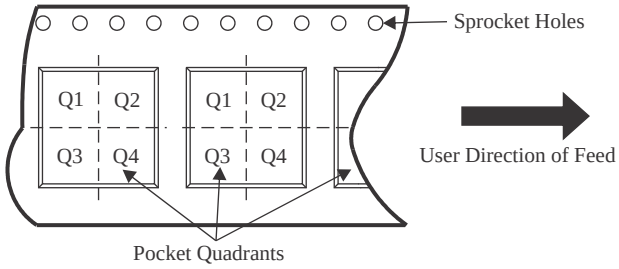



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

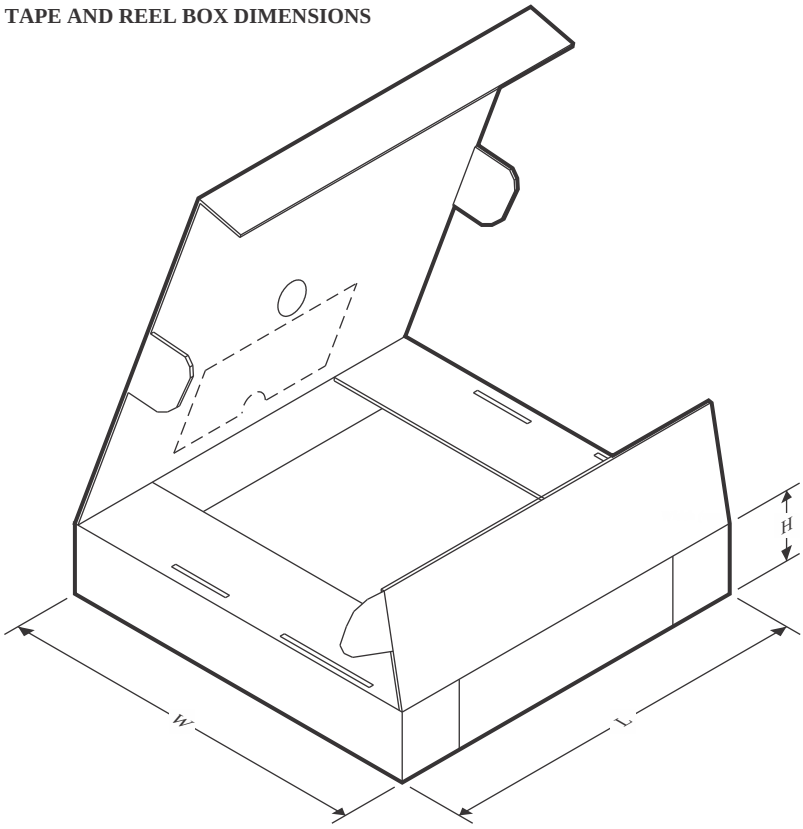
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV541ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV541ADGSR | VSSOP | DGS | 20 | 5000 | 330.0 | 16.4 | 5.4 | 5.4 | 1.45 | 8.0 | 16.0 | Q1 |
| SN74LV541ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LV541ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LV541ANSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LV541ANSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LV541APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74LV541APWRG4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74LV541APWRG4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74LV541ARGYR | VQFN | RGY | 20 | 3000 | 330.0 | 12.4 | 3.8 | 4.8 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV541ARKSR | VQFN | RKS | 20 | 3000 | 180.0 | 12.4 | 2.8 | 4.8 | 1.2 | 4.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

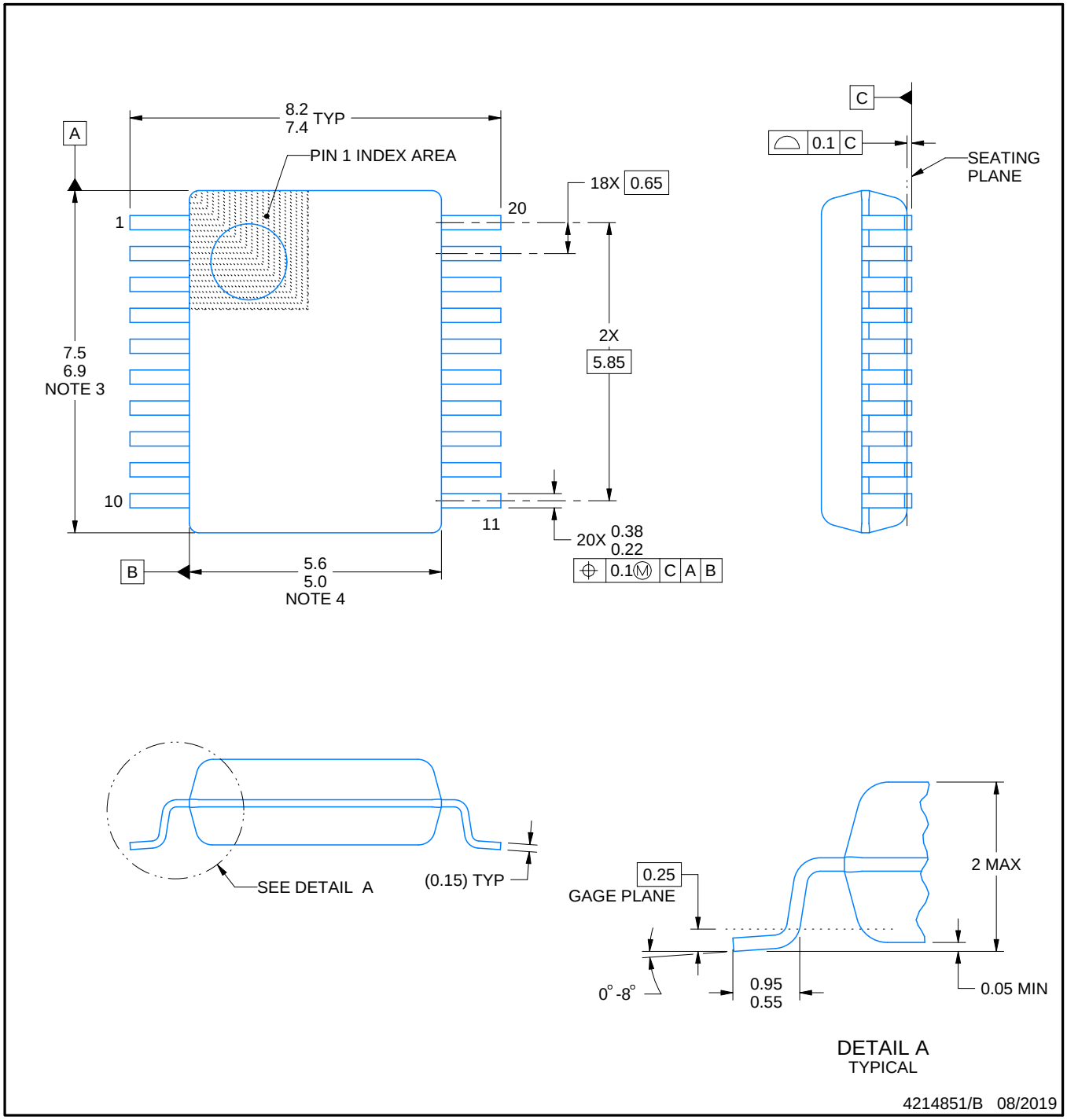
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV541ADBR | SSOP | DB | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV541ADGSR | VSSOP | DGS | 20 | 5000 | 356.0 | 356.0 | 35.0 |
| SN74LV541ADWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 41.0 |
| SN74LV541ADWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LV541ANSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LV541ANSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LV541APWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV541APWRG4 | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV541APWRG4 | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV541ARGYR | VQFN | RGY | 20 | 3000 | 356.0 | 356.0 | 35.0 |
| SN74LV541ARKSR | VQFN | RKS | 20 | 3000 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## DB0020A

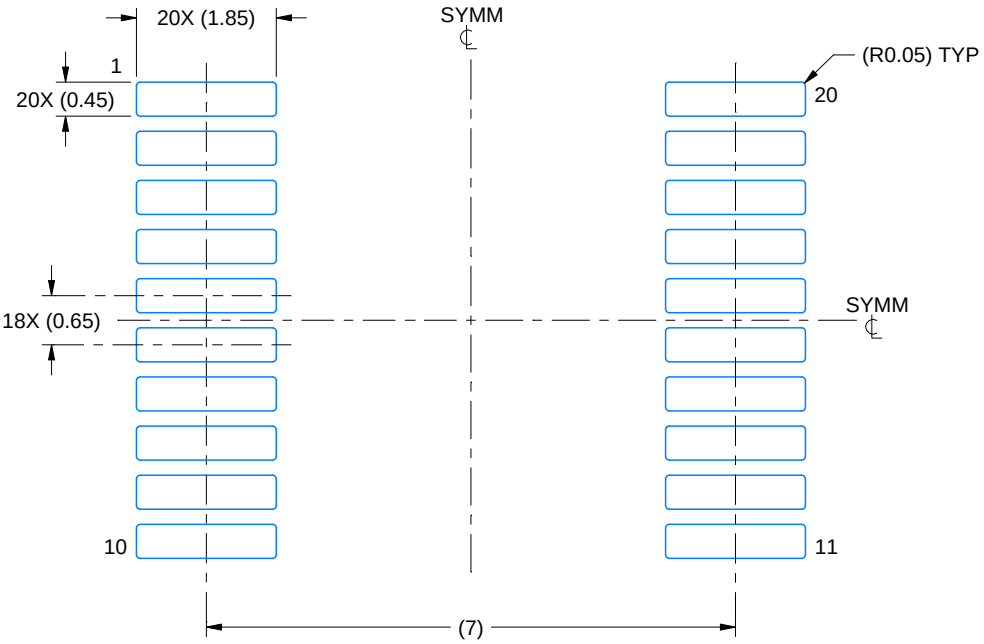
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

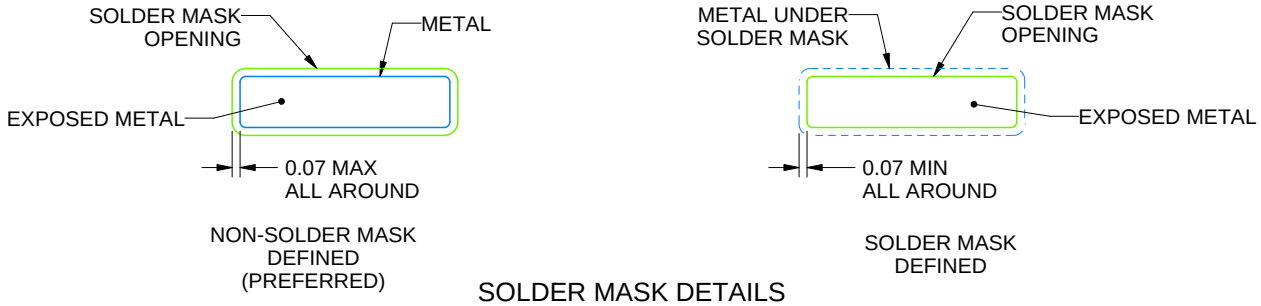



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

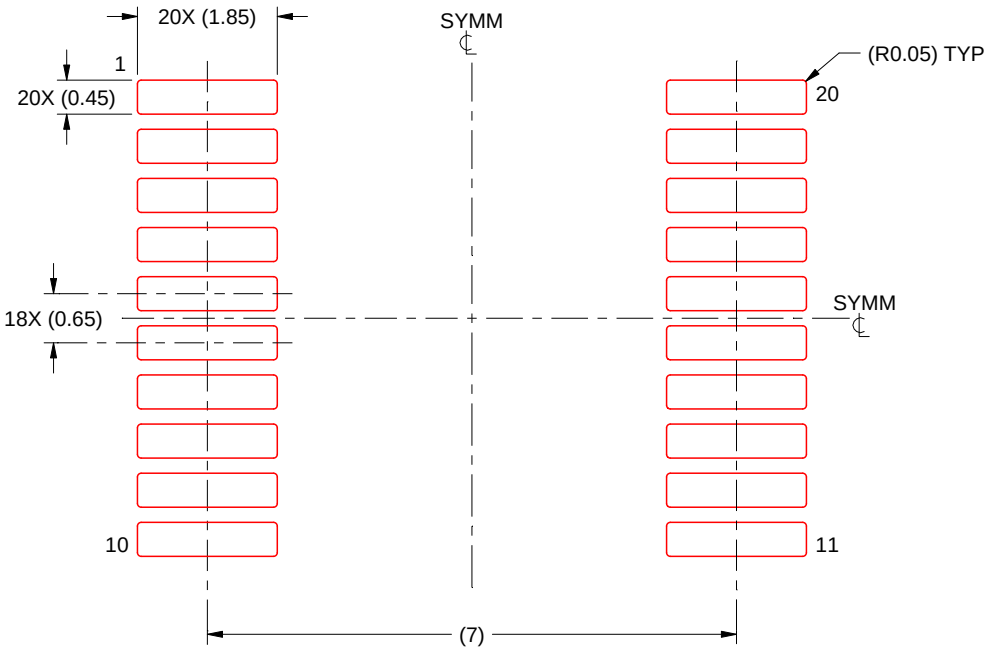
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DB0020A

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

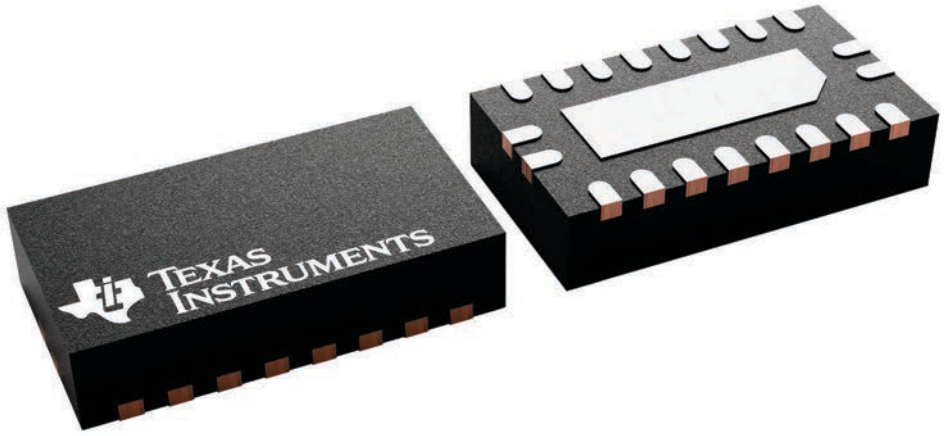
## RKS 20

## VQFN - 1 mm max height

**2.5 x 4.5, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

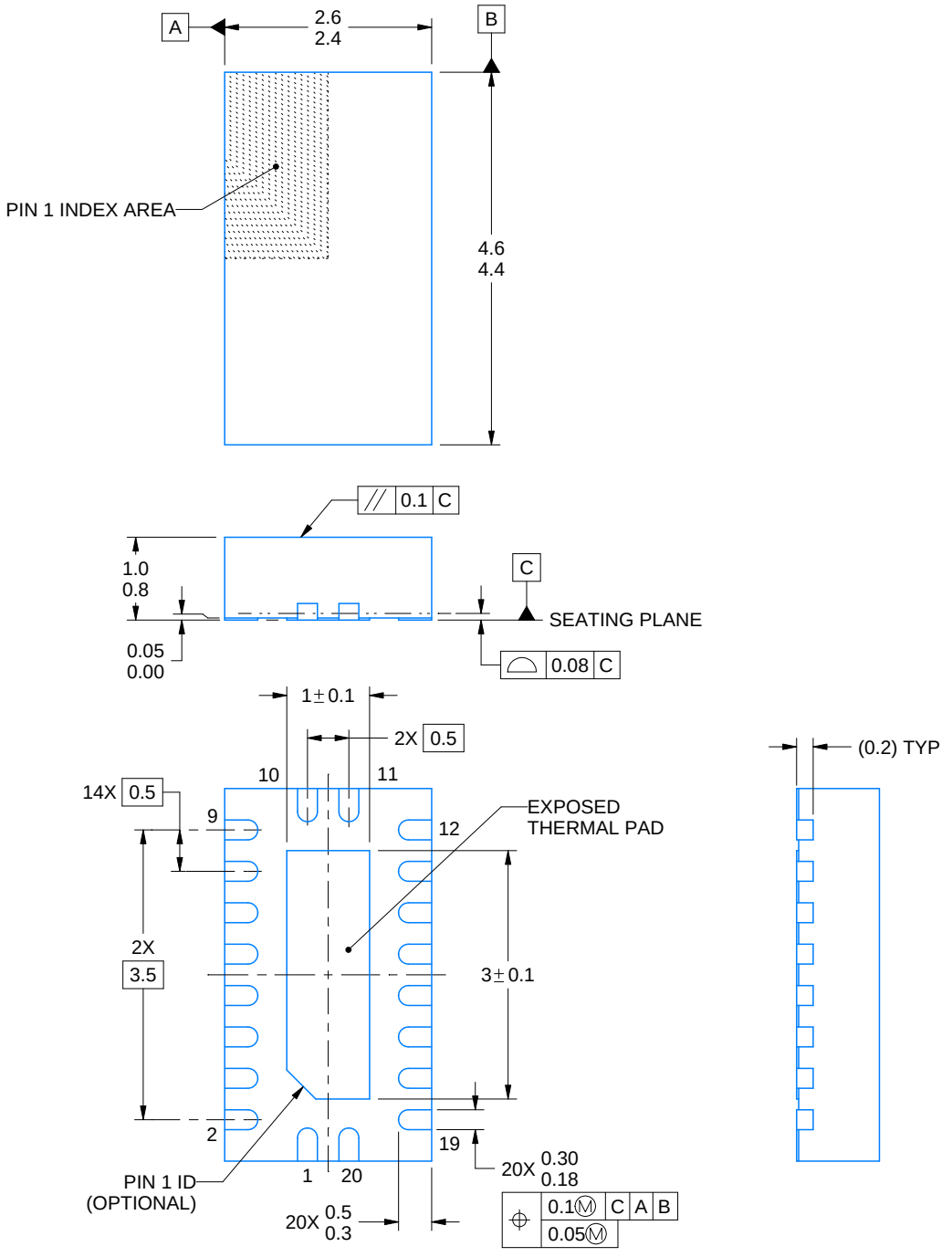


# PACKAGE OUTLINE

## RKS0020A

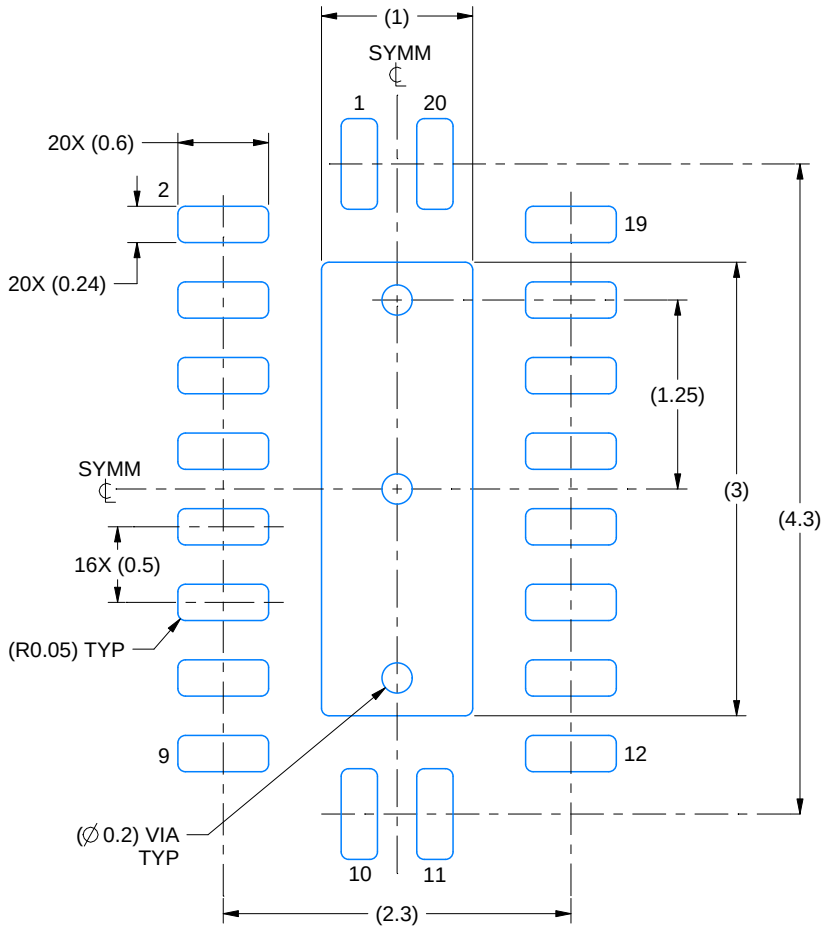
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

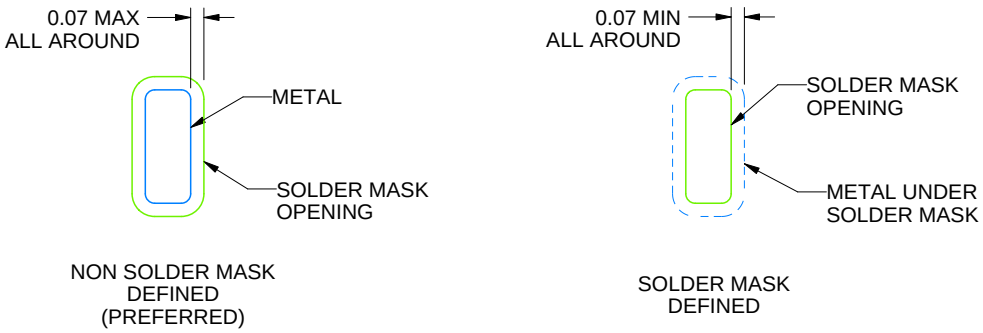



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:20X

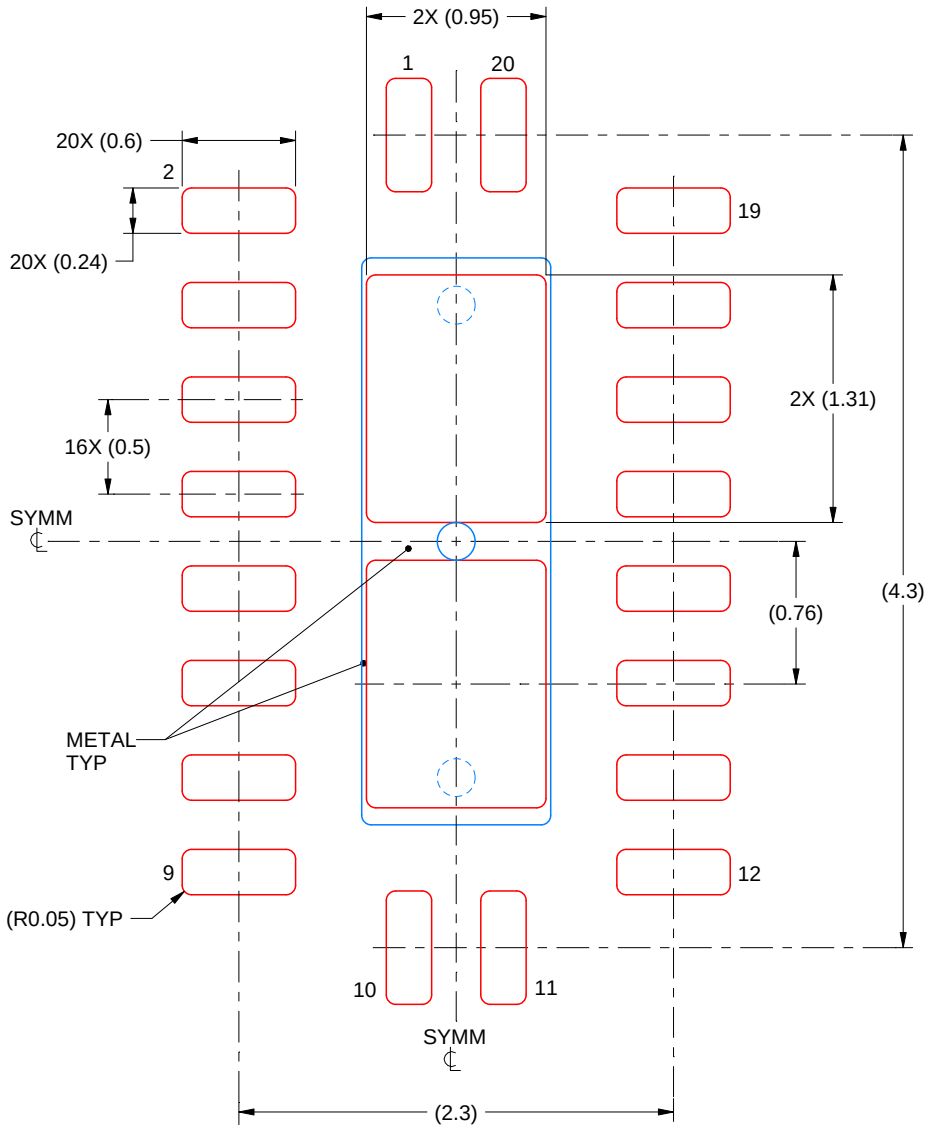



SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

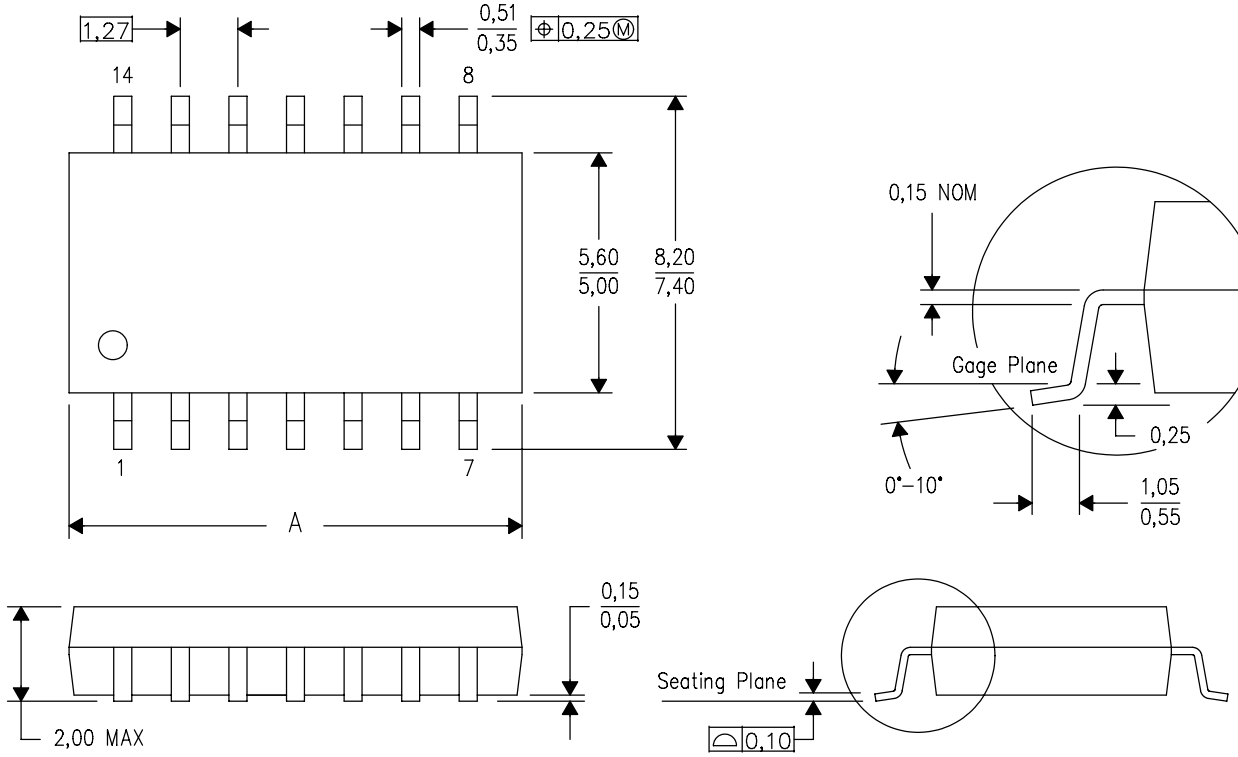
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

# GENERIC PACKAGE VIEW

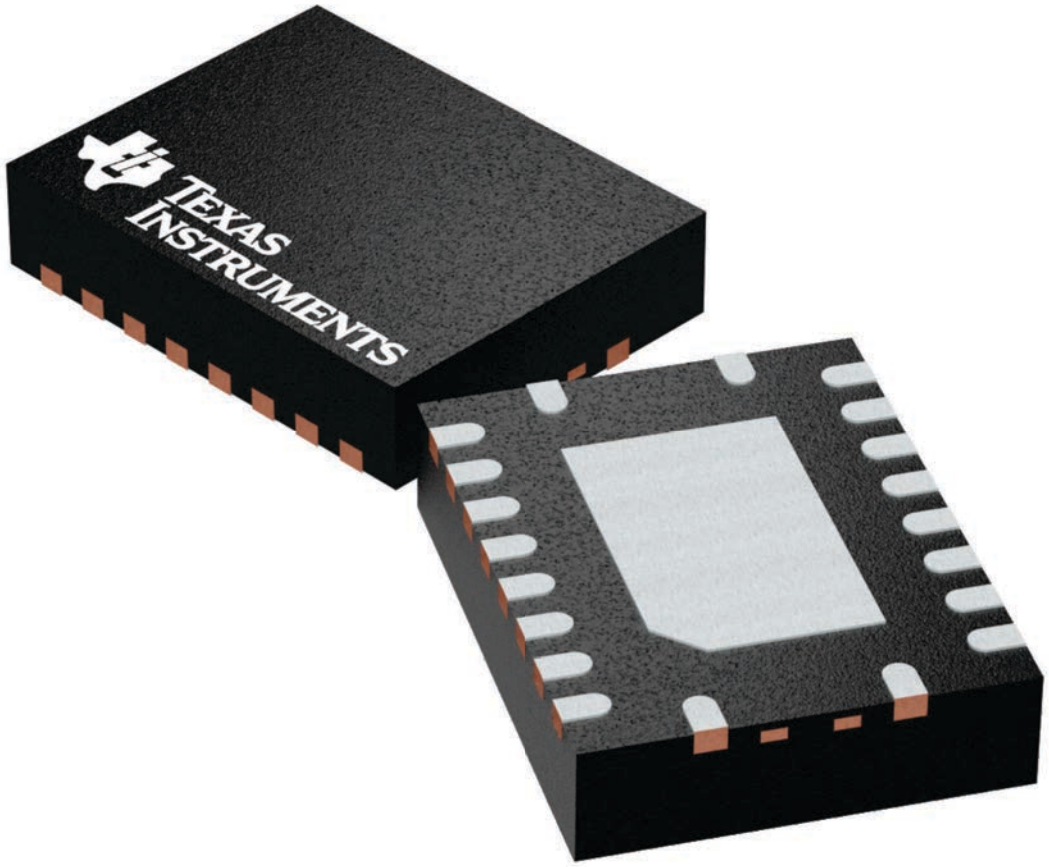
## RGY 20

## VQFN - 1 mm max height

**3.5 x 4.5, 0.5 mm pitch**

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



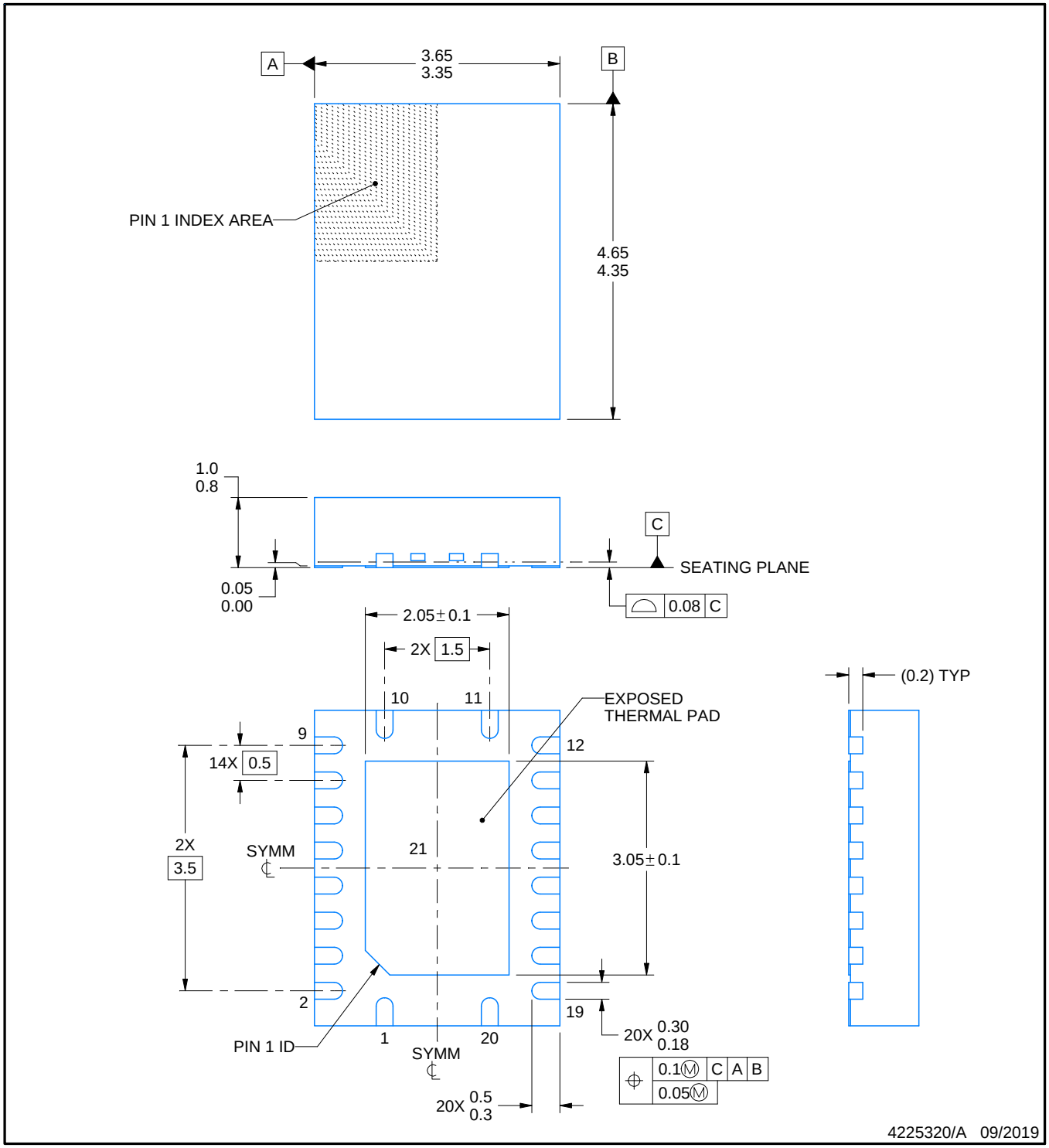

4225264/A

# PACKAGE OUTLINE

## RGY0020A

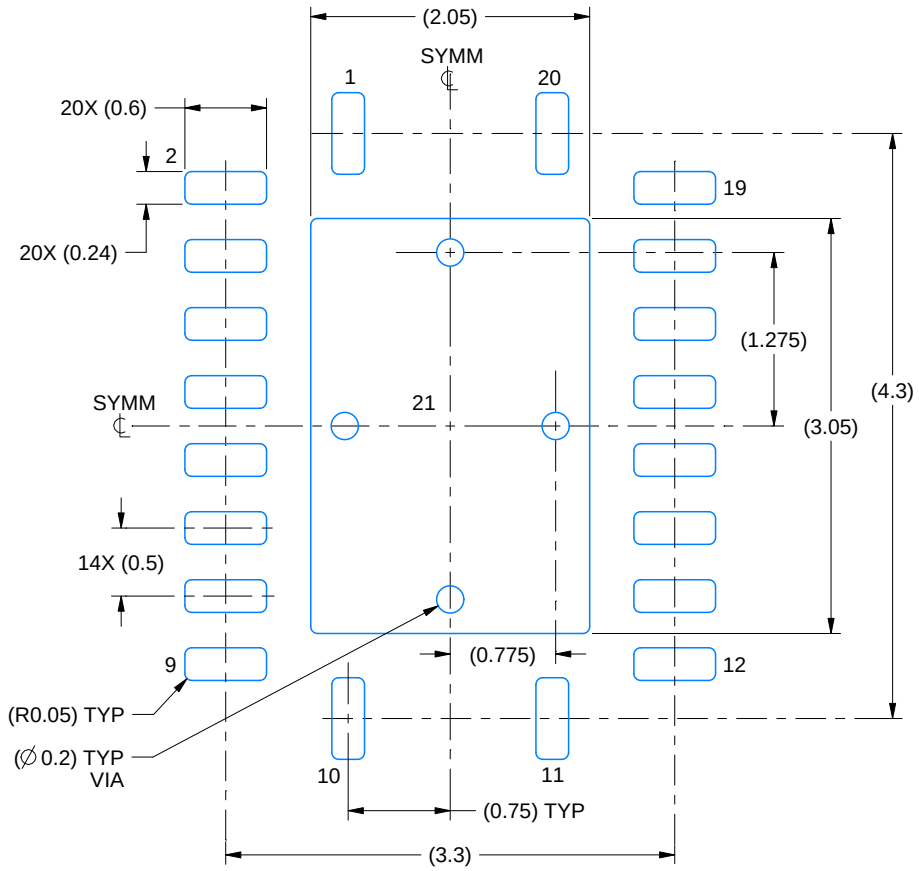
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

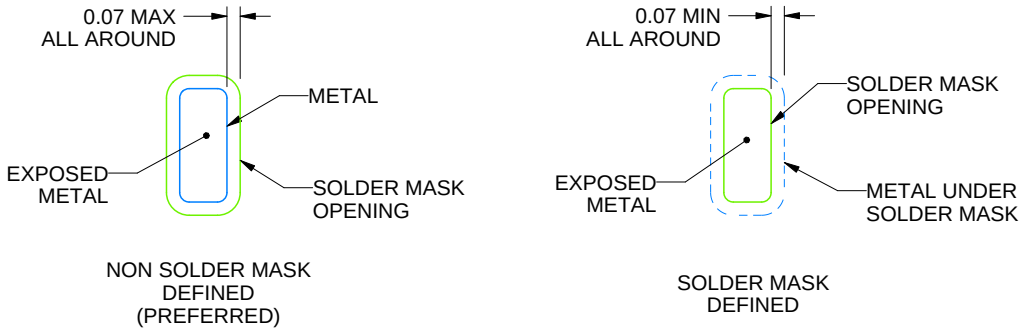



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

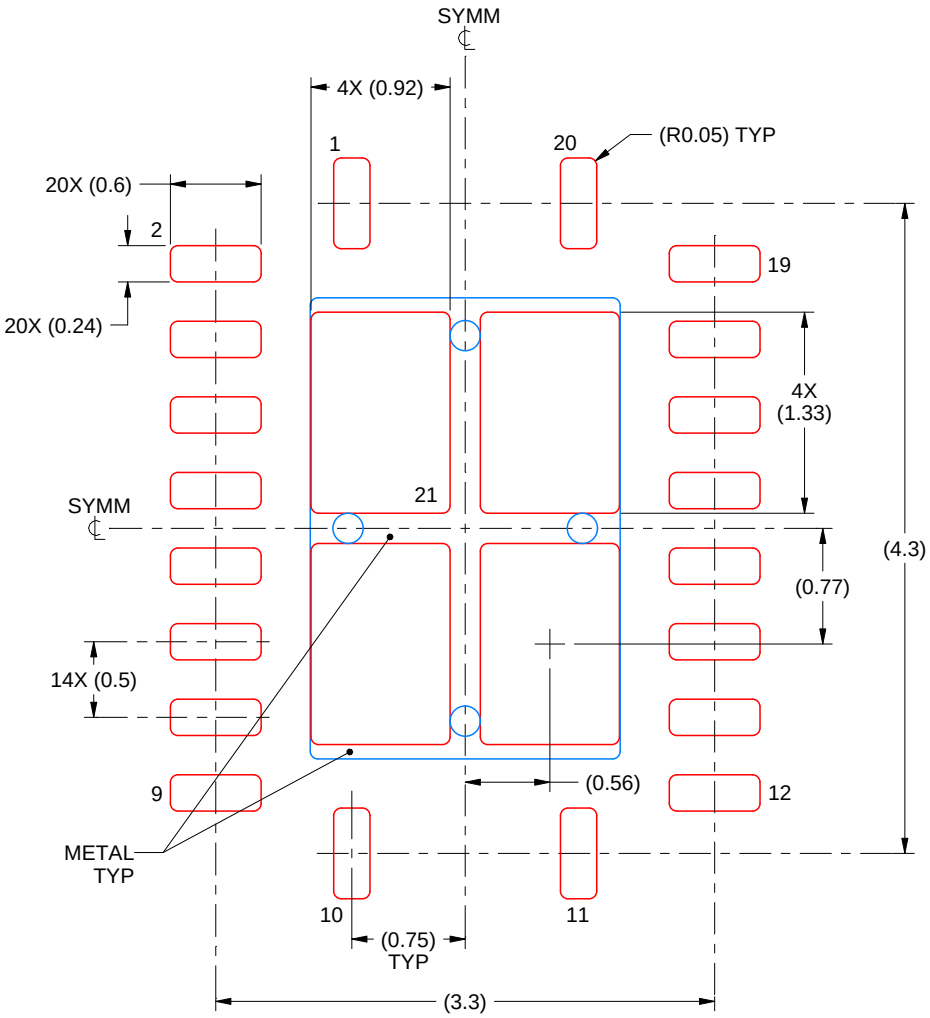



SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



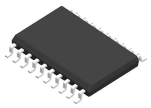

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

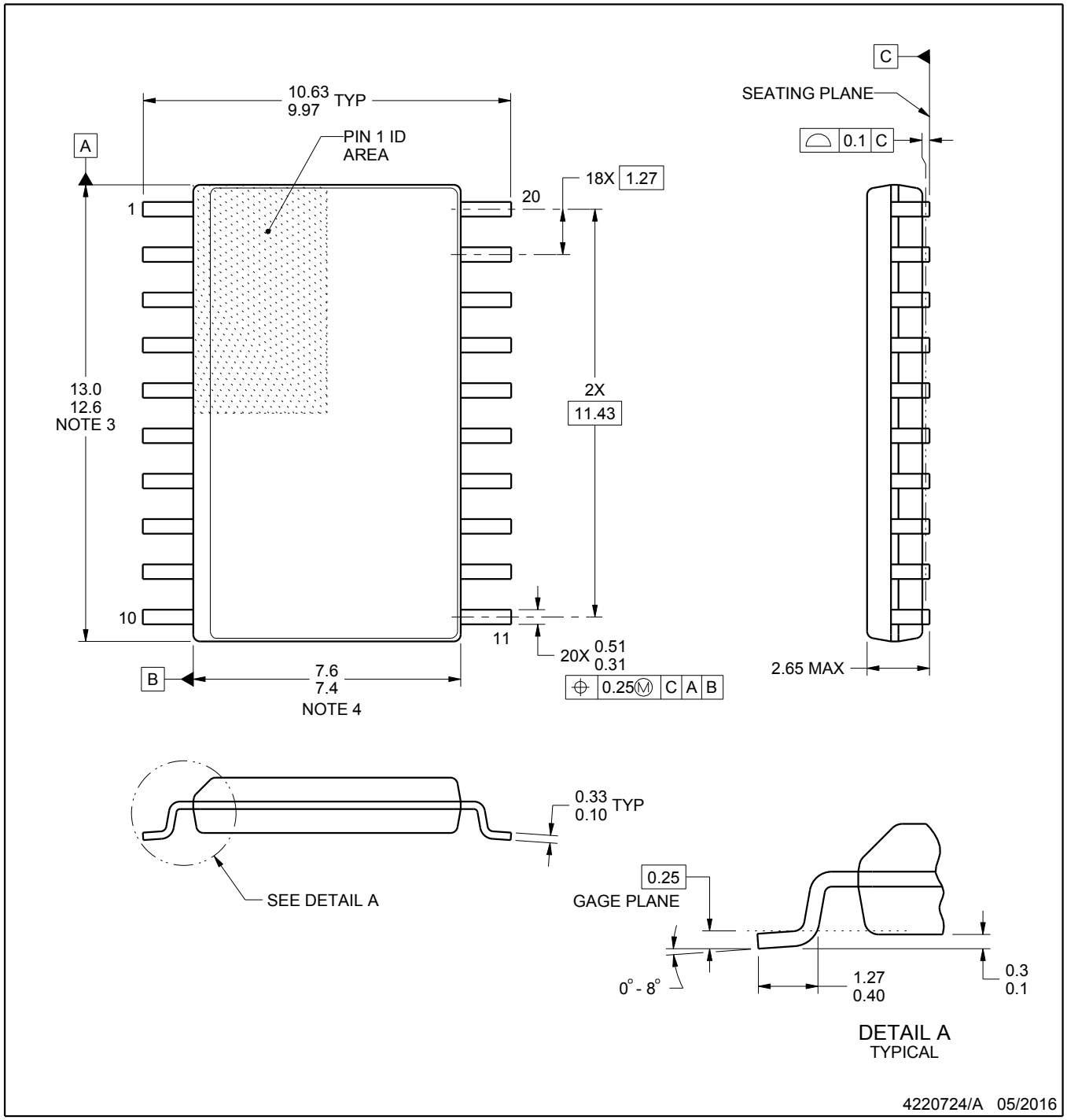


# PACKAGE OUTLINE

## DW0020A

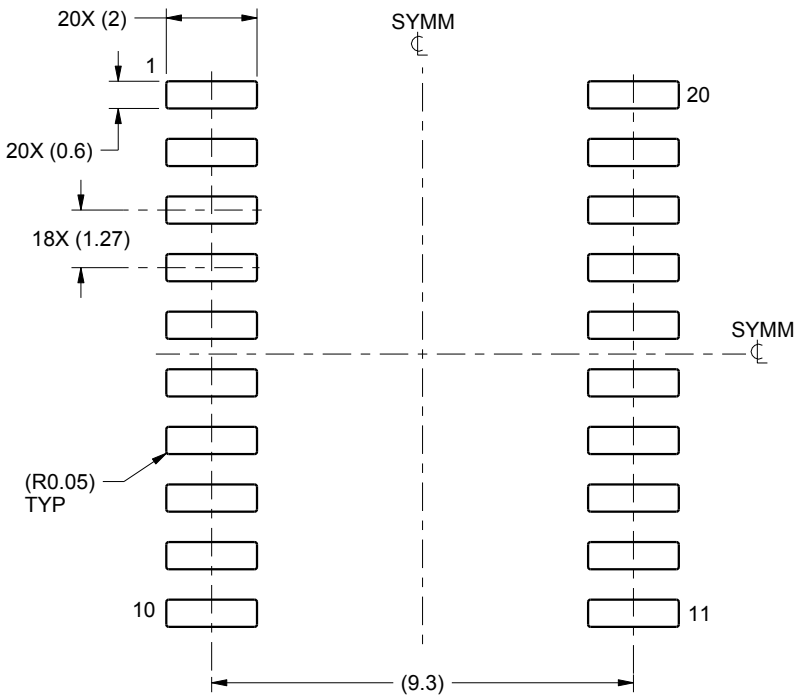
## SOIC - 2.65 mm max height

SOIC

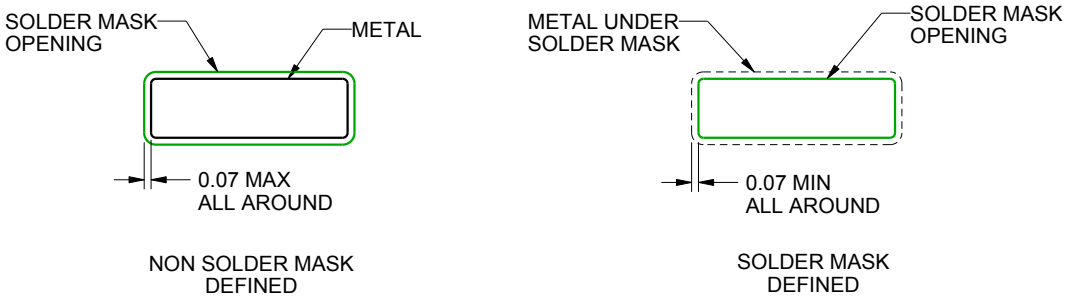



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

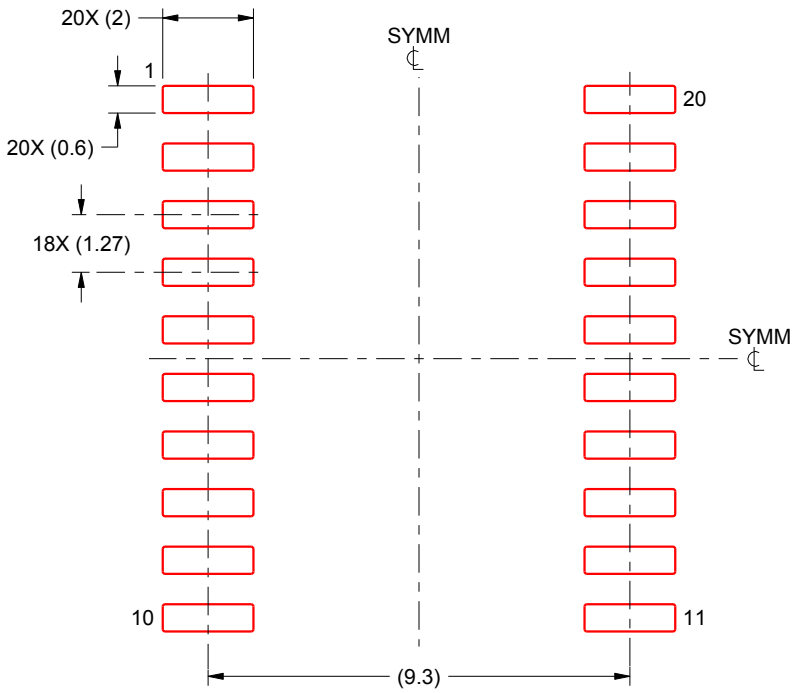



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

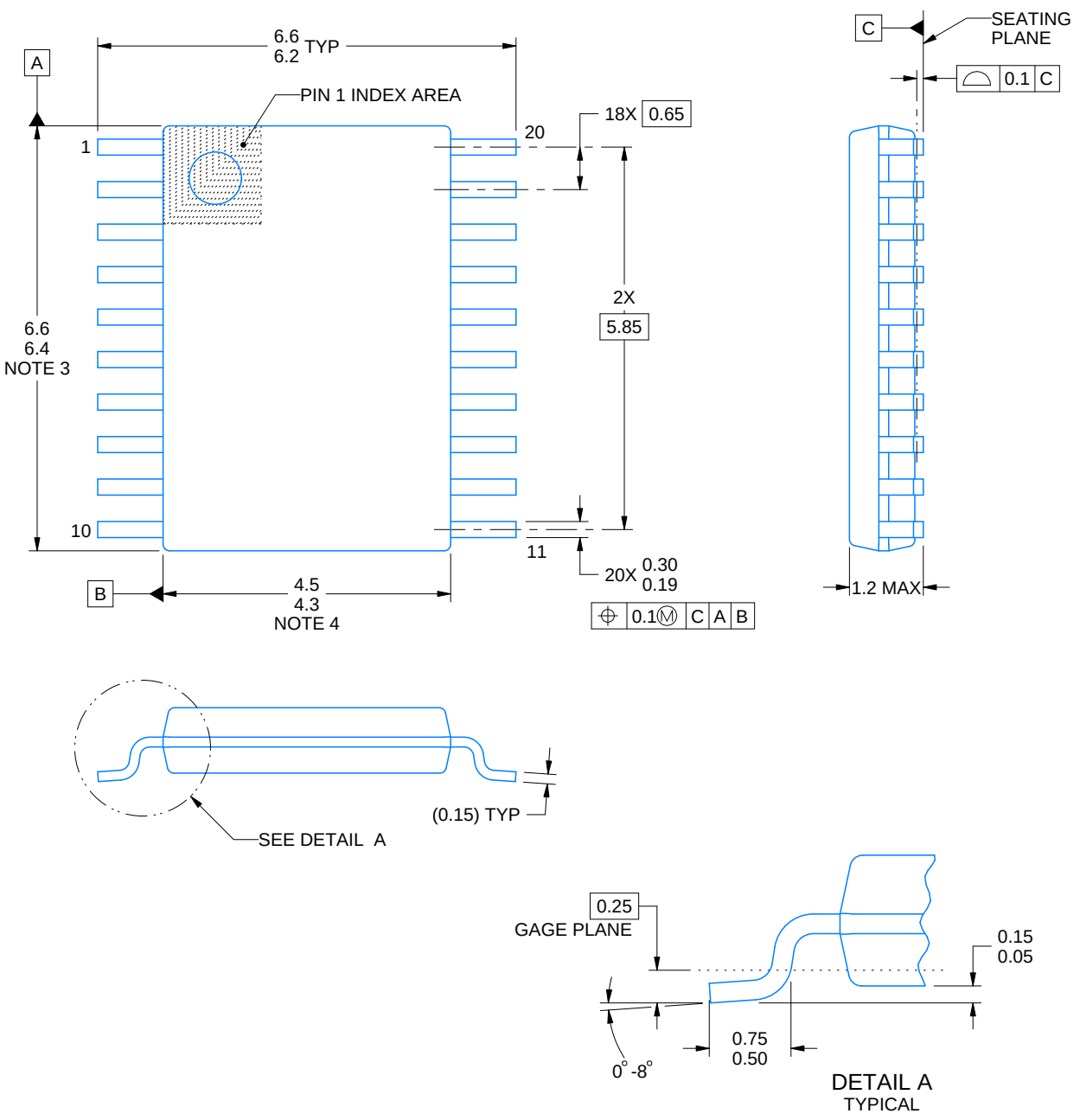
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## PW0020A

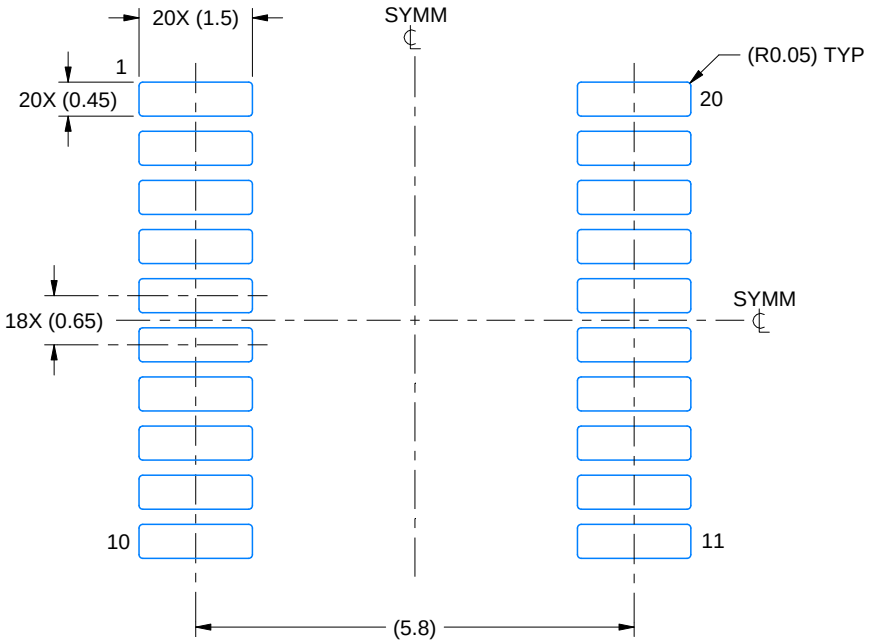
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

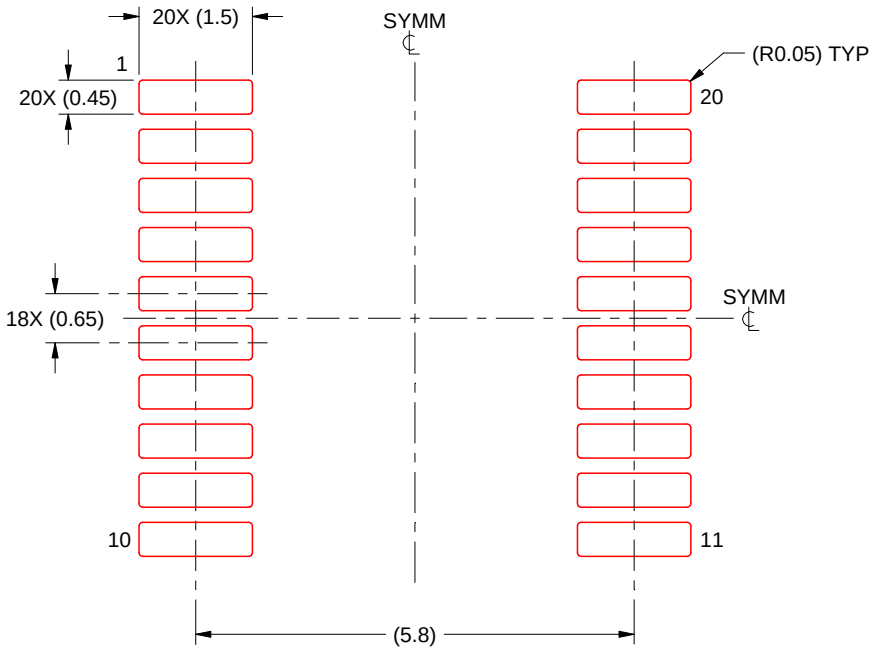



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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