DMP6110SFDF-13-VB Datasheet

P-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[d]	Q_g (Typ)
- 60	0.085 at V_{GS} = - 10 V	- 5	34
	0.100 at V_{GS} = - 4.5 V	- 4	

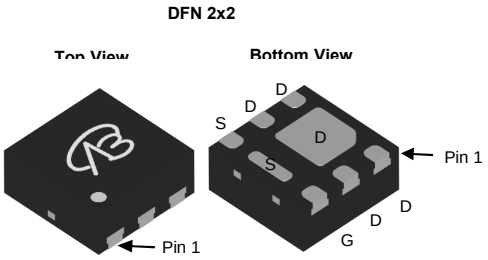
FEATURES

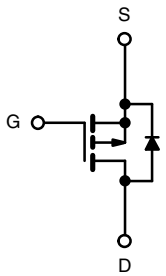
- **Halogen-free According to IEC 61249-2-21 Definition**
- Trench Power MOSFET
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC

RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

- High Side Switch for Full Bridge Converter
- DC/DC Converter for LCD Display





P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise note)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	- 5	A
	T_C = 100 °C		- 4	
Pulsed Drain Current		I_{DM}	- 15	
Avalanche Current, Single Pulse	L = 0.1 mH	I_{AS}	- 22	
Repetitive Avalanche Energy, Single Pulse[a]		E_{AS}	24.2	mJ
Power Dissipation	T_C = 25 °C	P_D	38.5[c]	W
	T_A = 25 °C		2.3[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b]	t ≤ 10 s	R_{thJA}	17	21	°C/W
	Steady State		45	55	
Maximum Junction-to-Case		R_{thJC}	2.7	3.25	

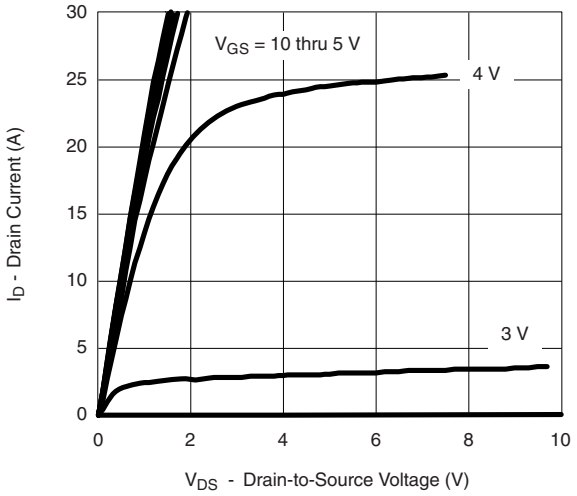
Notes:
a. Duty cycle ≤ 1 %.
b. When mounted on 1" square PCB (FR-4 material).
c. See SOA curve for voltage derating.
d. Based up on T_C = 25 °C.

SPECIFICATIONS (T_J = 25 °C, unless otherwise note)						
Parameter	**Symbol**	**Test Conditions**	**Min .**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 1		- 3	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 60 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 48 V, V_{GS} = 0 V, T_J = 125 °C			- 50	
		V_{DS} = - 48 V, V_{GS} = 0 V, T_J = 150 ° C			- 125	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = - 5 V, V_{GS} = - 10 V	- 20			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 10 A		0.085		Ω
		V_{GS} = - 10 V, I_D = - 10 A, T_J = 125 °C		0.127		
		V_{GS} = - 10 V, I_D = - 10 A, T_J = 150 °C		0.170		
		V_{GS} = - 4.5 V, I_D = - 5 A		0.100		
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 10 A		22		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = - 25 V, f = 1 MHz		1000		pF
Output Capacitance	C_{oss}			130		
Reverse Transfer Capacitance	C_{rss}			90		
Total Gate Charge[c]	Q_g	V_{DS} = - 30 V, V_{GS} = - 10 V, I_D = - 10 A		30	40	nC
Gate-Source Charge[c]	Q_{gs}			4.5		
Gate-Drain Charge[c]	Q_{gd}			7		
Gate Resistance	R_g	f = 1 MHz		7		Ω
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = - 30 V, R_L = 3 Ω I_D ≅ - 19 A, V_{GEN} = - 10 V, R_g = 2.5 Ω		8	15	ns
Rise Time[c]	t_r			9	15	
Turn-Off Delay Time[c]	$t_{d(off)}$			65	100	
Fall Time[c]	t_f			30	45	
Drain-Source Body Diode and Characteristics (T_C = 25 °C)[b]						
Continuous Current	I_S				- 5	A
Pulsed Current	I_{SM}				- 15	
Forward Voltage[a]	V_{SD}	I_F = - 19 A, V_{GS} = 0 V		-1	-1.5	V
Reverse Recovery Time	t_{rr}	I_F = - 19 A, di/dt = 100 A/µs		41	61	ns

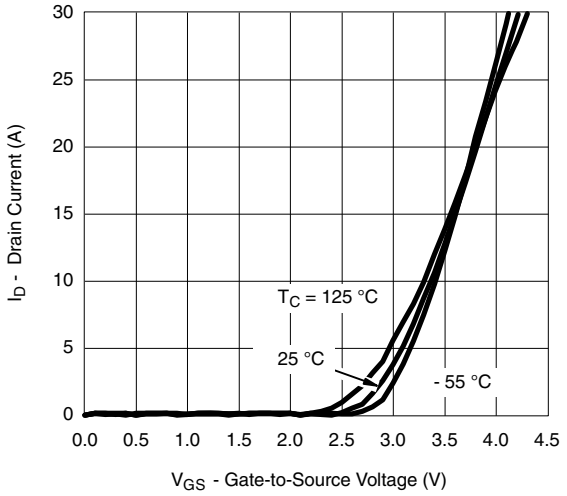
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

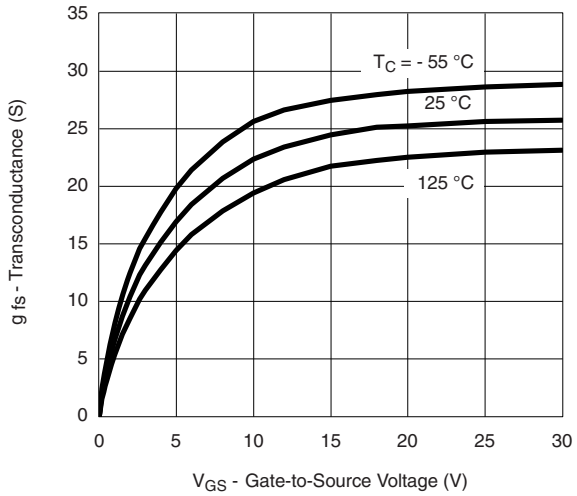
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



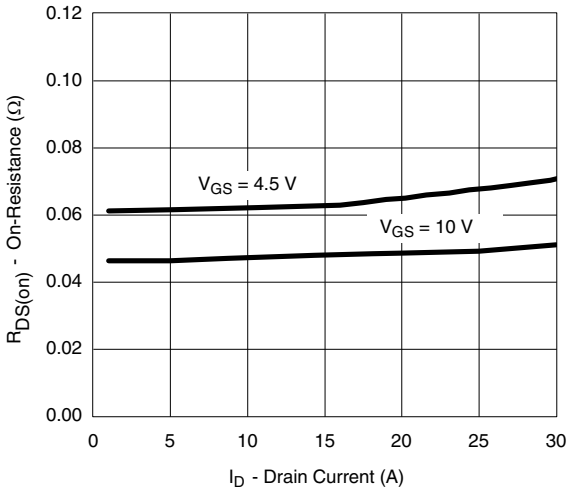
Output Characteristics



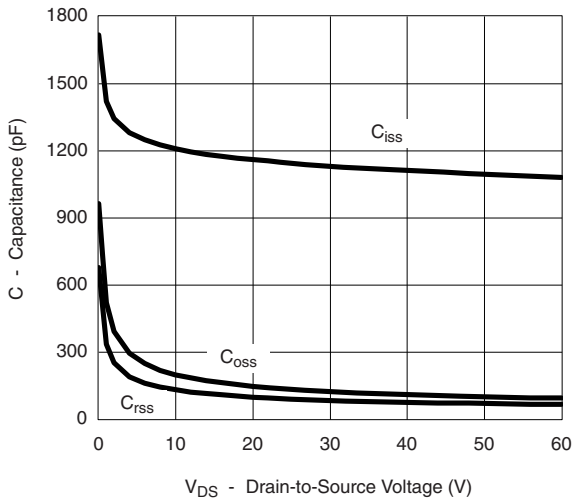
Transfer Characteristics



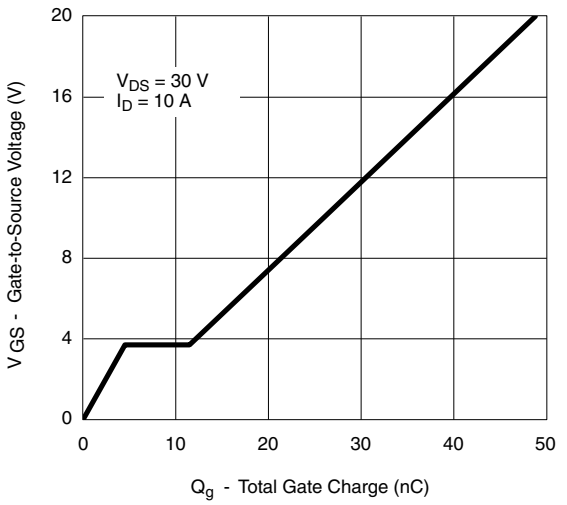
Transconductance



On-Resistance vs. Drain Current

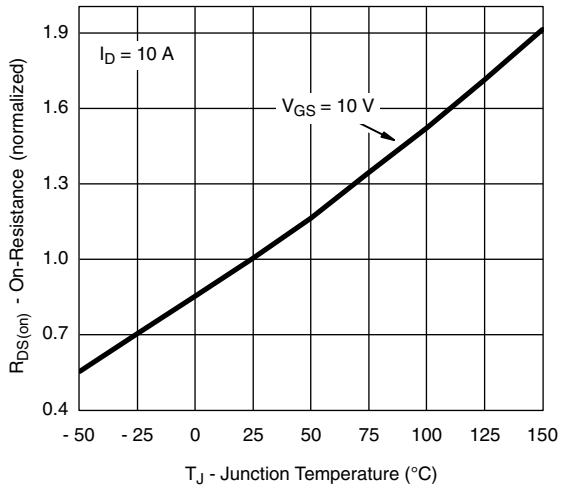


Capacitance

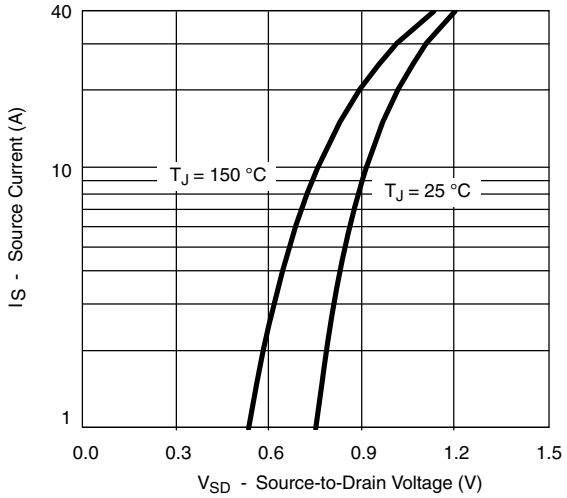


Gate Charge

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

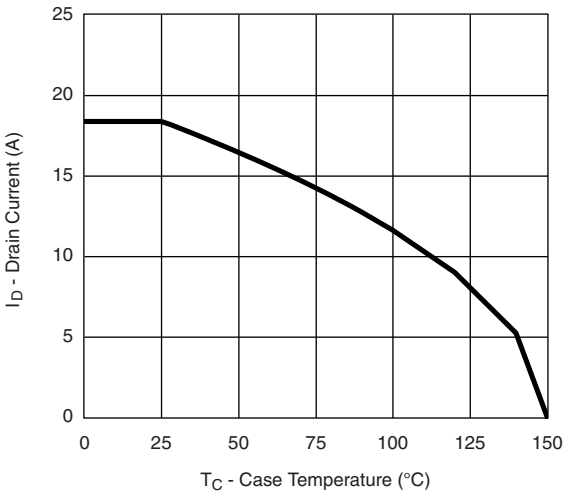


On-Resistance vs. Junction Temperature

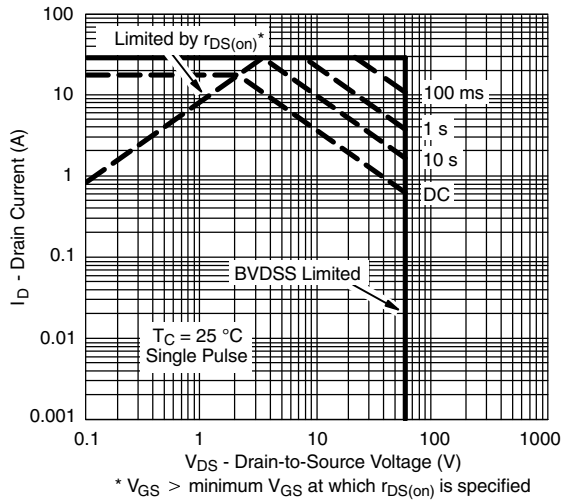


Source-Drain Diode Forward Voltage

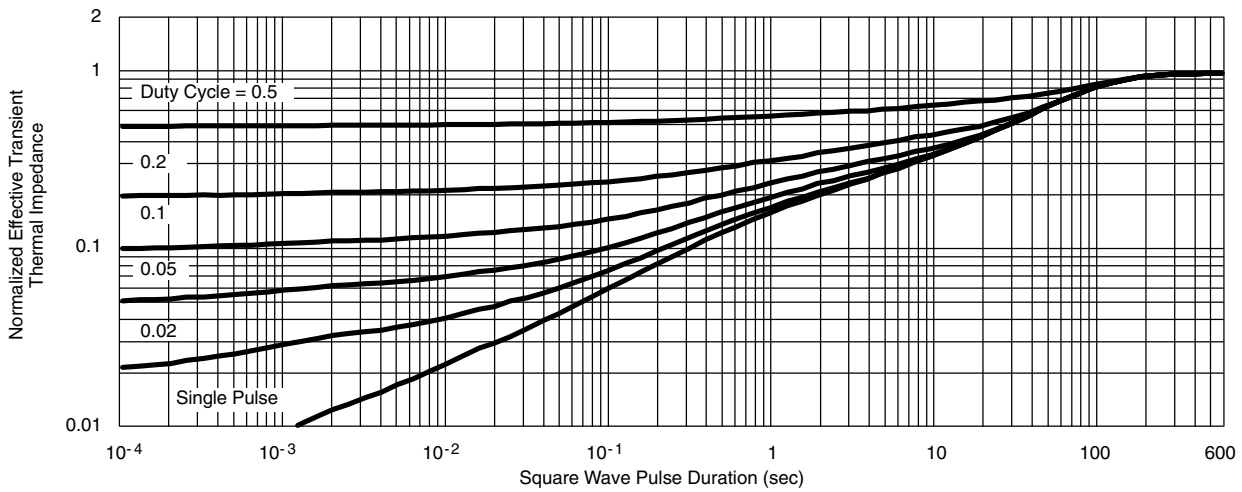
THERMAL RATINGS



Maximum Drain Current vs. Case Temperature

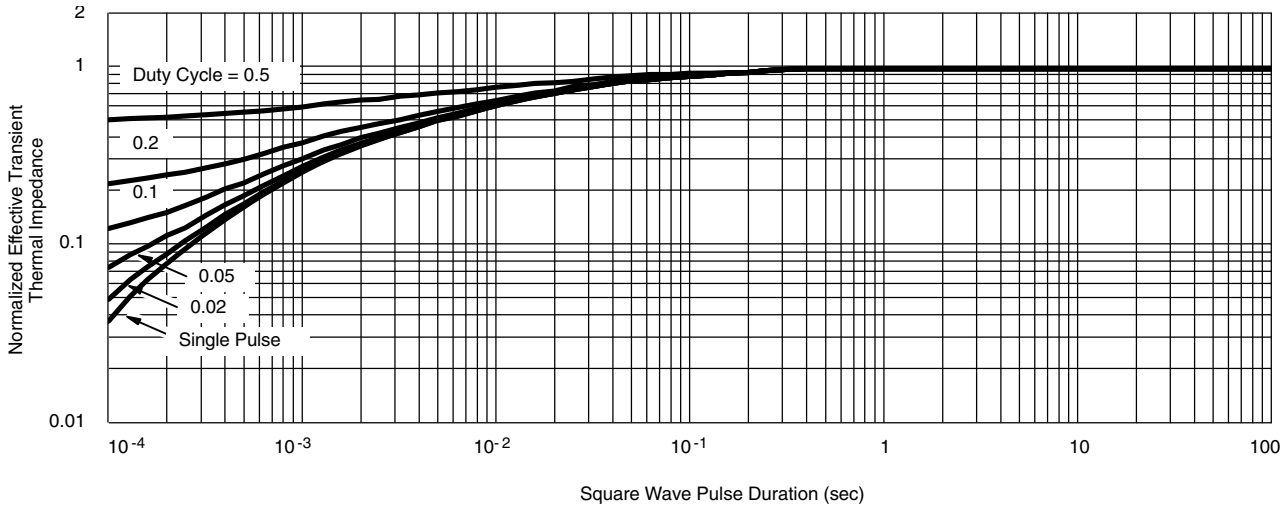


Safe Operating Area



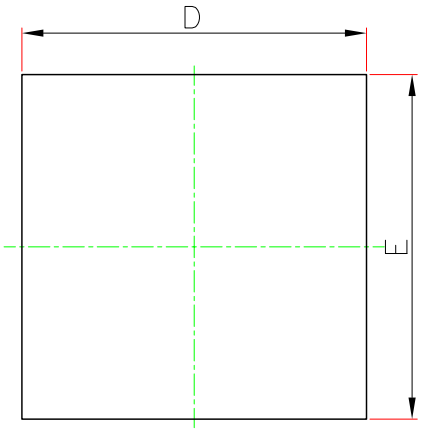
Normalized Thermal Transient Impedance, Junction-to-Ambient

THERMAL RATINGS

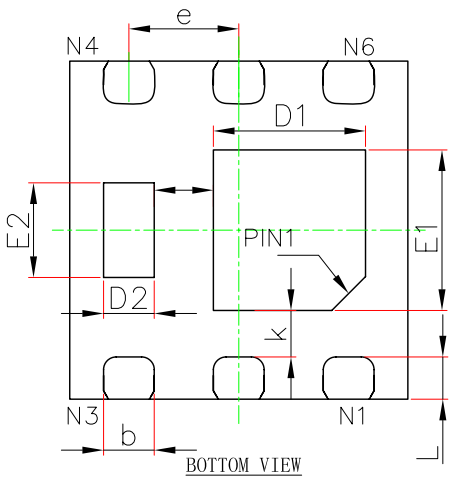


Normalized Thermal Transient Impedance, Junction-to-Case

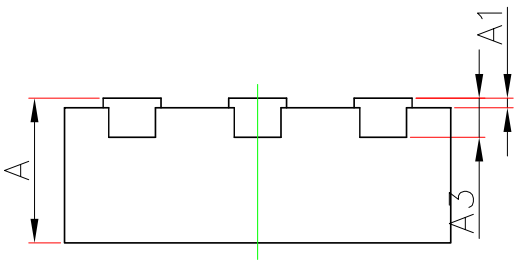
DFN2×2 Package Outline Dimensions



TOP VIEW
[顶视图]



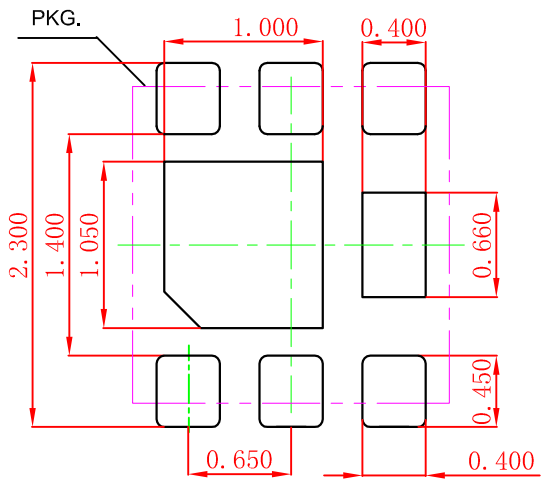
BOTTOM VIEW
[背视图]



SIDE VIEW
[侧视图]

Symbols	Dimensions in Milimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.152REF.		0.006REF.	
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D1	0.800	1.000	0.031	0.039
E1	0.850	1.050	0.033	0.041
D2	0.200	0.400	0.008	0.016
E2	0.460	0.660	0.018	0.026
b	0.250	0.350	0.010	0.014
e	0.650BSC.		0.026BSC.	
k	0.275REF.		0.011REF.	
k1	0.350REF.		0.014REF.	
L	0.200	0.300	0.007	0.012

DFN2×2 Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.050mm.
3.The pad layout is for reference purposes only.

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