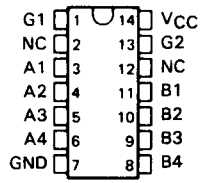
QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

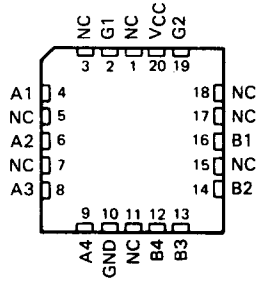
D2684, DECEMBER 1982 – REVISED JUNE 1989

- **2-Way Asynchronous Communication Between Data Buses**
- **High-Current Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Ceramic Chip Carriers and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC242, SN54HC243 . . . J PACKAGE
SN74HC242, SN74HC243 . . . N PACKAGE
(TOP VIEW)



SN54HC242, SN54HC243 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These four-data line tranceivers are designed for asynchronous two-way communications between data buses. The SN74HC' devices can be used to drive terminated lines down to 133 Ω.

These parts differ from their TTL counterparts (LS, ALS, and AS) in that these CMOS parts do not have a bus-latching mode in which both the outputs are simultaneously enabled. Instead of this latched mode, the buses are isolated, thus preventing potential bus conflicts if both buses are active. However, with the exception of the fourth line of the function table, their functional operation is identical to their TTL counterparts. The two enables have been renamed G1 and G2 since they work together to determine the direction of transmission rather than each enable controlling one direction independently of the other. Whenever G1 and G2 are at opposite logic levels with respect to each other, isolation between buses results.

The SN54HC' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC' family is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

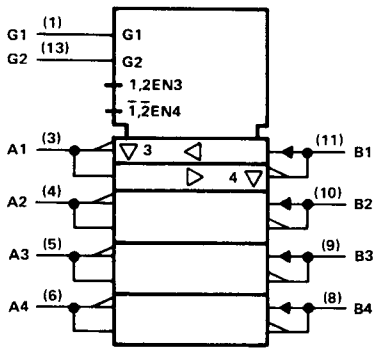
INPUTS		'HC242	'HC243
G1	G2		
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Isolation	Isolation

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

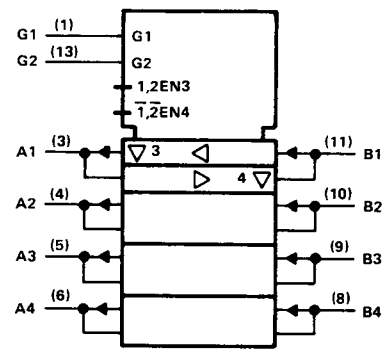
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logic symbols†

'HC242



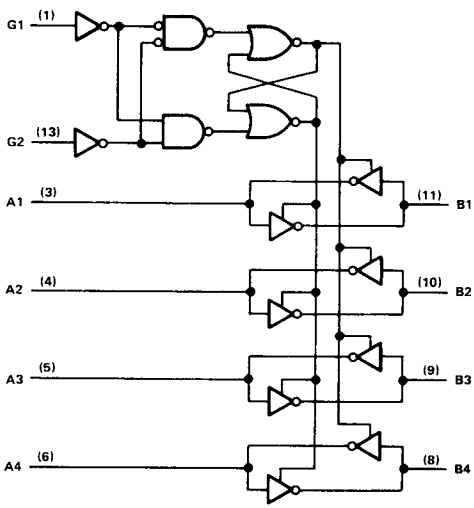
'HC243



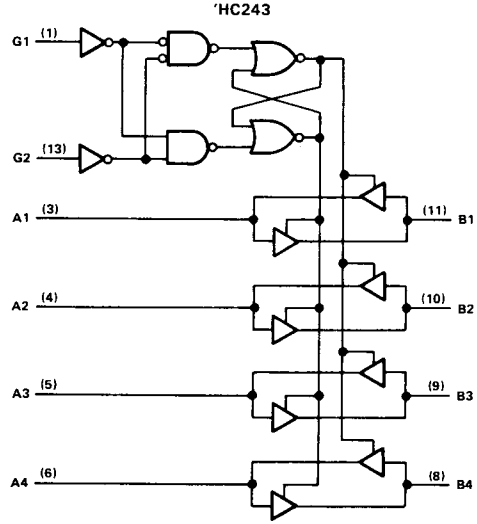
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

logic diagrams (positive logic)

'HC242



'HC243



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK}(V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK}(V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating contitions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC242 SN54HC243			SN74HC242 SN74HC243			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC242 SN54HC243		SN74HC242 SN74HC243		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}†	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL}	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i‡		2 to 6 V		3	10		10		10	pF

†For I/O ports, the parameter is included in the off-state output current.

‡This parameter C_i does not apply to I/O ports.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC242 SN54HC243		SN74HC242 SN74HC243		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		45	100		150		125	ns
			4.5 V		12	20		30		25	
			6 V		10	17		26		21	
t_{en}	G1 or G2	A or B	2 V		75	150		225		190	ns
			4.5 V		21	30		45		38	
			6 V		17	26		38		32	
t_{dis}	G1 or G2	A or B	2 V		48	150		225		190	ns
			4.5 V		23	30		45		38	
			6 V		20	26		38		32	
t_t		A or B	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	34 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC242 SN54HC243		SN74HC242 SN74HC243		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		63	150		225		190	ns
			4.5 V		17	30		45		38	
			6 V		14	26		38		32	
t_{en}	G1 or G2	A or B	2 V		100	200		300		250	ns
			4.5 V		26	40		60		50	
			6 V		21	34		51		43	
t_t		A or B	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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