# STL18N60M2-VB Datasheet

## N-Channel 650 V (D-S) Super Junction Power MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) at $T_J$ max. | 650 | |
| $R_{DS(on)}$ at 25 °C (Ω) | $V_{GS}$ = 10 V | 1.0 |

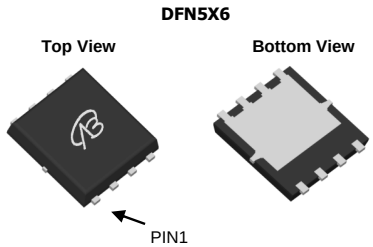
### FEATURES

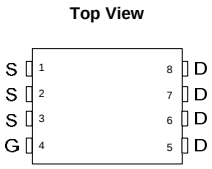
- Low figure-of-merit (FOM) $R_{on}$ x $Q_g$
- Low input capacitance ($C_{iss}$)
- Reduced switching and conduction losses
- Ultra low gate charge ($Q_g$)
- Avalanche energy rated (UIS)

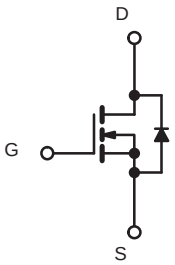
RoHS

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting




N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS ($T_C$ = 25 °C, unless otherwise noted) | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | | | **SYMBOL** | **LIMIT** | **UNIT** |
| Drain-Source Voltage | | | $V_{DS}$ | 650 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 30 | |
| Continuous Drain Current ($T_J$ = 150 °C) | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 5 | A |
| | | $T_C$ = 100 °C | | 3 | |
| Pulsed Drain Current [a] | | | $I_{DM}$ | 15 | |
| Linear Derating Factor | | | | 1.67 | W/°C |
| Single Pulse Avalanche Energy [b] | | | $E_{AS}$ | 550 | mJ |
| Maximum Power Dissipation | | | $P_D$ | 30 | W |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Drain-Source Voltage Slope | $T_J$ = 125 °C | | dV/dt | 50 | V/ns |
| Reverse Diode dV/dt [d] | | | | 15 | |
| Soldering Recommendations (Peak Temperature) [c] | for 10 s | | | 260 | °C |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. $V_{DD}$ = 100 V, starting $T_J$ = 25 °C, L = 30mH, $R_g$ = 25 Ω, $I_{AS}$ =13A.
c. 1.6 mm from case.
d. $I_{SD} \leq I_D$, dI/dt = 100 A/μs, starting $T_J$ = 25 °C.

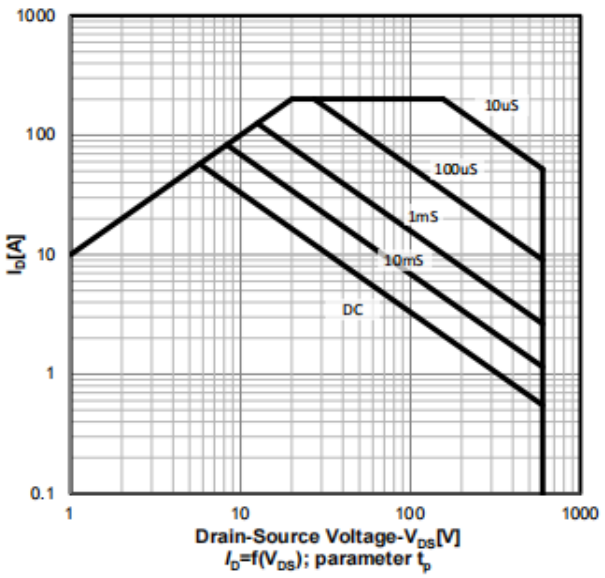
| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | 62 | °C/W |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | 0.38 | |

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 650 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | - | 0.70 | - | V/°C |
| Gate-Source Threshold Voltage (N) | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2.5 | - | 4.5 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 20 V | - | - | ± 100 | nA |
| | | $V_{GS}$ = ± 30 V | - | - | ± 1 | µA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 650V, $V_{GS}$ = 0 V | - | - | 1 | µA |
| | | $V_{DS}$ = 520 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | - | - | 100 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ =1.5A | - | 1.0 | - | Ω |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 30 V, $I_D$ = 1.5A | - | 5.6 | - | S |
| **Dynamic** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 100 V, f = 1 MHz | - | 450 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 50 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 4 | - | |
| Effective Output Capacitance, Energy Related [a] | $C_{o(er)}$ | $V_{DS}$ = 0 V to 520 V, $V_{GS}$ = 0 V | - | 63 | - | |
| Effective Output Capacitance, Time Related [b] | $C_{o(tr)}$ | | - | 213 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 10 V; $I_D$ = 3 A, $V_{DS}$ = 520 V | - | 20 | - | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 39 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 47 | - | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 520 V, $I_D$ = 3A, $V_{GS}$ = 10 V, $R_g$ = 9.1 Ω | - | 18 | 25 | ns |
| Rise Time | $t_r$ | | - | 24 | 55 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 80 | - | |
| Fall Time | $t_f$ | | - | 12 | - | |
| Gate Input Resistance | $R_g$ | f = 1 MHz, open drain | - | 0.8 | - | Ω |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 5 | A |
| Pulsed Diode Forward Current | $I_{SM}$ | | - | - | 15 | |
| Diode Forward Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 3 A, $V_{GS}$ = 0 V | - | - | 1.5 | V |
| Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = $I_S$ = 3 A, dI/dt = 100 A/µs, $V_R$ = 400 V | - | 80 | - | ns |
| Reverse Recovery Charge | $Q_{rr}$ | | - | 5.8 | - | µC |
| Reverse Recovery Current | $I_{RRM}$ | | - | 45 | - | A |

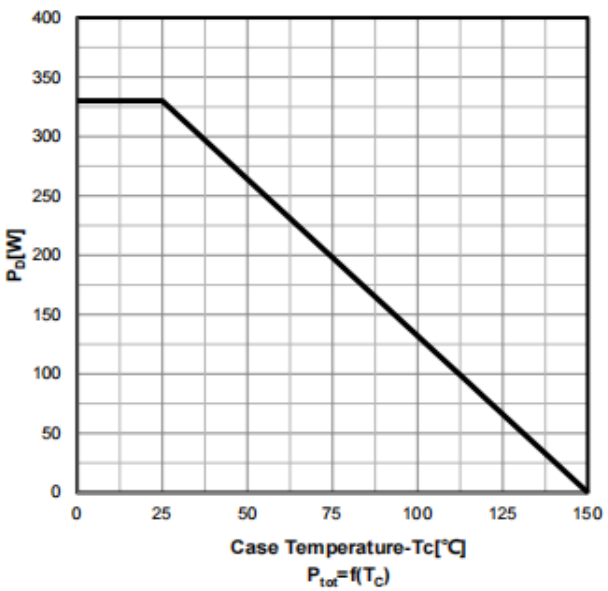
**Notes**

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DSS}$.
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DSS}$.

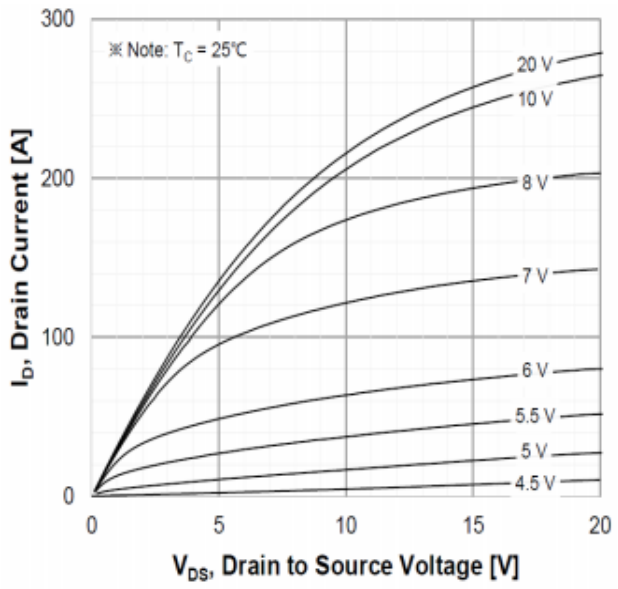
Safe operating area TC=25 ℃
TO-247



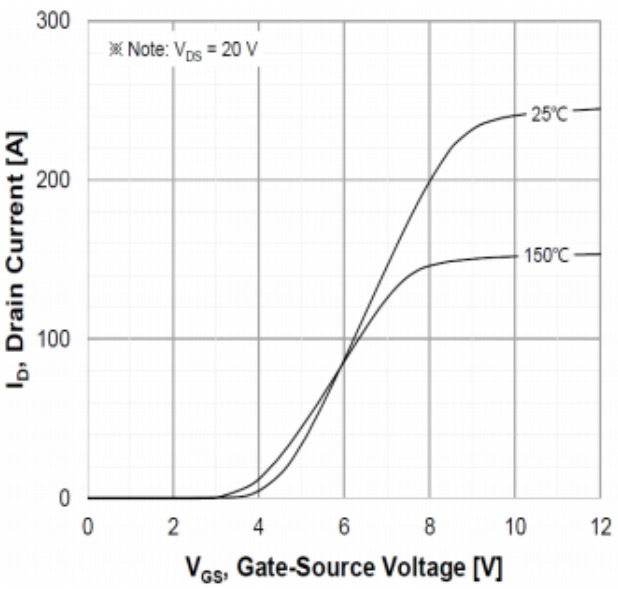

Power dissipation



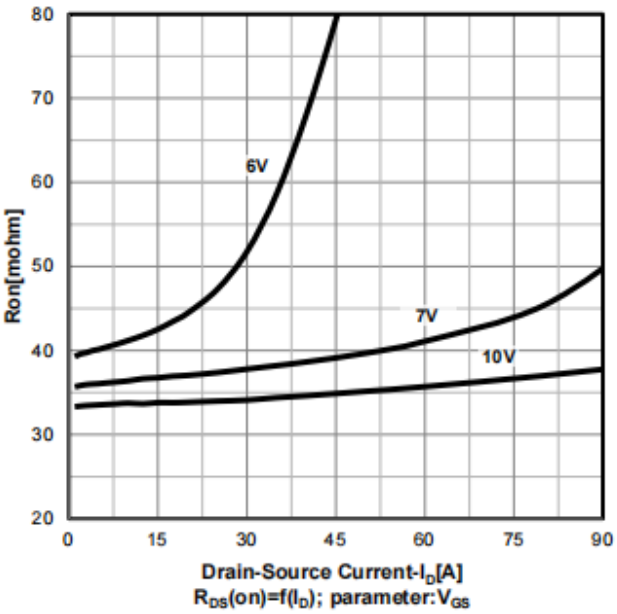

Typ. output characteristics $T_j$=25 ℃



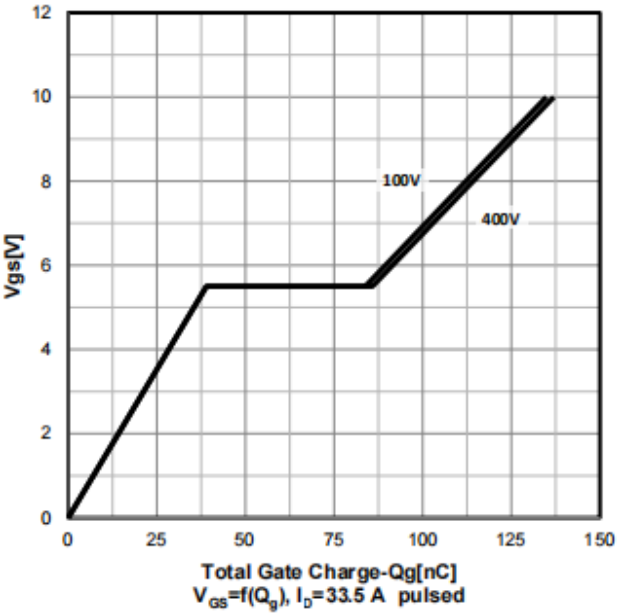

Transfer characteristics



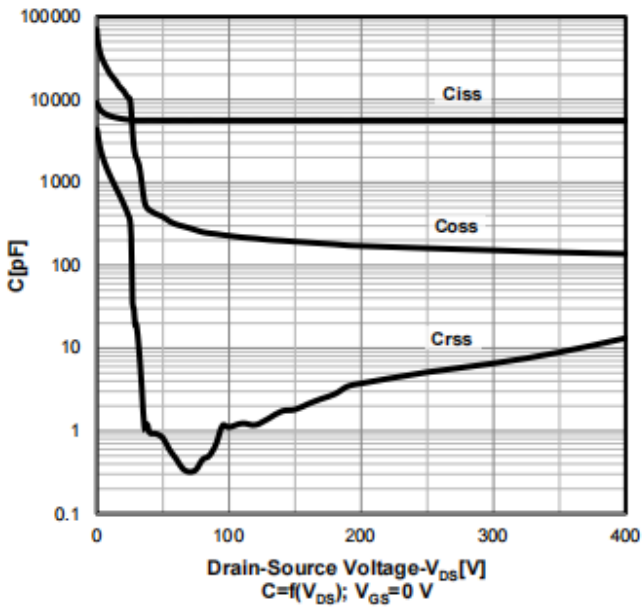
Typ. drain-source on-state resistance



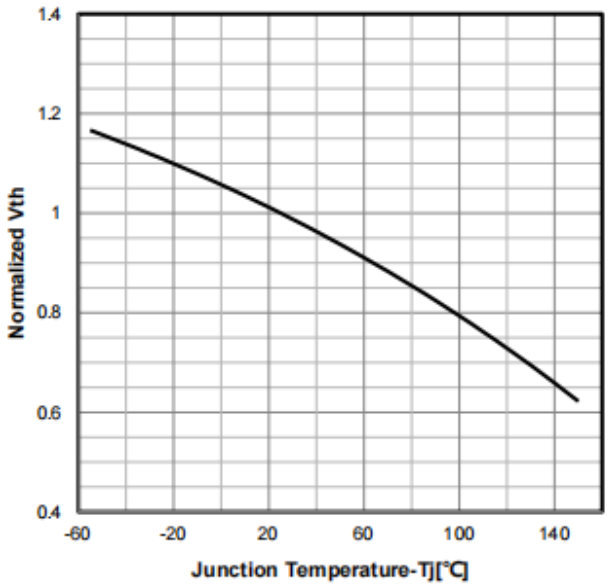

Typ. gate charge characteristics



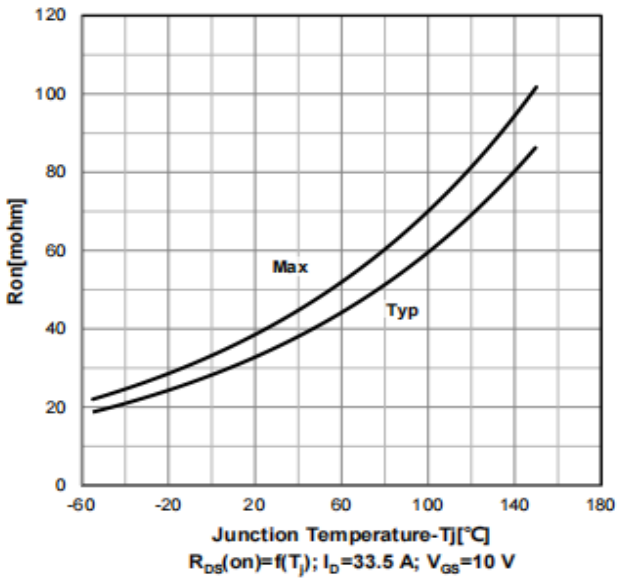

Typ. capacitances



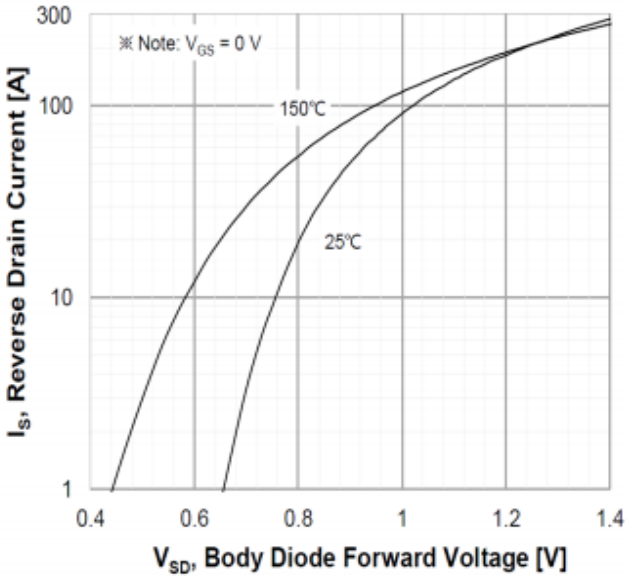

Normalized $V_{GS(th)}$ characteristics



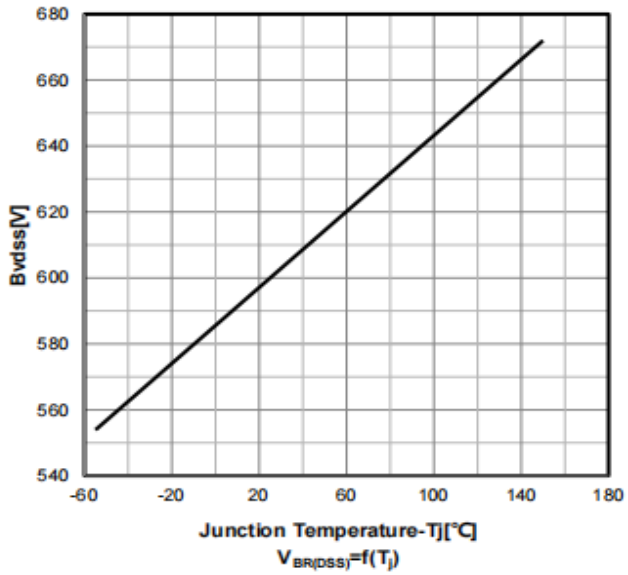
On-resistance vs temperature



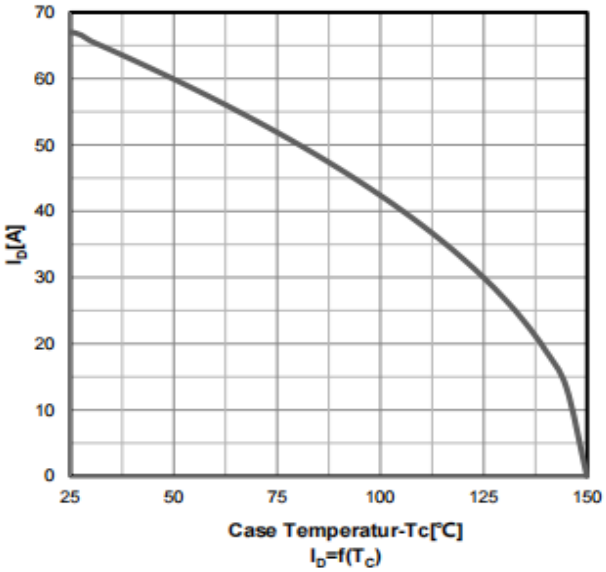

Forward characteristics of reverse diode



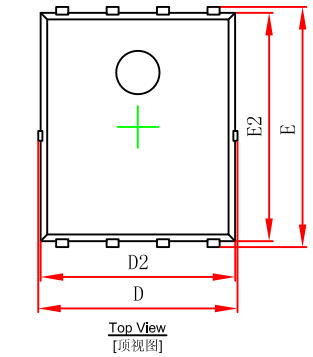

Drain-source breakdown voltage



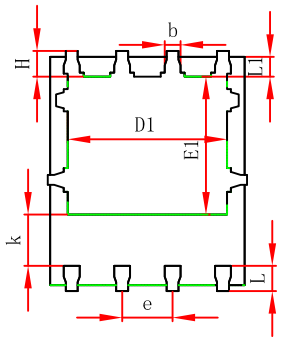

Drain current vs temperature



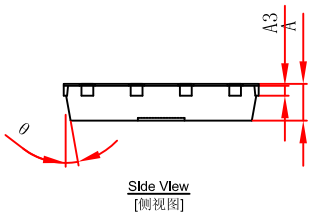
## PDFNWB5x6-8L Package Outline Dimensions




Top View
[顶视图]



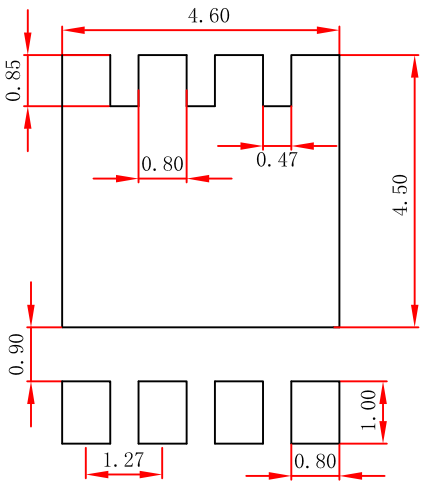

Bottom View
[背视图]




Side View
[侧视图]

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 0.900 | 1.000 | 0.035 | 0.039 |
| A3 | 0.254REF. | | 0.010REF. | |
| D | 4.944 | 5.096 | 0.195 | 0.201 |
| E | 5.974 | 6.126 | 0.235 | 0.241 |
| D1 | 3.910 | 4.110 | 0.154 | 0.162 |
| E1 | 3.375 | 3.575 | 0.133 | 0.141 |
| D2 | 4.824 | 4.976 | 0.190 | 0.196 |
| E2 | 5.674 | 5.826 | 0.223 | 0.229 |
| k | 1.190 | 1.390 | 0.047 | 0.055 |
| b | 0.350 | 0.450 | 0.014 | 0.018 |
| e | 1.270TYP. | | 0.050TYP. | |
| L | 0.559 | 0.711 | 0.022 | 0.028 |
| L1 | 0.424 | 0.576 | 0.017 | 0.023 |
| H | 0.574 | 0.726 | 0.023 | 0.029 |
| θ | 10° | 12° | 10° | 12° |

## PDFNWB5x6-8L Suggested Pad Layout




Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

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