SiT3907
High Precision Digitally Controlled Oscillator (DCXO)

SiTime™
The Smart Timing Choice™

Features

- Factory programmable between 1 MHz and 220 MHz
- Digitally controlled pull range: ±25, ±50, ±100, ±200, ±400, ±800, ±1600 PPM
- Eliminate the need for an external DAC
- Superior pull range linearity of <= 0.01%
- LVCMOS/LVTTL compatible output
- Three industry-standard packages: 3.2 mm x2.5 mm (4-pin), 5.0 mm x 3.2 mm (6-pin), 7.0 mm x 5.0 mm (6-pin)
- Programmable drive strength to reduce EMI
- Outstanding silicon reliability of 2 FIT

Applications

- Ideal for clock synchronization, instrumentation, low bandwidth PLL, jitter cleaner, clock recovery, audio, video, and FPGA



Electrical Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency Range	f	1	–	220	MHz	
Frequency Stability	F_stab	-10	–	+10	PPM	Inclusive of initial tolerance, operating temperature, rated power, supply voltage and load change
		-25	–	+25	PPM	
		-50	–	+50	PPM	
Aging	F_aging	-5	–	+5	PPM	10 years
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage	Vdd	1.71	1.8	1.89	V	
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.97	3.3	3.63	V	
Pull Range	PR	±25, ±50, ±100, ±200 ±400, ±800, ±1600			PPM	See the last page for Absolute Pull Range, APR table
Linearity	Lin	–	–	0.01	%	
Frequency Change Polarity	–	Positive Slope			–	
Frequency Update Rate	F_update	–	–	25	kU / s	Frequency control mode 1, see Table 1
		–	–	12.5	kU / s	Frequency control mode 2, see Table 2
Current Consumption	Idd	–	32	34	mA	No load condition, f = 100 MHz, Vdd = 2.5V, 2.8V or 3.3V
		–	31	34	mA	No load condition, f = 100 MHz, Vdd = 1.8 V
Duty Cycle	DC	45	–	55	%	Vdd = 1.8V, 2.5V, 2.8V or 3.3V
Rise/Fall Time	Tr, Tf	–	1.2	2	ns	Vdd =1.8V, 2.5V, 2.8V or 3.3V, 10% - 90% Vdd level
Output High Voltage	VOH	90	–	–	%Vdd	IOH = -6mA, Vdd = 3.3V, 2.8V, 2.5V IOL = -3mA, Vdd = 1.8V
Output Low Voltage	VOL	–	–	10	%Vdd	IOH = -6mA, Vdd = 3.3V, 2.8V, 2.5V IOL = -3mA, Vdd = 1.8V
Output Load	Ld	–	–	15	pF	
Start-up Time	T_start	–	6	10	ms	
Input Low Voltage	VIL	–	–	0.2xVdd	V	See Figure 5
Input Middle Voltage	VIM	0.4xVdd	–	0.6xVdd	V	See Figure 5
Input High Voltage	VIH	0.8xVdd	–	–	V	See Figure 5
Input High or Low Logic Pulse	T_logic	500	–	–	ns	See Figure 5
Input Middle Pulse Width	T_middle	500	–	–	ns	See Figure 5
Input Impedance	Zin	100	–	–	kΩ	
Input Capacitance	Cin	–	5	–	pF	20% to 80%
RMS period Jitter	T_jitt	–	1.5	2	ps	f = 20 MHz, all Vdds
		–	2	3	ps	f = 20 MHz, all Vdds
RMS Phase Jitter (random)	T_phj	–	0.6	1	ps	f = 20 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds. No activity on DP pin.
		–	0.65	1	ps	With full activity on DP pin.

Notes:
1. Absolute Pull Range (APR) is defined as the guaranteed pull range over temperature and voltage.
2. APR = pull range (PR) - frequency stability (F_stab) - Aging (F_aging)

Pin Description (4-pin device)

Pin	Map	Functionality
1	Digital Programming Pin (DPpin)	See “Frequency Control Protocol Description” section
2	GND	Electrical ground[3]
3	CLK	Oscillator output
4	VDD	VDD power supply[3]

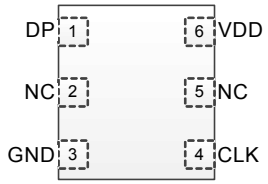
Top View



Pin Description (6-pin device)

Pin	Map	Functionality
1	Digital Programming Pin (DPpin)	See “Frequency Control Protocol Description” section
2	NC	No connect
3	GND	Electrical ground[3]
4	CLK	Oscillator output
5	NC	No connect
6	VDD	VDD power supply[3]

Top View



Note:
3. A capacitor value of 0.1 µF between VDD and GND is required.

Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	**MIL-STD-883F, Method 2002**
Mechanical Vibration	**MIL-STD-883F, Method 2007**
Temperature Cycle	**JESD22, Method A104**
Solderability	**MIL-STD-883F, Method 2003**
Moisture Sensitivity Level	**MSL1 @ 260°C**

Description

SiT3907 device is a digitally controlled programmable oscillator (DCXO), which allows pulling the frequency around a nominal value dynamically. User can communicate with the device through a 1-pin tri-level serial interface. This device has two DCXO registers, which control the amount of frequency pull. Once the registers are set, the device sets its output frequency to a new value dynamically. The pull range is programmable to a maximum of ±1600 PPM. The resolution varies between1 part-per-billion (ppb) and 50 ppb depending on total pull range selected. Writing into the DCXO registers does not cause any interruptions of output oscillations; the frequency will switch from one value to the new one smoothly.

The device allows two modes of operation. In mode 1, user can set one of the DCXO registers to control frequency. In mode 2, the user can set both registers to achieve better resolution while maintaining wide pull ranges.

Default Startup Condition

The SiT3907 starts up at its factory programmed frequency. The DCXO registers values are initialized all zeros, effectively setting the frequency to the middle of the control range.

Frequency Control Protocol Description

The device includes two DCXO registers. Data for each register is written to the device using a data frame.

Data Frame Format

Each frame consists of 40 bits. A frame has 3 parts:

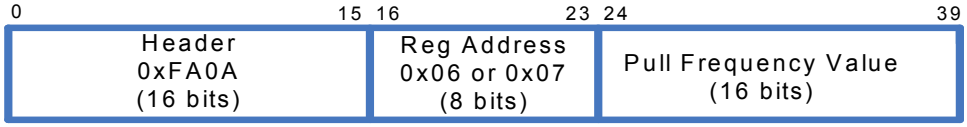
- The header, 16 bits

- Register address, 8 bits

- Pull frequency (PF) value represented as 2's complement binary number, 16 bits or 23 bits depending on programming mode explained in the following paragraphs.

Most significant bits of a frame are sent first. When writing to both DCXO registers, the least significant word is sent first.

The header allows the devices to recognize that the master is initiating communication. The header includes the device address, which is factory programmable. The valid header format is 0xFAIA, where "I" can be a hex digits from 0 to F. If not specified at the order time, the device address will be defaulted to zero. For all examples and in this document, the device address is considered to be zero (default).



Frequency Control Mode 1

In this resolution mode, only one frame per frequency update is required, and the output frequency is updated at the end of each frame. The length of the pull frequency data is 16 bits, and is written to the device as shown below:



Figure 1. Frequency Control Mode 1

Frequency Control Mode 2

In this mode, two frames per frequency update are required, and frequency is only updated at the end of the second frame. The pull frequency value in this mode is 23 bits. This value is written to the device in two frames as Figure 2. Note that register (address: 0x07) carries the most significant 7 bits as indicated by the XXXXXXX in Figure 2. The rest of the most significant bits must be set to 0.

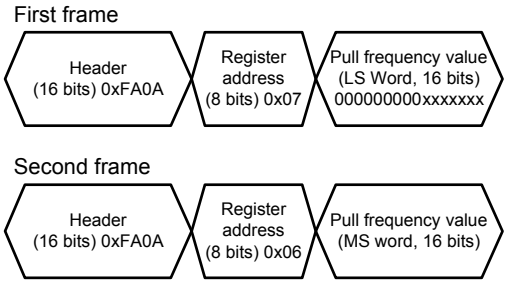


Figure 2. Frequency Control Mode 2

Pull Range (PPM)	Step Resolution (ppb)	Max Update Rate (Updates Per Second)
±25	1	25 K
±50	1.5	25 K
±100	3	25 K
±200	6	25 K
±400	12	25 K
±800	25	25 K
±1600	49	25 K

Table 1. Resolution and Update Rate for Mode 1

Pull Range (PPM)	Step Resolution (ppb)	Max Update Rate (Updates Per Second)
±25	1	12.5 K
±50	1	12.5 K
±100	1	12.5 K
±200	1	12.5 K
±400	1	12.5 K
±800	1	12.5 K
±1600	1	12.5 K

Table 2. Resolution and Update Rate for Mode 2

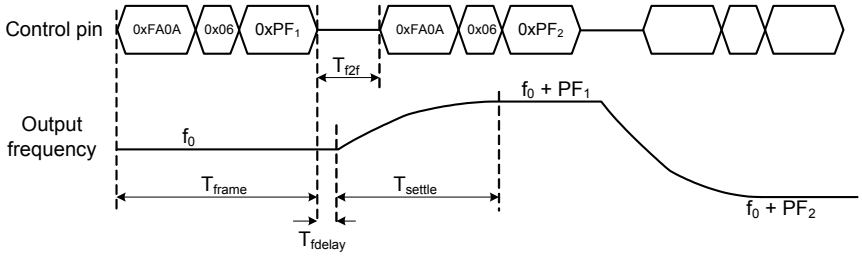


Figure 3. Mode 1 Frame Timing

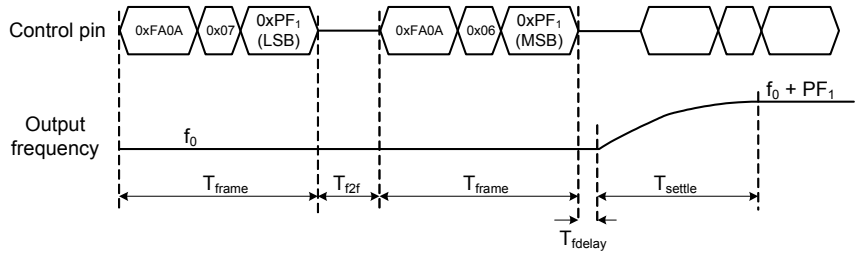


Figure 4. Mode 2 Frame Timing

Frame Timing Parameters

Parameter	Symbol	Min.	Max.	Unit
Frame Length	T_{frame}	40	—	µS
Frame to Frame Delay	T_{f2f}	2	—	µS
Frequency Settling Time	T_{settle}	—	30	µS
Frame to Frequency Delay	T_{fdelay}	—	8	µS

Calculating Pull Frequency Values

The frequency control value must be encoded as a 2's complement number (16-bit in mode 1 and 23-bit in mode 2), representing the full scale range of the device. For example, for a ±1600ppm device in mode 2, the 23-bit number represents the full ±1600ppm range.

The upper 16 bits of the value are written to address 0x06. If the high-resolution register (address 0x07) is used, the other 7 bits are written to the lowest seven bits of address 0x07.

Here are the steps to calculate the pull frequency (PF) value:

1. Find the scale factor (calculated for half of the pull range) from the tables below where PR is the Pull Range:

K (scale) Factor

Mode	K = Scale Factor
1	(2^15-1) / (PR*1.00135625)
2	(2^22-1) / (PR*1.00135625)

2. Enter the desired_PPM in equation below:
   Frequency control (decimal value) = round (desired_PPM * K).
3. For any frequency shifts (positive or negative PPM), convert the frequency control value to a 2's complement binary number.

Two examples follow:

Example 1

This example shows how to shift the frequency by +245.6 ppm in a device with ±1600 pull range using Mode 2 (23-bit):

Decimal value: round(245.6 * K) = 642954
23-bit value = 0x09CF8A

LS Word value = 0x000A (to be written to address 0x07)
MS Word value = 0x139F (to be written to address 0x06)
Write LS Word: 0xFA0A 07 000A (Frequency will not update)
Write MS Word: 0xFA0A 06 139F (Frequency updates after write)

Example 2

This example shows how to shift the frequency by -831.2 ppm in a device with ±1600 pull range using Mode 2 (23-bit):

Decimal value: round(abs(831.2 * K) = 2175989
23-bit abs binary value: 0100001001100111110101
23-bit 2's comp binary value: 1011110110011000 0001011
LS Word value = 0x 000B
MS Word value = 0x BD98
Write LS Word: 0xFA0A 07 000B (Frequency will not update)
Write MS Word: 0xFA0A 06 BD98 (Frequency updates after write)

Physical Interface

The SiTime DCMO uses a serial input interface to adjust the pull frequency value. The interface uses a one-wire tri-level return-to-middle signaling format. Figure 5 below shows the signal waveform of the interface.

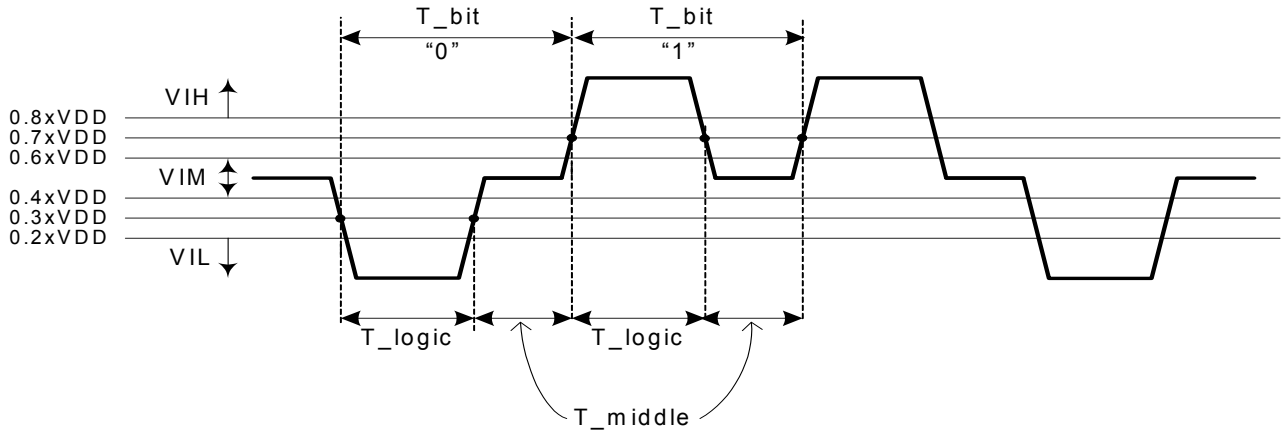


Figure 5. Serial 1-Wire Tri-Level Signaling

A logical bit "1" is defined by a high-logic followed by mid-logic. A logical bit "0" is defined by a low-logic followed by mid-logic. The voltage ranges and time durations corresponding to low-logic, high-, and mid-logic are illustrated in Figure 5 and specified in electrical specification table.

The overall baud rate is computed as below:

$$baud_rate = \frac{1}{T_bit}$$

Figure 6 shows a simple circuit to generate tri-level circuit with a general purpose IO (GPIO) with tri-state capability. Most FPGAs and micro controllers/processors include such GPIOs. If the GPIO does not support tri-state output, two IO s may be used in combination with external tri-state buffer to generate the tri-level signal; an example of such buffer is the SN74LVC1G126. The waveform at the output of the tri-state buffer is shown in Figure 7. When the GPIO drives Low or High voltage, the rise/fall times are typically fast (sub-5ns range). When the output is set to Hi-Z, the output settles at middle voltage with a RC response. The time constant is determined based on the total capacitance on frequency control pin and the parallel resistance of the pull-up and pull-down resistors. The time constant in most practical situations will be less than 50ns; this necessitate choosing longer T_middle to allow the RC waveform to settle within 5% or so.

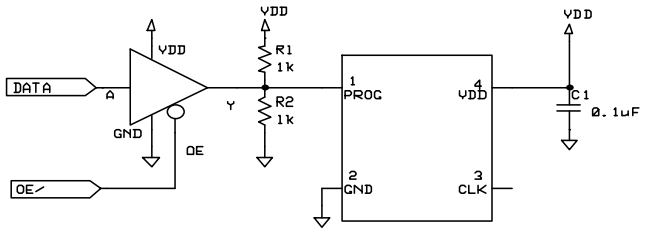


Figure 6. Circuit Diagram for Generating Tri-Level Signal with Tri-State Buffer

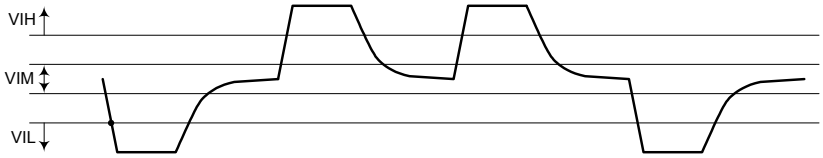


Figure 7. Tri-State Signal Generated with Tri-State Buffer

When using a tri-state buffer as shown above, care must be taken if the DATA and OE lines transition at the same time that there are no glitches. A glitch might occur, for example, if the OE line enables the output slightly before the data line has finished its logical transition. One way around this, albeit at the cost of some data overhead, is to use an extra OE cycle on every bit, as shown in Figure 8. Note that the diagram assumes an SN74LVC125, which has a low-true OE/ line (output is enabled when OE/ is low). For a high-true OE part, such as the SN74LVC126, the polarity of that signal would be reversed.

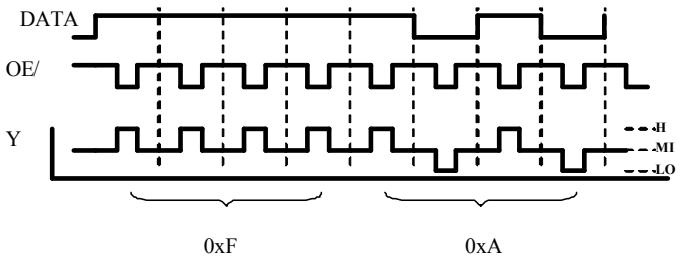


Figure 8. Signal Polarity

Programmable Drive Strength

The SiT3907 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the SiTime Applications Note section; http://www.sitime.com/support/application-notes.

EMI Reduction by Slowing Rise/Fall Time

Figure 9 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

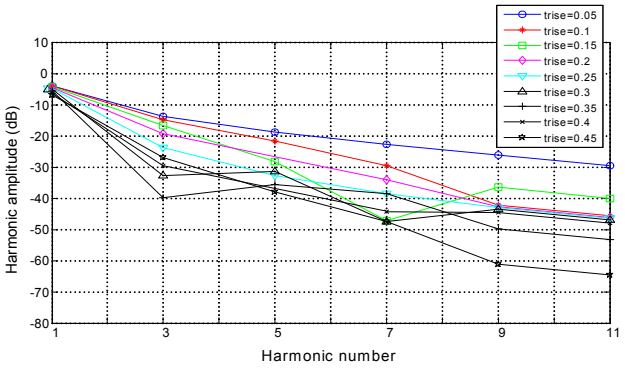


Figure 9. Harmonic EMI reduction as a Function of Slower Rise/Fall Time

Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to increase rise/fall time (edge rate) of the input clock. Some chipsets would require faster rise/fall time in order to reduce their sensitivity to this type of jitter. The SiT3907 provides up to 3 additional high drive strength settings for very fast rise/fall time. Refer to the Rise/Fall Time Tables to determine the proper drive strength.

High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3V SiT3907 device with default drive strength setting, the typical rise/fall time is 1.15ns for 15 pF output load. The typical rise/fall time slows down to 2.72ns when the output load increases to 45 pF. One can choose to speed up the rise/fall time to 1.41ns by then increasing the drive strength setting on the SiT3907.

The SiT3907 can support up to 60 pF or higher in maximum capacitive loads with up to 3 additional drive strength settings. Refer to the Rise/Tall Time Tables to determine the proper drive strength for the desired combination of output load vs. rise/fall time

SiT3907 Drive Strength Selection

Tables 1 through 5 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the SiT3907 nominal supply voltage (1.8V, 2.5V, 2.8V, 3.3V).
2. Select the capacitive load column that matches the application requirement (5 pF to 60 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

Calculating Maximum Frequency

Based on the rise and fall time data given in Tables 1 through 4, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature as follows:

$$\text{Max Frequency} = \frac{1}{3.5 \times \text{Trf_10/90}}$$

Where Trf_10/90 is the typical rise/fall time at 10% to 90% Vdd.

Example 1

Calculate f_{MAX} for the following condition:

- Vdd = 1.8V (Table 1)
- Capacitive Load: 30 pF
- Typical Tr/f time = 5 ns (rise/fall time part number code = G)

Rise/Fall Time (10% to 90%) vs C_{LOAD} Tables

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	12.45	17.68	19.48	46.21	57.82
A	6.50	10.27	16.21	23.92	30.73
R	4.38	7.05	11.61	16.17	20.83
B	3.27	5.30	8.89	12.18	15.75
S	2.62	4.25	7.20	9.81	12.65
D	2.19	3.52	6.00	8.31	10.59
T	1.76	3.01	5.14	7.10	9.15
E	1.59	2.59	4.49	6.25	7.98
U	1.49	2.28	3.96	5.55	7.15
F	1.22	2.10	3.57	5.00	6.46
W	1.07	1.88	3.23	4.50	5.87
G	1.01	1.64	2.95	4.12	5.40
X	0.96	1.50	2.74	3.80	4.98
K	0.92	1.41	2.56	3.52	4.64
Y	0.88	1.34	2.39	3.25	4.32
Q	0.86	1.29	2.24	3.04	4.06
Z or "-": Default	0.82	1.24	2.07	2.89	3.82
M	0.77	1.20	1.94	2.72	3.61
N	0.66	1.15	1.84	2.58	3.41
P	0.51	1.09	1.76	2.45	3.24

Table 3. Vdd = 1.8V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	8.68	13.59	18.36	32.70	42.06
A	4.42	7.18	11.93	16.60	21.38
R	2.93	4.78	8.15	11.19	14.59
B	2.21	3.57	6.19	8.55	11.04
S	1.67	2.87	4.94	6.85	8.80
D	1.50	2.33	4.11	5.68	7.33
T	1.06	2.04	3.50	4.84	6.26
E	0.98	1.69	3.03	4.20	5.51
U	0.93	1.48	2.69	3.73	4.92
F	0.90	1.37	2.44	3.34	4.42
W	0.87	1.29	2.21	3.04	4.02
G or "-": Default	0.67	1.20	2.00	2.79	3.69
X	0.44	1.10	1.86	2.56	3.43
K	0.38	0.99	1.76	2.37	3.18
Y	0.36	0.83	1.66	2.20	2.98
Q	0.34	0.71	1.58	2.07	2.80
Z	0.33	0.65	1.51	1.95	2.65
M	0.32	0.62	1.44	1.85	2.50
N	0.31	0.59	1.37	1.77	2.39
P	0.30	0.57	1.29	1.70	2.28

Table 4. Vdd = 2.5V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	7.93	12.69	17.94	30.10	38.89
A	4.06	6.66	11.04	15.31	19.80
R	2.68	4.40	7.53	10.29	13.37
B	2.00	3.25	5.66	7.84	10.11
S	1.59	2.57	4.54	6.27	8.07
D	1.19	2.14	3.76	5.21	6.72
T	1.00	1.79	3.20	4.43	5.77
E	0.94	1.51	2.78	3.84	5.06
U	0.90	1.38	2.48	3.40	4.50
F	0.87	1.29	2.21	3.03	4.05
W	0.62	1.19	1.99	2.76	3.68
G or "-": Default	0.41	1.08	1.84	2.52	3.36
X	0.37	0.96	1.72	2.33	3.15
K	0.35	0.78	1.63	2.15	2.92
Y	0.33	0.67	1.54	2.00	2.75
Q	0.32	0.63	1.46	1.89	2.57
Z	0.31	0.60	1.39	1.80	2.43
M	0.30	0.57	1.31	1.72	2.30
N	0.30	0.56	1.22	1.63	2.22
P	0.29	0.54	1.13	1.55	2.13

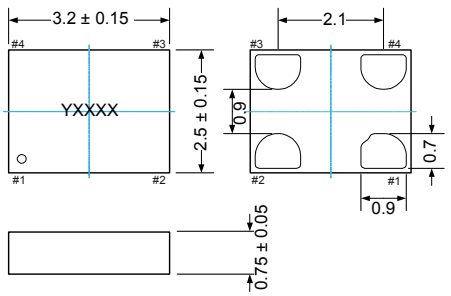
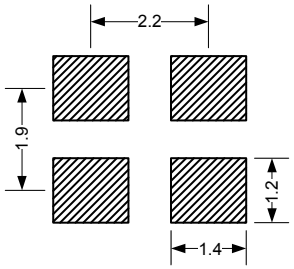
Table 5. Vdd = 2.8V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	7.18	11.59	17.24	27.57	35.57
A	3.61	6.02	10.19	13.98	18.10
R	2.31	3.95	6.88	9.42	12.24
B	1.65	2.92	5.12	7.10	9.17
S	1.43	2.26	4.09	5.66	7.34
D	1.01	1.91	3.38	4.69	6.14
T	0.94	1.51	2.86	3.97	5.25
E	0.90	1.36	2.50	3.46	4.58
U	0.86	1.25	2.21	3.03	4.07
F or "-": Default	0.48	1.15	1.95	2.72	3.65
W	0.38	1.04	1.77	2.47	3.31
G	0.36	0.87	1.66	2.23	3.03
X	0.34	0.70	1.56	2.04	2.80
K	0.33	0.63	1.48	1.89	2.61
Y	0.32	0.60	1.40	1.79	2.43
Q	0.32	0.58	1.31	1.69	2.28
Z	0.30	0.56	1.22	1.62	2.17
M	0.30	0.55	1.12	1.54	2.07
N	0.30	0.54	1.02	1.47	1.97
P	0.29	0.52	0.95	1.41	1.90

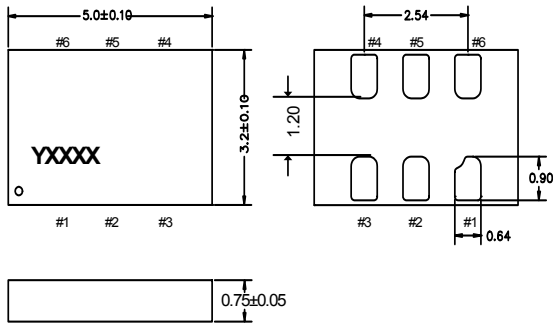
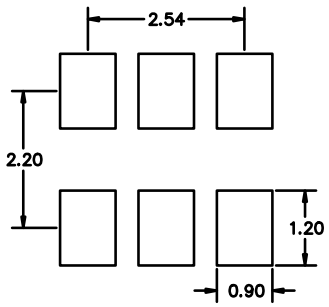
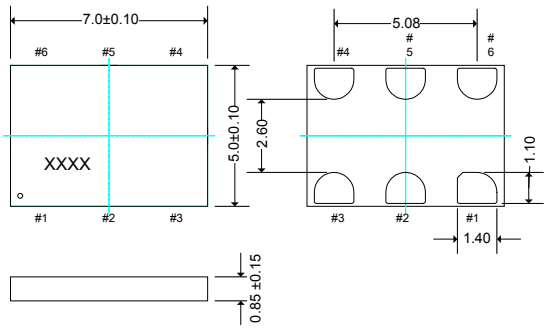
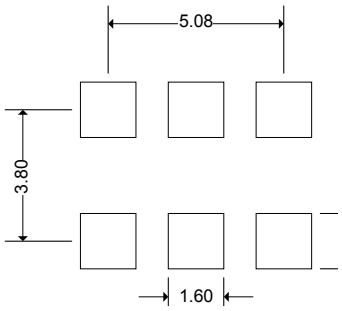
Table 6. Vdd = 3.3V Rise/Fall Times for Specific C_{LOAD}

Dimensions and Patterns

Packages (4-pin device)

Package Size – Dimensions (Unit: mm)[5]	Recommended Land Pattern (Unit: mm)[6]
3.2 x 2.5 x 0.75 mm 	

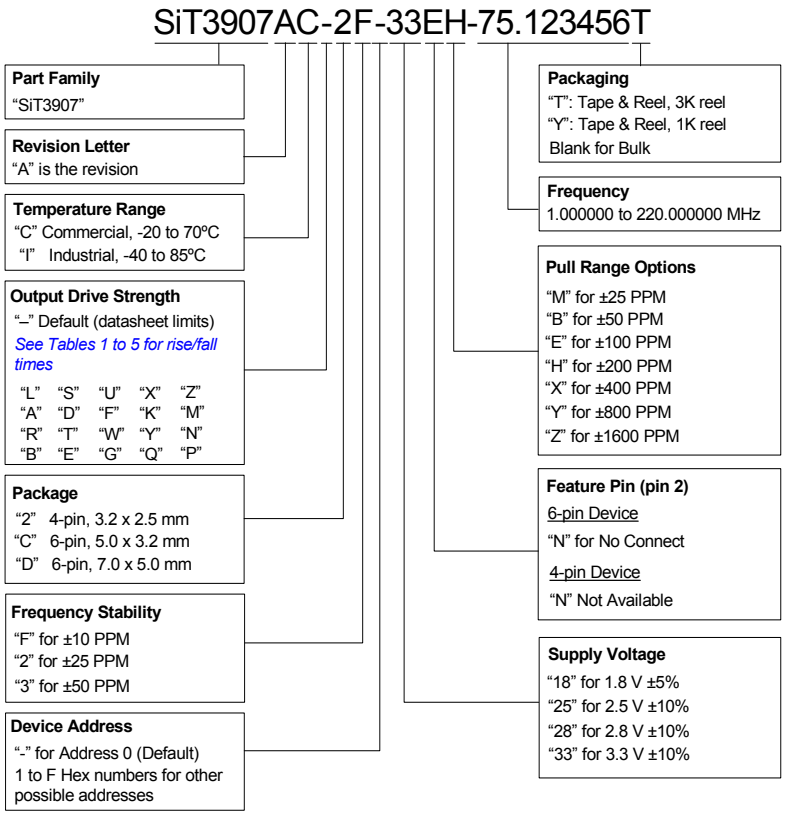
Packages (6-pin device)

Package Size – Dimensions (Unit: mm)[5]	Recommended Land Pattern (Unit: mm)[6]
5.0 x 3.2 x 0.75 mm 	
7.0 x 5.0 x 0.90 mm 	

Notes:

5. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
6. A capacitor of value 0.1 µF between Vdd and GND is recommended.

Ordering Information



APR Definition

Absolute pull range (APR) = Nominal pull range (PR) - frequency stability (F_stab) - Aging (F_aging)

APR Table

Nominal Pull Range	Frequency Stability		
	± 10	± 25	±50
	APR (PPM)		
± 25	± 10	—	—
± 50	± 35	± 20	—
± 100	± 85	± 70	± 45
± 200	± 185	± 170	± 145
± 400	± 385	± 370	± 345
± 800	± 785	± 770	± 745
± 1600	± 1585	± 1570	± 1545

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