Features

- ESD Protect for 4 high-speed I/O channels
- Provide ESD protection for each channel to
  IEC 61000-4-2 (ESD) ±30kV (air / contact)
  IEC 61000-4-5 (Lightning) 15A (8/20μs) for any I/O-to-GND
  IEC 61000-4-5 (Lightning) 30A (8/20μs) for VDD-to-GND
- For low operating voltage applications: 5V, 4.2V, 3.3V, 2.5V
- Low capacitance : 2pF typical
- Fast turn-on and Low clamping voltage
- Array of surge rated diodes with internal equivalent TVS diode
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green Part***
- ***AEC-Q101 qualified***

Applications

- Automotive Application
- USB2.0 Power and Data lines protection
- Notebook and PC Computers
- Monitors and Flat Panel Displays

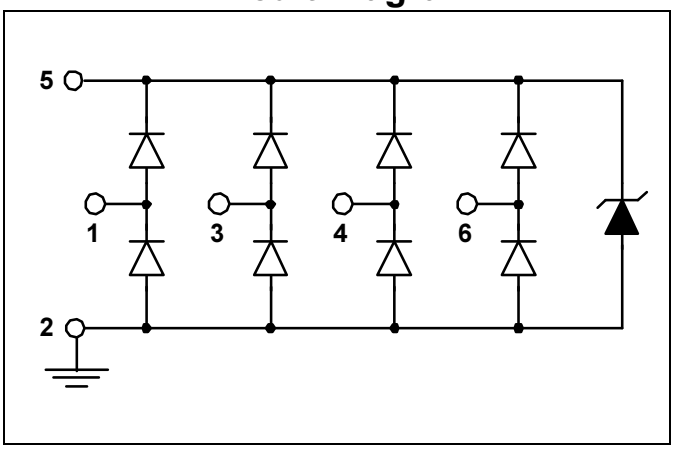
Description

AZ9115-04S is a high performance and low cost design which includes surge rated diode arrays to protect high speed data interfaces. The AZ9115-04S family has been specifically designed to protect sensitive components, which are connected to data and transmission lines, from over-voltage caused by Electrostatic Discharging (ESD) and Lightning.

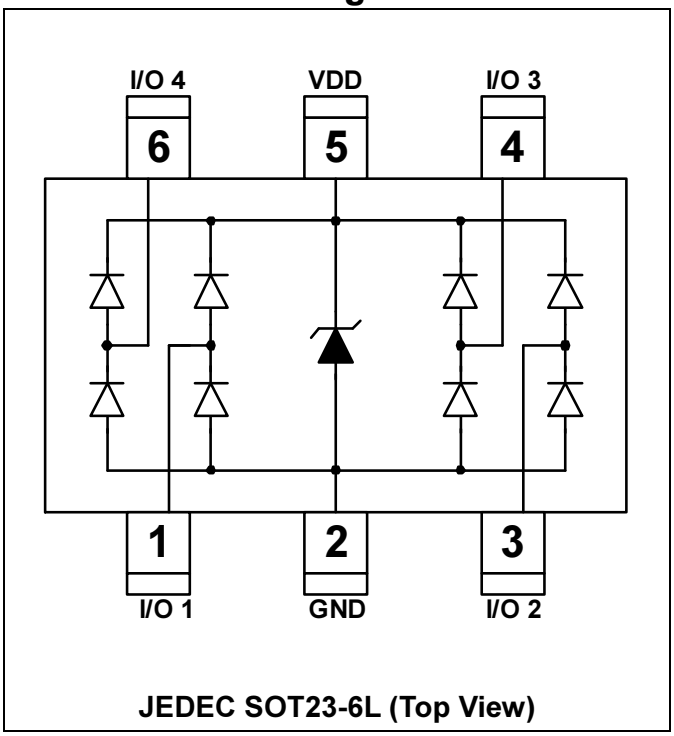
AZ9115-04S is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to the ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components.

AZ9115-04S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (± 15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



JEDEC SOT23-6L (Top View)

SPECIFICATIONS

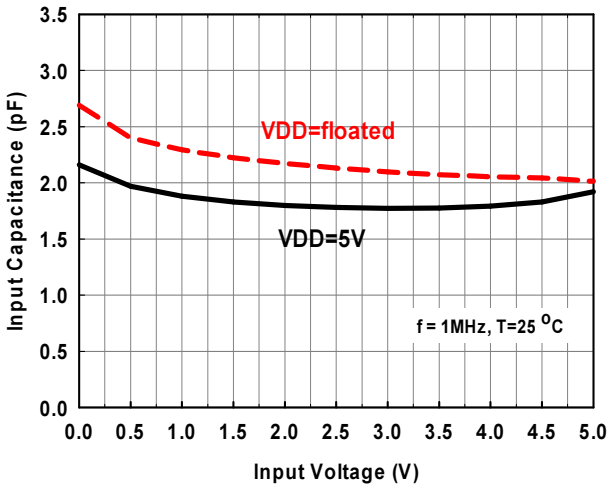
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**SYMBOL**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20μs, any I/O-to-GND)	I_{PP}	15	**A**
Peak Pulse Current (tp =8/20μs, VDD-to-GND)	I_{PP}	30	**A**
Operating Supply Voltage (VDD-GND)	V_{DC}	5.5	**V**
ESD per IEC 61000-4-2 (Air / Contact)	V_{ESD}	30	**kV**
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	**°C**
Operating Temperature	T_{OP}	-55 to +125	**°C**
Storage Temperature	T_{STO}	-55 to +150	**°C**
DC Voltage at any I/O pin	V_{IO}	(GND - 0.5) to 5.5	**V**

ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin 5 to pin 2, T=25 °C			5	**V**
Reverse Leakage Current	I_{Leak}	V_{RWM} = 5V, T=25 °C, Pin 5 to pin 2			5	**μA**
Channel Leakage Current	$I_{CH-Leak}$	V_{Pin5} = 5V, V_{Pin2} = 0V, T=25 °C			1	**μA**
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, Pin 5 to Pin 2	6		10	**V**
Forward Voltage	V_F	I_F = 15mA, T=25 °C, Pin 2 to Pin 5		0.8	1.2	**V**
ESD Clamping Voltage –I/O (Note 1)	V_{clamp_io}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), T=25 °C, Contact mode, any I/O pin to Ground		9		**V**
ESD Clamping Voltage –VDD (Note 1)	V_{clamp_VDD}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), T=25 °C, Contact mode, VDD pin to Ground		7		**V**
ESD Dynamic Turn on Resistance –I/O	$R_{dynamic_io}$	IEC 61000-4-2, 0~+8kV, T=25 °C, Contact mode, any I/O pin to Ground		0.13		Ω
ESD Dynamic Turn on Resistance –VDD	$R_{dynamic_VDD}$	IEC 61000-4-2, 0~+8kV, T=25 °C, Contact mode, VDD pin to Ground		0.05		Ω
Lightning Clamping Voltage	$V_{lightning_io}$	I_{PP}=15A, tp=8/20μs, T=25 °C Any Channel pin to Ground		9.5		**V**
Lightning Clamping Voltage	$V_{lightning_VDD}$	I_{PP}=30A, tp=8/20μs, T=25 °C VDD pin to Ground		10		**V**
Channel Input Capacitance -1	C_{IN-1}	**V_{pin5} =5V,** V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C, Any Channel pin to Ground		2.0	2.5	**pF**
Channel Input Capacitance - 2	C_{IN-2}	**V_{pin5}=floated**,V_{pin2}=0V,**V_{IN}=2.5V**,f=1MHz, T=25°C,Any Channel pin to Ground		2.4	3.0	**pF**

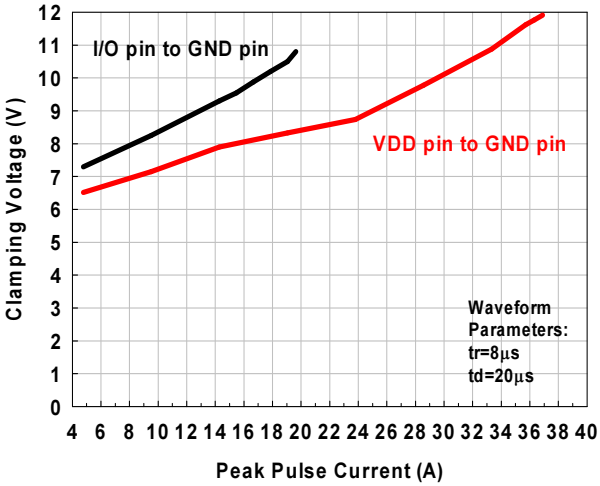
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics

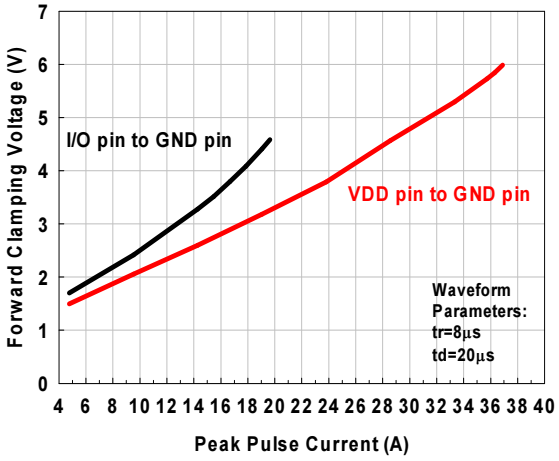
Typical Variation of C_{IN} vs. V_{IN}



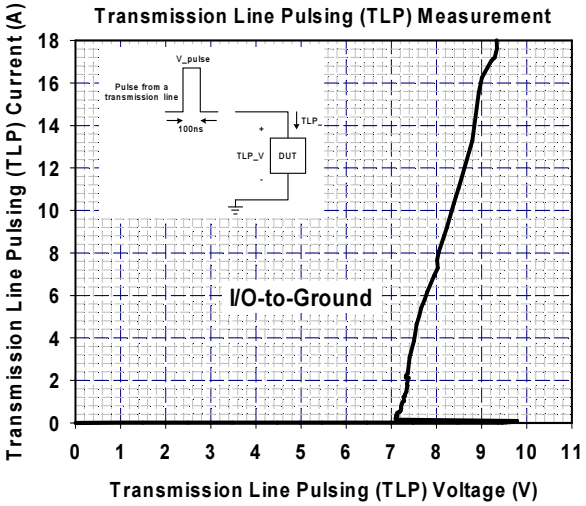
Clamping Voltage vs. Peak Pulse Current



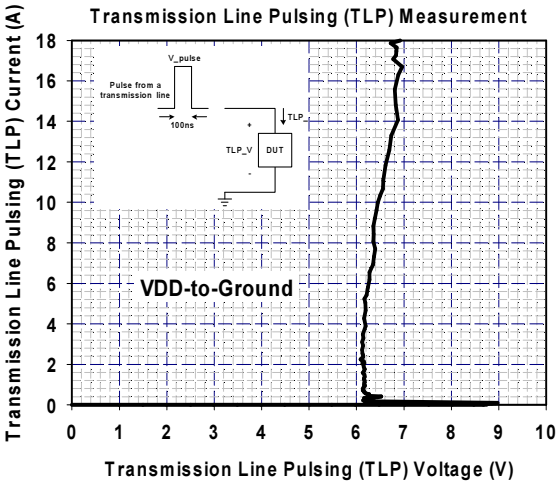
Forward Clamping Voltage vs. Peak Pulse Current



Transmission Line Pulsing (TLP) Measurement



Transmission Line Pulsing (TLP) Measurement



Applications Information

A. Design Considerations

The ESD protection scheme for system I/O connector is shown in the Fig. 1. In Fig. 1, the diodes D1 and D2 are general used to protect data line from ESD stress pulse. If the power-rail ESD clamping circuit is not placed between VDD and GND rails, the positive pulse ESD current (I_{ESD1}) will pass through the ESD current path1. Thus, the ESD clamping voltage V_{CL} of data line can be described as follow:

V_{CL} = Fwd voltage drop of D1 + supply voltage of VDD rail + $L_1 \times d(I_{ESD1})/dt + L_2 \times d(I_{ESD1})/dt$

Where L_1 is the parasitic inductance of data line, and L_2 is the parasitic inductance of VDD rail.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30A in 1ns. Here $d(I_{ESD1})/dt$ can be approximated by $\Delta I_{ESD1}/\Delta t$, or 30/(1x10-9). So just 10nH of total parasitic inductance (L_1 and L_2 combined) will lead to over 300V increment in V_{CL}! Besides, the ESD pulse current which is directed into the VDD rail may potentially damage any components that are attached to that rail. Moreover, it is common for the forward voltage drop of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. Of course, the discrete diode is also possible to be destroyed due to its power dissipation capability is exceeded.

The AZ9115-04S has an integrated power-rail ESD clamped circuit between VDD and GND rails. It can successfully overcome previous disadvantages. During an ESD event, the positive ESD pulse current (I_{ESD2}) will be directed through the integrated power-rail ESD clamped circuit to GND rail (ESD current path2). The clamping voltage V_{CL} on the data line is small and protected IC will not be damaged because power-rail ESD clamped circuit offer a low impedance path to discharge ESD pulse current.

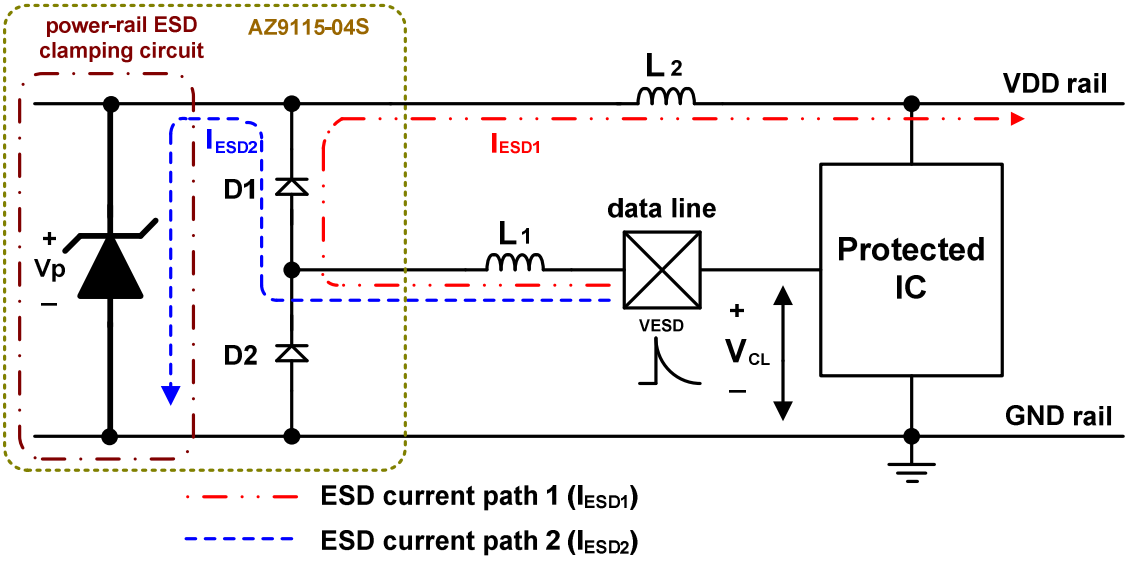


Fig. 1 Application of positive ESD pulse between data line and GND rail.

B. Device Connection

The AZ9115-04S is designed to protect four data lines and power rails from transient over-voltage (such as ESD stress pulse). The device connection of AZ9115-04S is shown in the Fig. 2. In Fig. 2, the four protected data lines are connected to the ESD protection pins (pin1, pin3, pin4, and pin6) of AZ9115-04S. The ground pin (pin2) of AZ9115-04S is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible. In addition, the power pin (pin 5) of AZ9115-04S is a positive reference pin. This pin should directly connect to the VDD rail of PCB., then the VDD rail also can be protected by the power-rail ESD clamped circuit (not shown) of AZ9115-04S.

AZ9115-04S can provide protection for 4 I/O signal lines simultaneously. If the number of I/O signal lines is less than 4, the unused I/O pins can be simply left as NC pins.

In some cases, systems are not allowed to be reset or restart after the ESD stress directly applying at the I/O-port connector. Under this situation, in order to enhance the sustainable ESD Level, a 0.1μF chip capacitor can be added between the VDD and GND rails. The place of this chip capacitor should be as close as possible to the AZ9115-04S.

In some cases, there isn't power rail presented on the PCB. Under this situation, the power pin (pin 5) of AZ9115-04S can be left as floated. The protection will not be affected, only the load capacitance of I/O pins will be slightly increased. Fig. 3 shows the detail connection.

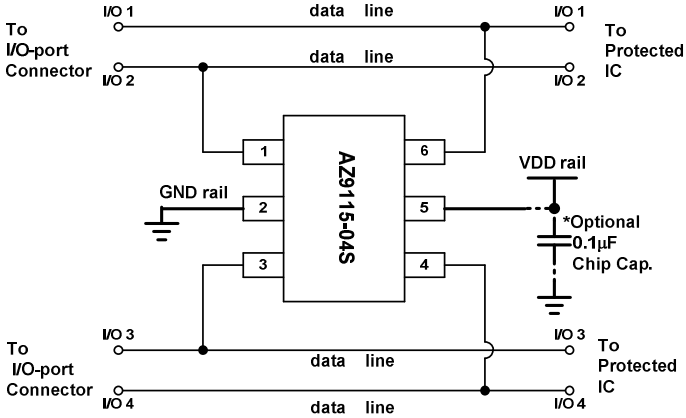


Fig. 2 Data lines and power rails connection of AZ9115-04S.

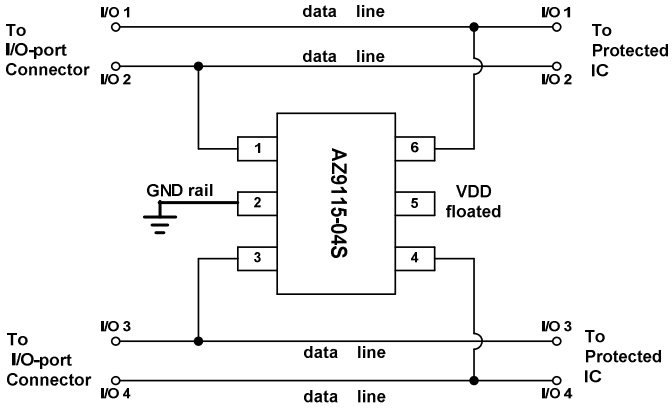


Fig. 3 Data lines and power rails connection of AZ9115-04S. VDD pin is left as floating when no power rail presented on the PCB.

C. Applications

1. Universal Serial Bus (USB) ESD Protection

The AZ9115-04S can be used to protect the USB port on the monitors, computers, peripherals or portable systems. The ESD protection scheme for dual USB ports is shown in Fig. 3. In the Fig.3, each device will protect up two USB ports. The voltage bus (V_{BUS}) of USB ports (port1 and port2) are connected to the power pin (pin 5) of AZ9115-04S. Each data line (D+/D-) of USB port is connected to the ESD protection pin of AZ9115-04S.

When ESD voltage pulse appears on the data line, the ESD pulse current will be conducted by AZ9115-04S away from the USB controller chip. In addition, the ESD pulse current also can be conducted by AZ9115-04S away from the USB controller chip when the ESD voltage pulse appears on the voltage bus (V_{BUS}) of USB port. Therefore, the data lines (D+/D-) and voltage bus (V_{BUS}) of two USB ports are complementally protected with an AZ9115-04S.

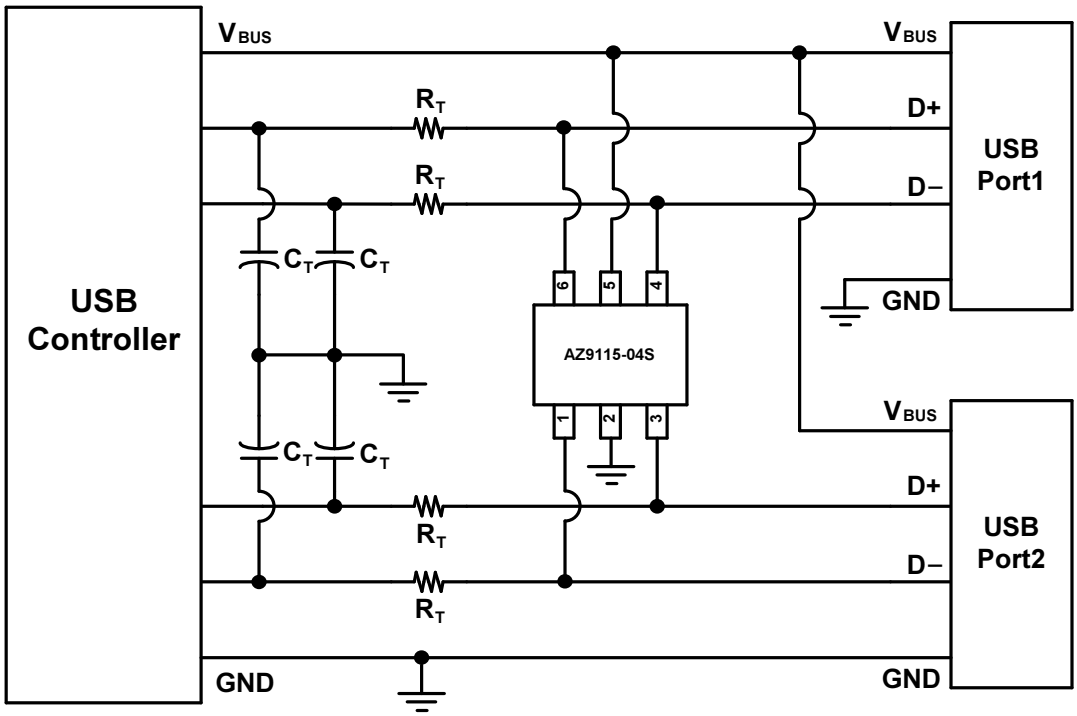


Fig. 3 ESD Protection scheme for dual USB ports by using AZ9115-04S.

2. Audio Interface ESD Protection

For the audio interface, the Right/Left channel and TMC terminals should be protected from the ESD stress. The AZ9115-04S can be used for the audio interface ESD protection. The ESD protection scheme for audio interface is shown in the Fig. 4. In the Fig. 4, the Right and Left channels of audio connector are connected to ESD protection pins (such as pin 1 and pin 6) of AZ9115-04S. In addition, the TMC terminals of audio connector are also connected to ESD protection pins (such as pin 3 and pin 4) of AZ9115-04S. For the power pin (pin 5) of AZ9115-04S, it should directly connect to the VDD power supply.

When ESD voltage pulse appears on the Right/Left channel or TMC terminals of audio connector, the ESD pulse current will be discharged by AZ9115-04S. Therefore, the Right/Left channel and TMC terminals of audio chip are complementally protected with an AZ9115-04S.

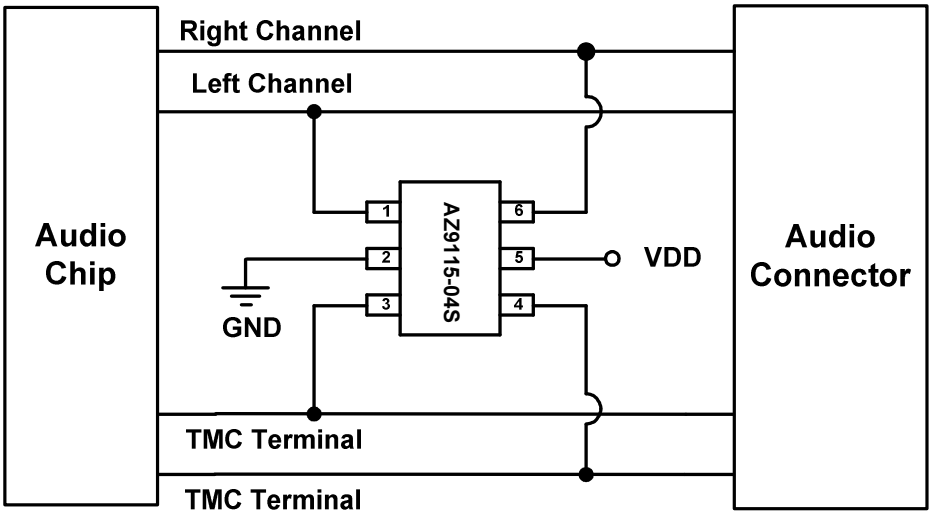


Fig. 4 ESD Protection scheme for audio interface by using AZ9115-04S.

3. Video (VGA) Interface ESD Protection

AZ9115-04S is designed for protecting high speed I/O ports from very high over-voltage caused by Electrostatic Discharging (ESD). Thus, a lot of kinds of high speed I/O ports can be the applications of AZ9115-04S, especially, the VGA and DVI ports with the ESD spec. of contact / air 30kV, Class-C above.

The VGA Input Port

The schematic of ESD protection design for a VGA input port on a display system is shown in Fig. 5. In most of VGA input circuit designs, there are always two power supplies, one is from the connector's DSUB-5V pin which potential comes from another VGA output port, the other is from the own power supply circuit of the VGA input port, system 5V. The VDD pin of AZ9115-04S is directly connected to the connector's DSUB-5V pin to block the ESD event which comes from the DSUB-5V pin.

The PCB layout example for the VGA Port

Fig. 6 shows the PCB layout example for a VGA port with two AZ9115-04S being used. In order to get good signal quality, in this PCB example, the signal traces for R, G, and B signals are with 0.4mm width and are accompanied with GND traces, respectively.

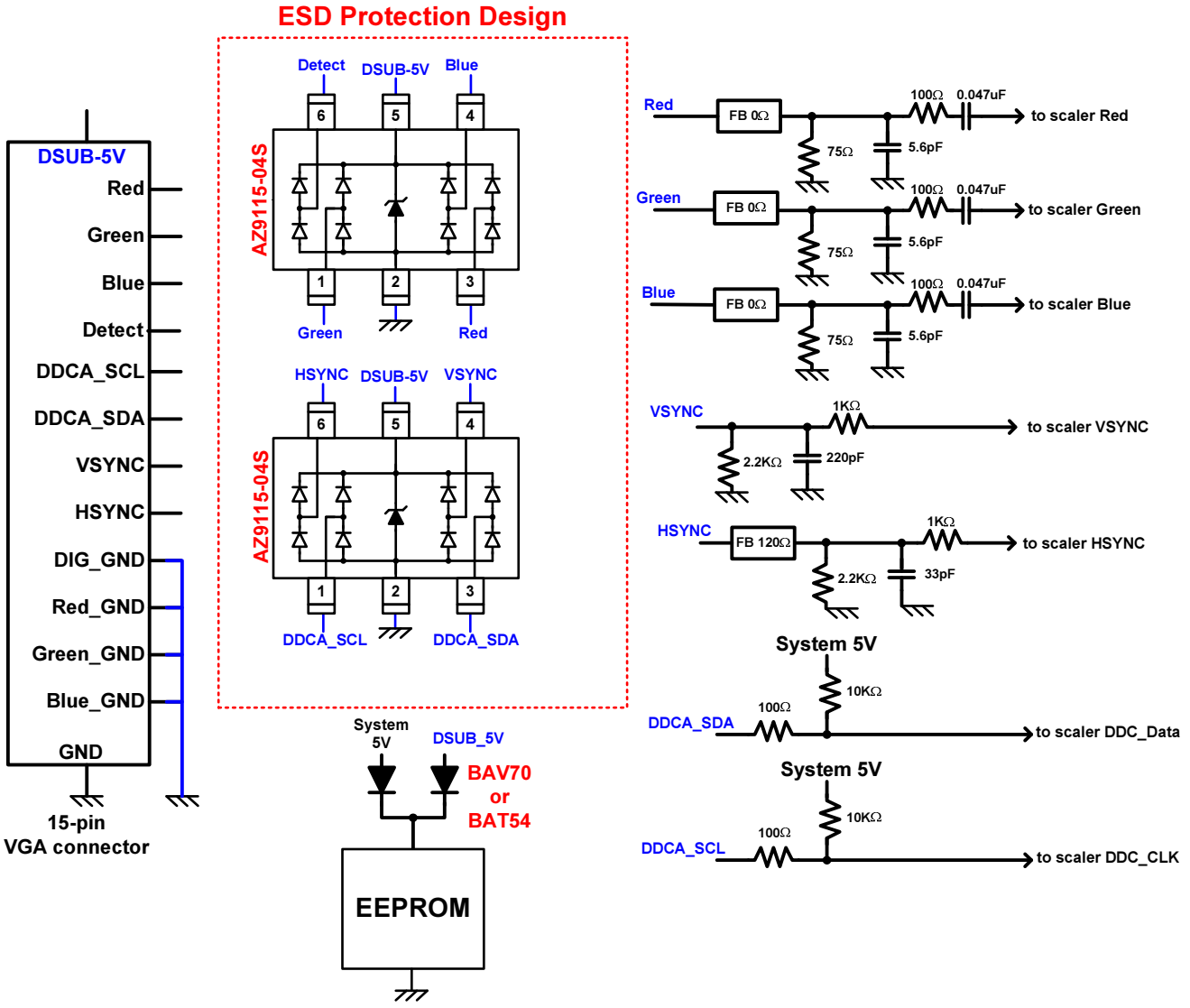


Fig. 5 The ESD design for a VGA *INPUT* port which two AZ9115-04S are used.

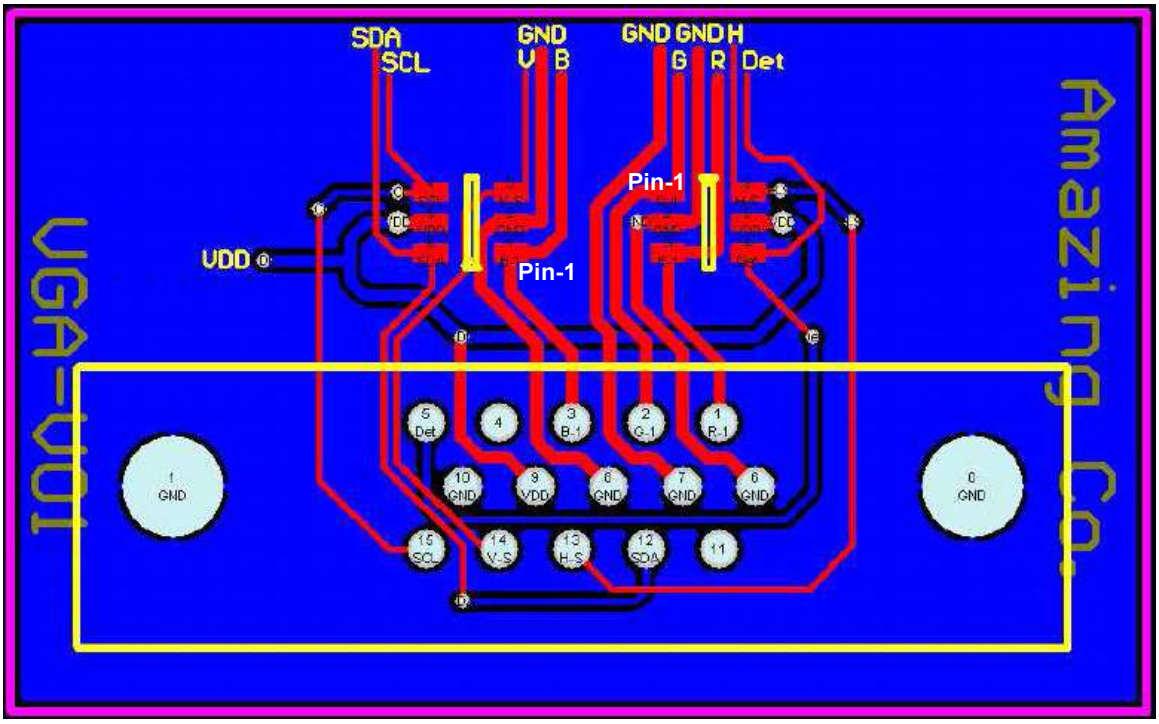


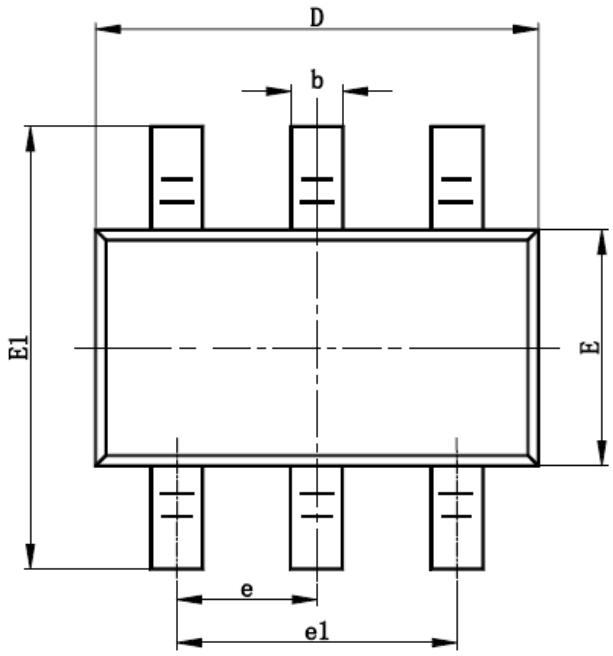
Fig. 6 The PCB layout example for a VGA port with two AZ9115-04S being used.

Mechanical Details

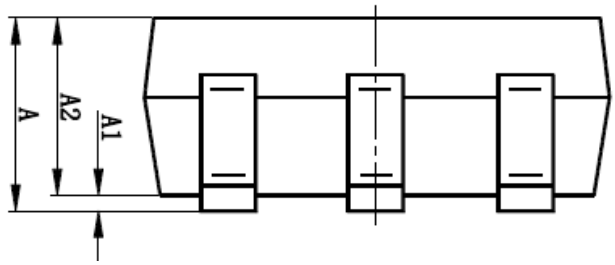
SOT23-6L

PACKAGE DIAGRAMS

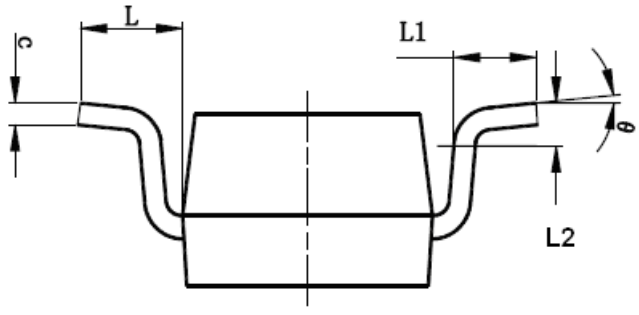
TOP VIEW



SIDE VIEW



END VIEW



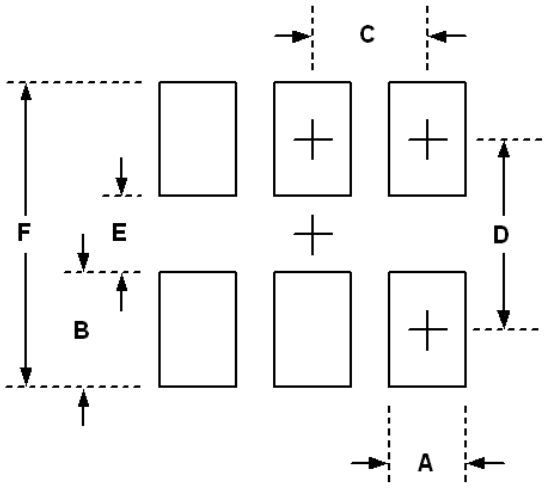
PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A		1.25		0.049
A1	0	0.15	0.000	0.006
A2	0.9	1.3	0.035	0.051
b	0.3	0.5	0.012	0.020
c	0.08	0.21	0.003	0.008
D	2.72	3.12	0.107	0.123
E	1.4	1.8	0.055	0.071
E1	2.6	3	0.102	0.118
e	0.95BSC		0.037BSC	
e1	1.9BSC		0.075BSC	
L1	0.3	0.6	0.012	0.024
L	0.7REF		0.028REF	
L2	0.25BSC		0.010BSC	
θ	0	8	0	8

Notes:

- This dimension complies with JEDEC outline standard MO-178 Variation AB.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- All dimensions are in millimeters, and the dimensions in inches are for reference only.
- 1mm = 40 mils = 0.04 inches.

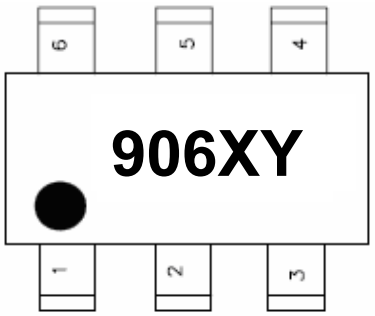
LAND LAYOUT



Dimensions		
Index	**Millimeter**	**Inches**
A	0.60	0.024
B	1.10	0.043
C	0.95	0.037
D	2.50	0.098
E	1.40	0.055
F	3.60	0.141

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



906 = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZ9115-04S (Green Part)	906XY

Note : Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ9115-04S.R7G	Green	T/R	7 inch	3,000/reel	4 reel=12,000/box	6 box=72,000/carton

Revision History

Revision	Modification Description
Revision 2015/11/06	Preliminary Release.
Revision 2016/06/24	Formal Release.

Unikeyic Electronics

Global Electronic Components Distributor

Click to view pricing, inventory, delivery, and lifecycle information:

Amazing Microelectronic:

AZ1023-04F AZ3133-04F AZ5013-01F AZ5123-01F.R7G AZ9113-04S AZ5125-01H.R7G AZ5825-01F.R7GR AZ9707-01F AZ9812-01F AZC199-02S.R7G AZ1023-02F AZ1065-06F.R7G AZ1143-04F.R7G AZ3133-08F AZ4514-01F AZ1043-08F AZ1045-04F.R7G AZ1045-08F AZ1065-06F AZ3105-01F AZ5725-01F.R7G AZ3028-04P AZ1015-02N AZ2015-05R AZC199-04S.R7G AZ1065-06Q AZ3125-08F AZ5123-01F.R7GR AZ5725-01F AZ3205-01F