General Description

The TS321ILT brings performance and economy to low power systems. With a high unity gain frequency and a guaranteed 0.4V/μs slew rate, the quiescent current is only 430μA/amplifier (5V).

The input common mode range in cludes ground and therefore the device is able to operate in single supply ap -plications as well as in dual supply applica tions. It is also capable of comfortably driving large capaci tive loads.

The TS321ILT is available in the SOT23-5 package . Overall the TS321ILT is a low power , wide supply range performance op amp that can be designed into a wide range of applications at an economical price without sacri -ficing valuable board space.

Features

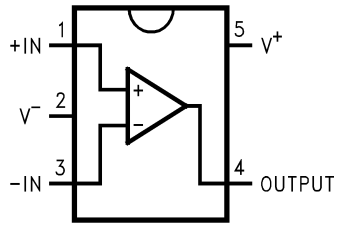
(V_{CC} = 5V, T_A = 25°C. Typical values unless specified).

- Gain-Bandwidth product 1MHz
- Low supply current 430μA
- Low input bias current 45nA
- Wide supply voltage range +3V to +32V
- Stable with high capacitive loads

Applications

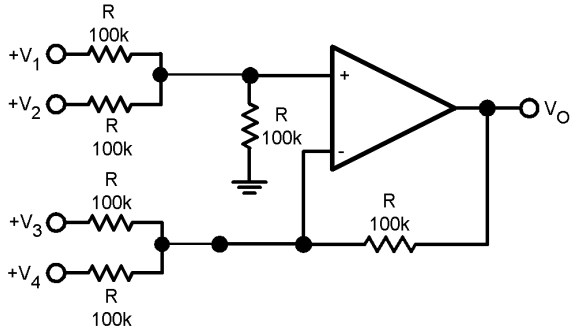
- Chargers
- Power supplies
- Industrial: controls, instruments
- Desktops
- Communications infrastructure

Reference News

Pinning and Package	Marking
 Top View **SOT-23-5**	A63A

Application Circuit

DC Summing Amplifier
($V_{IN's} \geq 0\ V_{DC}$ and $V_O \geq V_{DC}$)



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Where: $V_0 = V_1 + V_2 - V_3 - V_4$, $(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

Absolute Maximum Ratings (Note 1)

Differential Input Voltage	±Supply Voltage
Input Current (V_{IN} < −0.3V) (Note 6)	50mA
Supply Voltage (V^+ - V^-)	32V
Input Voltage	−0.3V to +32V
Output Short Circuit to GND, $V^+ \leq 15V$ and $T_A = 25^\circ C$ (Note 2)	Continuous
Storage Temperature Range	−65˚C to 150˚C
Junction Temperature (Note 3)	150˚C
Mounting Temperature	
Lead Temp (Soldering, 10 sec)	260˚C
Infrared (10 sec)	215˚C
Thermal Resistance to Ambient (θ_{JA})	265˚C/W
ESD Tolerance (Note 10)	300V

Operating Ratings (Note 1)

Temperature Range	−25˚C to 85˚C
Supply Voltage	3V to 30V

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at $T_A = 25^\circ C$; $V^+ = 5V$, $V^- = 0V$, $V_O = 1.4V$. **Boldface** limits apply at temperature extremes.

Symbol	Parameter		Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{OS}	Input Offset Voltage		(Note 7)		2	7 **9**	mV
I_{OS}	Input Offset Current				5	50 **150**	nA
I_B	Input Bias Current (Note 8)				45	250 **500**	nA
V_{CM}	Input Common-Mode Voltage Range		$V^+ = 30V$ (Note 9) For CMRR > = 50dB	0		$V^+ - 1.5$ **$V^+ - 2$**	V
A_V	Large Signal Voltage Gain		($V^+ = 15V$, $R_L = 2k\Omega$ $V_O = 1.4V$ to 11.4V)	25 **15**	100		V/mV
PSRR	Power Supply Rejection Ratio		$R_S \leq 10k\Omega$, $V^+ \leq 5V$ to 30V	65	100		dB
CMRR	Common Mode Rejection Ratio		$R_S \leq 10k\Omega$	65	85		dB
V_O	Output Swing	V_{OH}	$V^+ = 30V$, $R_L = 2k\Omega$	**26**			V
			$V^+ = 30V$, $R_L = 10k\Omega$	**27**	**28**		
		V_{OL}	$V^+ = 5V$, $R_L = 10k\Omega$		**5**	**20**	mV
I_S	Supply Current, No Load		$V^+ = 5V$		0.430 **0.7**	1.15 **1.2**	mA
			$V^+ = 30V$		0.660 **1.5**	2.85 **3**	
I_{SOURCE}	Output Current Sourcing		$V_{ID} = +1V$, $V^+ = 15V$, $V_O = 2V$	20 **10**	40 **20**		mA
I_{SINK}	Output Current Sinking		$V_{ID} = -1V$ $V^+ = 15V$, $V_O = 2V$	10 **5**	20 **8**		mA
			$V_{ID} = -1V$ $V^+ = 15V$, $V_O = 0.2V$	12	100		µA
I_O	Output Short Circuit to Ground (Note 2)		$V^+ = 15V$		40	85	mA
SR	Slew Rate		$V^+ = 15V$, $R_L = 2k\Omega$, $V_{IN} = 0.5$ to 3V $C_L = 100pF$, Unity Gain		0.4		V/µs
GBW	Gain Bandwidth Product		$V^+ = 30V$, f = 100kHz, $V_{IN} = 10mV$, $R_L = 2k\Omega$, $C_L = 100pF$		1		MHz
ϕm	Phase Margin				60		deg

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_A = 25°C; V^+ = 5V, V^- = 0V, V_O = 1.4V. **Boldface** limits apply at temperature extremes. (Continued)

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
THD	Total Harmonic Distortion	f = 1kHz, A_V = 20dB R_L = 2kΩ, V_O = $2V_{PP}$, C_L = 100pF, V^+ = 30V		0.015		%
e_n	Equivalent Input Noise Voltage	f = 1kHz, R_S = 100Ω V^+ = 30V		40		nV/ $\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Short circuits from the output V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground the maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 4: Typical values represent the most likely parametric norm.

Note 5: All limits are guaranteed by testing or statistical analysis.

Note 6: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.36V (at 25°C).

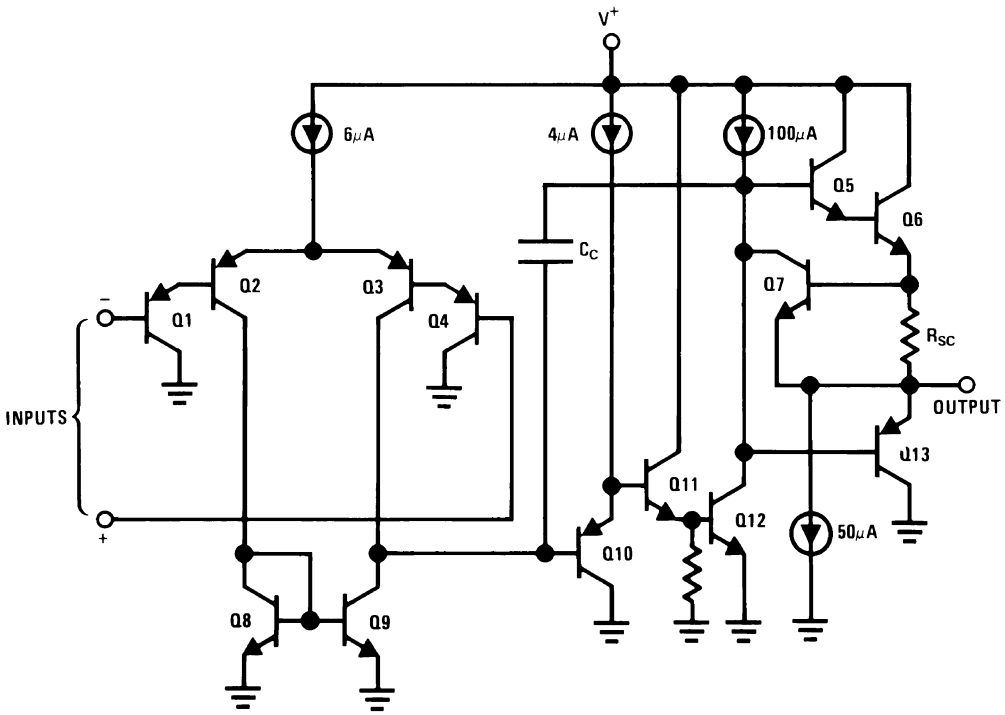
Note 7: $V_O \cong$ 1.4V, R_S = 0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V_+ - 1.5V) at 25°C.

Note 8: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 9: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V+ - 1.5V at 25°C, but either or both inputs can go to +32V without damage, independent of the magnitude of V+.

Note 10: Human Body Model, 1.5kΩ in series with 100pF.

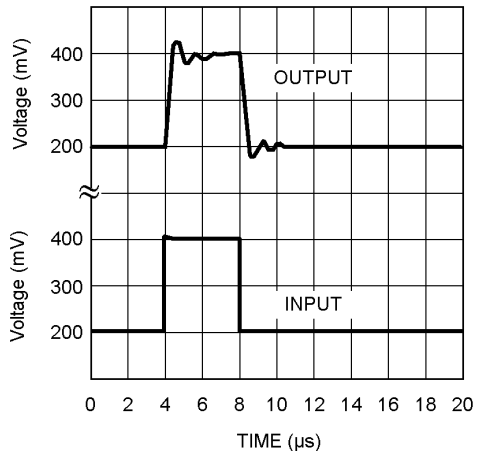
Simplified Schematic



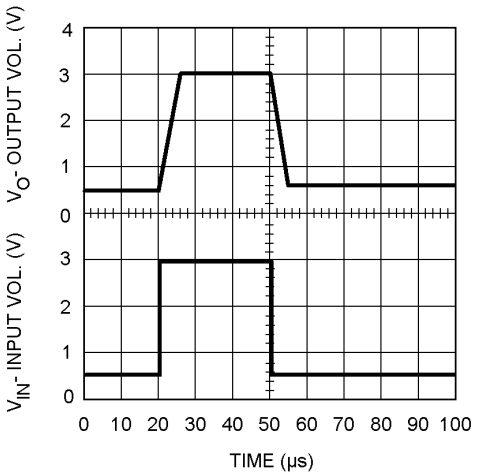
Typical Performance Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C.

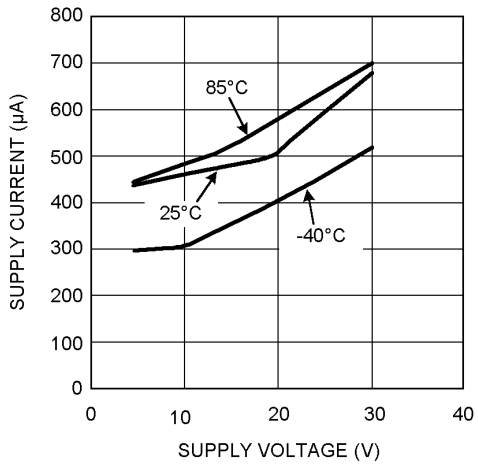
Small Signal Pulse Response



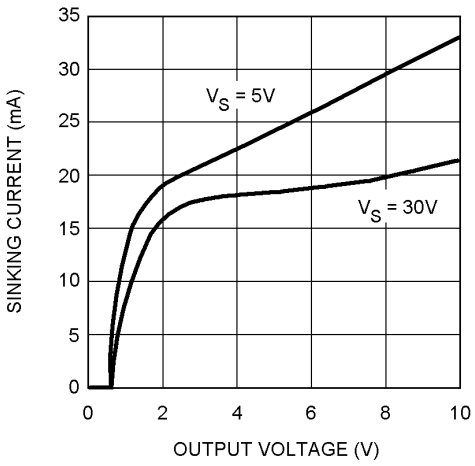
Large Signal Pulse Response



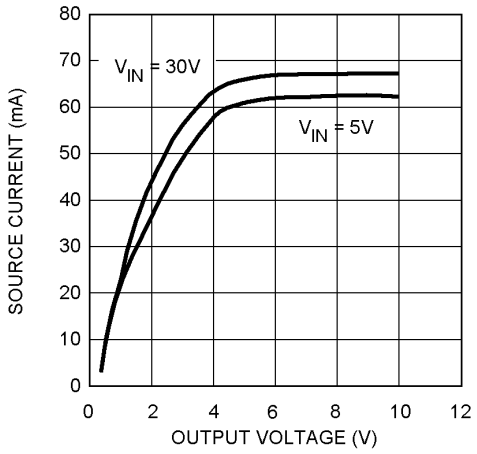
Supply Current vs. Supply Voltage



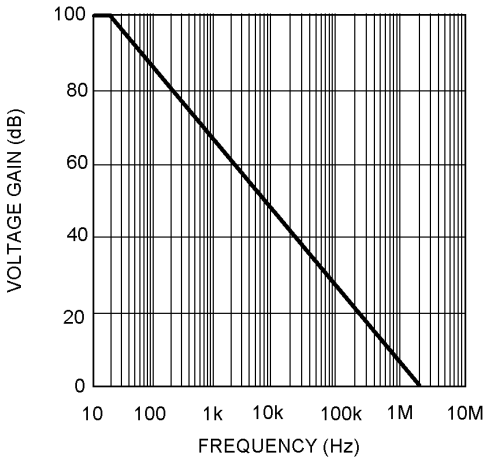
Sinking Current vs. Output Voltage



Source Current vs. Output Voltage



Open Loop Frequency Response



Application Hints

The TS321ILT opamp can operate with a single or dual power supply voltage, has true-differential inputs,and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. This amplifier operates over a wide range of power supply voltages, with little change in performance characteristics. At 25˚C amplifier operation is possible down to a minimum supply voltage of 3V.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25˚C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifier has a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For AC applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and to reduce distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if large load capacitance must be driven by the amplifier.

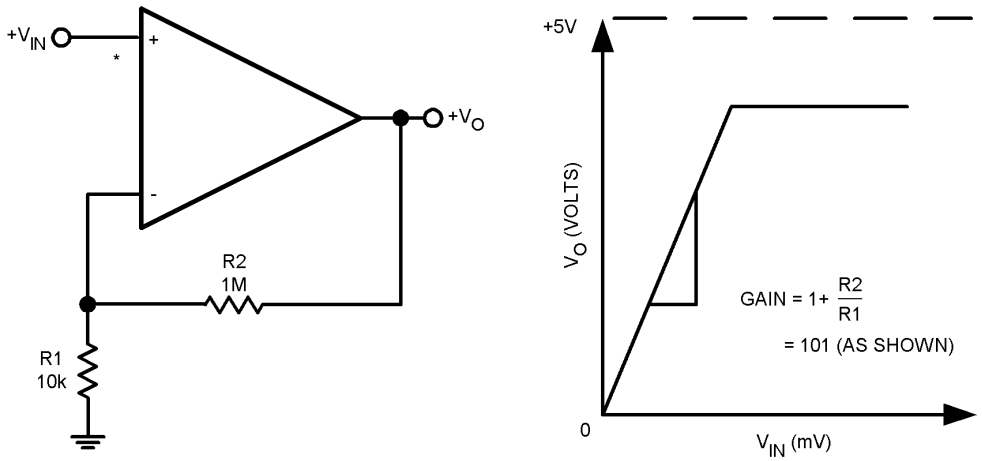
The bias network of the TS321ILT establishes a supply current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. The larger value of output source current which is available at 25˚C provides a larger output current capability at elevated temperatures than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Applications

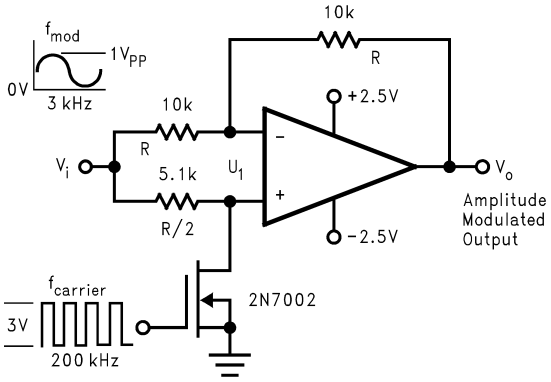
Non-Inverting DC Gain (0V Input = 0V Output)



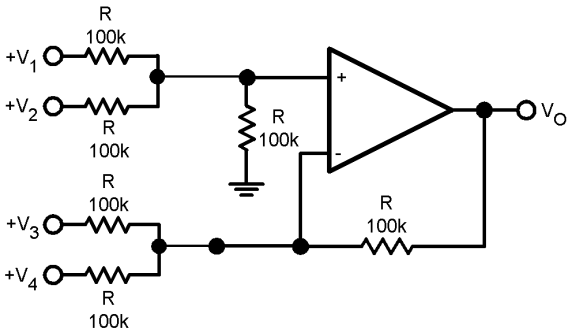
* R NOT NEEDED DUE TO TEMPERATURE INDEPENDENT I_{IN}

Typical Applications (Continued)

Amplitude Modulator Circuit

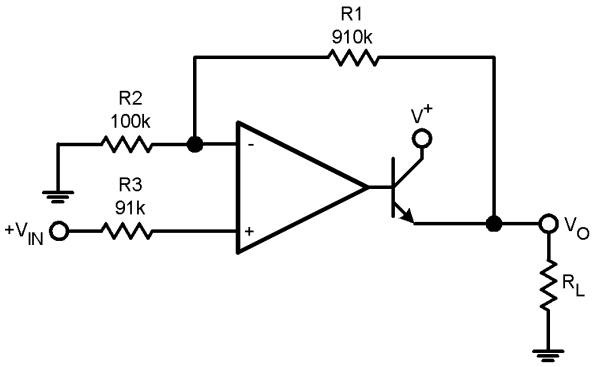


DC Summing Amplifier
($V_{IN's} \geq 0\ V_{DC}$ and $V_O \geq V_{DC}$)



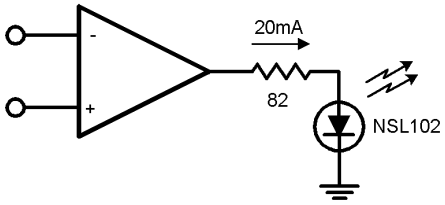
Where: $V_0 = V_1 + V_2 - V_3 - V_4$, $(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

Power Amplifier

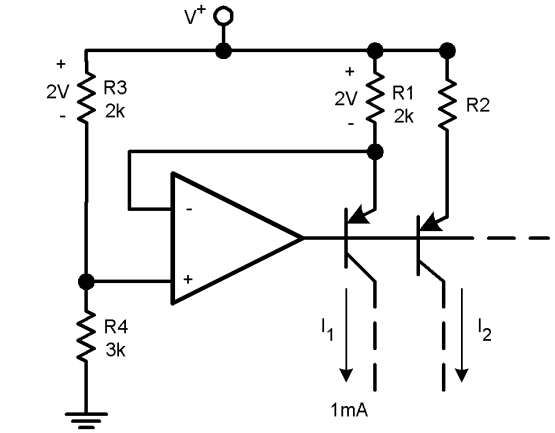


$V_0 = 0\ V_{DC}$ for $V_{IN} = 0\ V_{DC}$, $A_V = 10$

LED Driver

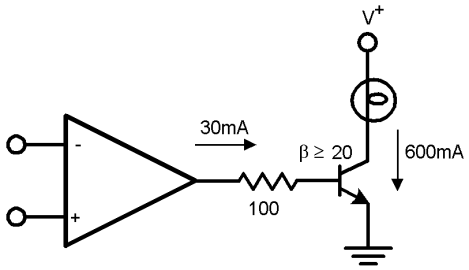


Fixed Current Sources



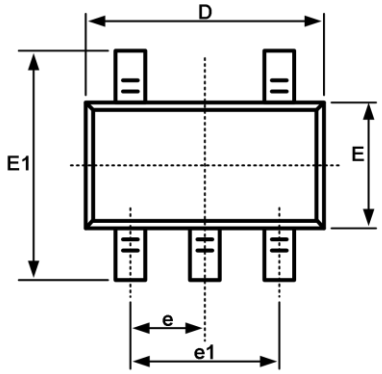
$$I_2 = \left[\frac{R1}{R2}\right] I_1$$

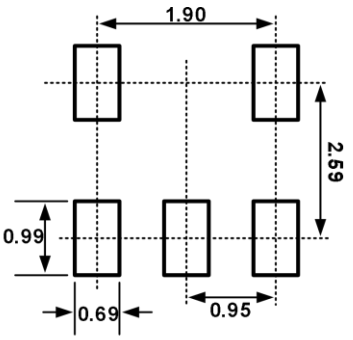
Lamp Driver



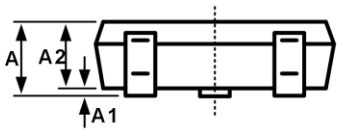
Package Outline

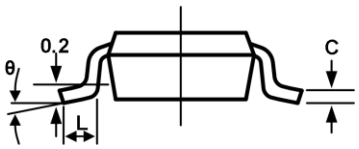
SOT23-5





Recommended Land Pattern (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950BSC		0.037BSC	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600REF		0.024REF	
θ	0°	8°	0°	8°