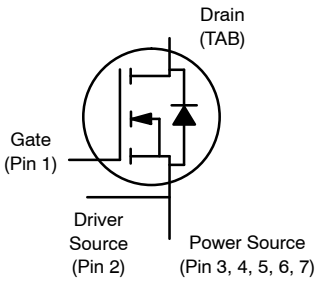
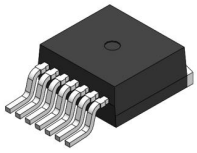
Silicon Carbide (SiC) MOSFET – 60 mohm, 900 V, M2, D2PAK-7L

NVBG060N090SC1

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
900 V	84 mΩ @ 15 V	44 A



N−CHANNEL MOSFET



D2PAK−7L
CASE 418BJ

Features

- Typ. $R_{DS(on)}$ = 60 mΩ @ V_{GS} = 15 V
- Typ. $R_{DS(on)}$ = 43 mΩ @ V_{GS} = 18 V
- Ultra Low Gate Charge ($Q_{G(tot)}$ = 88 nC)
- High Speed Switching with Low Capacitance (C_{oss} = 115 pF)
- 100% Avalanche Tested
- T_J = 175°C
- AEC−Q101 Qualified and PPAP Capable
- This Device is Halide Free and RoHS Compliant with exemption 7a, Pb−Free 2LI (on second level interconnection)

Typical Applications

- Automotive On Board Charger
- Automotive DC-DC converter for EV/HEV

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	900	V
Gate−to−Source Voltage			V_{GS}	+22/−8	V
Recommended Operation Values of Gate−to−Source		T_C < 175°C	V_{GSop}	+15/−5	V
Continuous Drain Current (Note 2)	Steady State	T_C = 25°C	I_D	44	A
Power Dissipation (Note 2)			P_D	211	W
Continuous Drain Current (Notes 1, 2)	Steady State	T_A = 25°C	I_D	5.8	A
Power Dissipation (Notes 1, 2)			P_D	3.6	W
Pulsed Drain Current (Note 3)	T_A = 25°C		I_{DM}	176	A
Single Pulse Surge Drain Current Capability (Note 4)	T_A = 25°C, t_p = 10 μs, R_G = 4.7 Ω		I_{DSC}	320	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	21	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 18 A, L = 1 mH) (Note 5)			E_{AS}	162	mJ
Maximum Lead Temperature for Soldering (1/8″ from case for 5 s)			T_L	245	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on a FR−4 board using1 in^2 pad of 2 oz copper.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. Repetitive rating, limited by max junction temperature.
4. Peak current might be limited by transconductance.
5. EAS of 162 mJ is based on starting T_J = 25°C; L = 1 mH, I_{AS} = 18 A, V_{DD} = 100 V, V_{GS} = 15 V.

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Traceability
NVBG060N090SC1 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NVBG060N090SC1	D2PAK−7L	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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Table 1. THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Case − Steady State (Note 2)	$R_{\theta JC}$	0.70	°C/W
Junction−to−Ambient − Steady State (Notes 1, 2)	$R_{\theta JA}$	41	

Table 2. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA		900			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 1 mA, referenced to 25°C			502		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 900 V	T_J = 25°C			100	μA
			T_J = 175°C			250	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = +22/−8 V, V_{DS} = 0 V				±1	μA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 5 mA		1.8	2.7	4.3	V
Recommended Gate Voltage	V_{GOP}			−5		+15	V
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 15 V, I_D = 20 A, T_J = 25°C			60	84	mΩ
		V_{GS} = 18 V, I_D = 20 A, T_J = 25°C			43		
		V_{GS} = 15 V, I_D = 20 A, T_J = 175°C			76	135	
Forward Transconductance	g_{FS}	V_{DS} = 20 V, I_D = 20 A			16		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 450 V			1800		pF
Output Capacitance	C_{OSS}				115		
Reverse Transfer Capacitance	C_{RSS}				12		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −5/15 V, V_{DS} = 720 V, I_D = 10 A			88		nC
Threshold Gate Charge	$Q_{G(TH)}$				16		
Gate−to−Source Charge	Q_{GS}				27		
Gate−to−Drain Charge	Q_{GD}				28		
Gate−Resistance	R_G	f = 1 MHz			3.0		Ω
SWITCHING CHARACTERISTICS, VGS = 10 V							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = −5/15 V, V_{DS} = 720 V, I_D = 20 A, R_G = 2.5 Ω Inductive load			24	40	ns
Rise Time	t_r				23	66	
Turn−Off Delay Time	$t_{d(OFF)}$				35	74	
Fall Time	t_f				11	20	
Turn−On Switching Loss	E_{ON}				410		μJ
Turn−Off Switching Loss	E_{OFF}				19		
Total Switching Loss	E_{tot}				429		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Continuous Drain−Source Diode Forward Current	I_{SD}	V_{GS} = −5 V, T_J = 25°C				21	A
Pulsed Drain−Source Diode Forward Current (Note 3)	I_{SDM}					176	
Forward Diode Voltage	V_{SD}	V_{GS} = −5 V, I_{SD} = 10 A, T_J = 25°C			3.9		V

Table 2. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS (continued)						
Reverse Recovery Time	t_{RR}	V_{GS} = −5/15 V, I_{SD} = 30 A, dI_S/dt = 1000 A/μs, V_{DS} = 720 V		18		ns
Reverse Recovery Charge	Q_{RR}			80		nC
Reverse Recovery Energy	E_{REC}			1.0		μJ
Peak Reverse Recovery Current	I_{RRM}			9.0		A
Charge Time	t_a			10		ns
Discharge Time	t_b			8.0		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

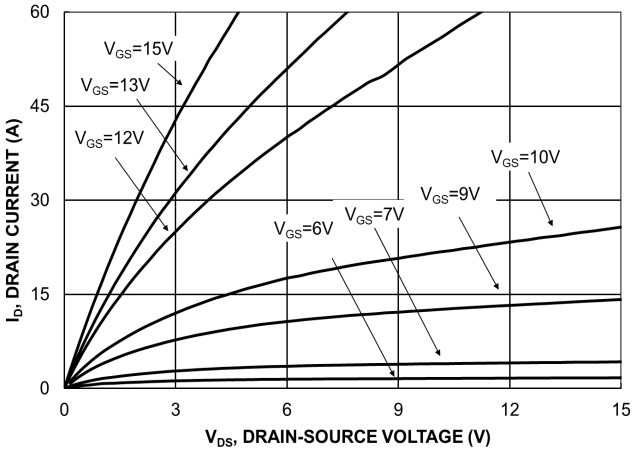


Figure 1. On−Region Characteristics

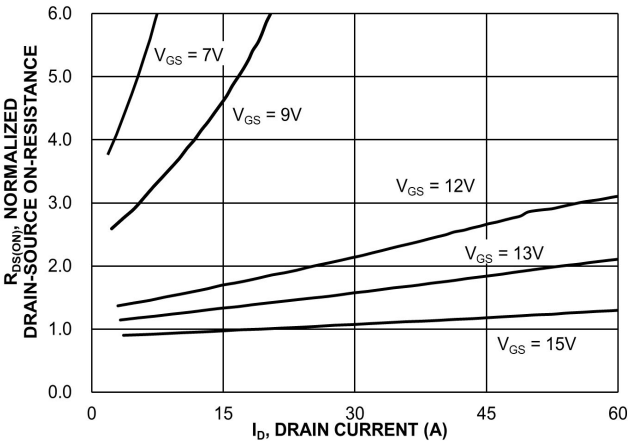


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

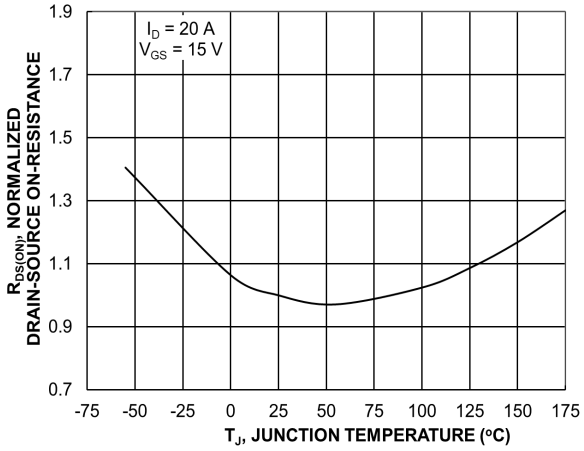


Figure 3. On−Resistance Variation with Temperature

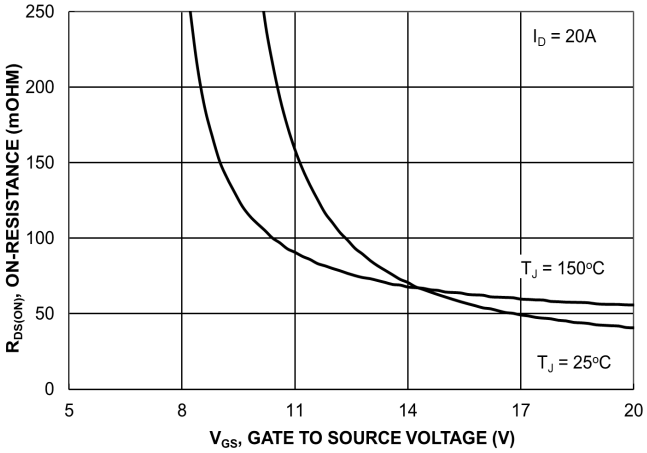


Figure 4. On−Resistance vs. Gate−to−Source Voltage

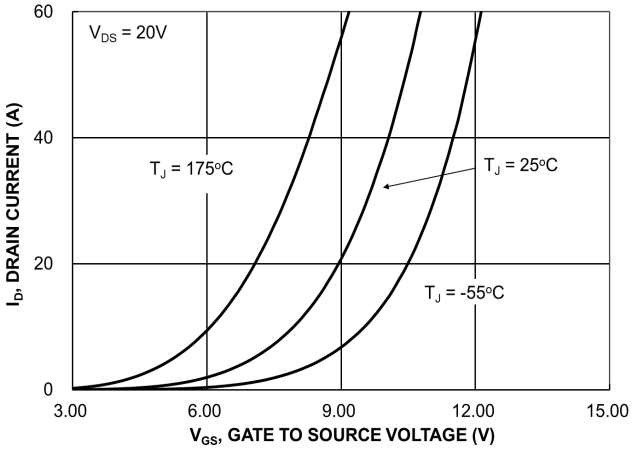


Figure 5. Transfer Characteristics

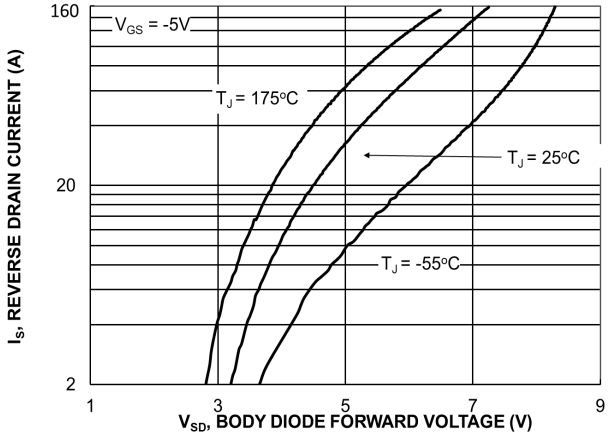


Figure 6. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS (continued)

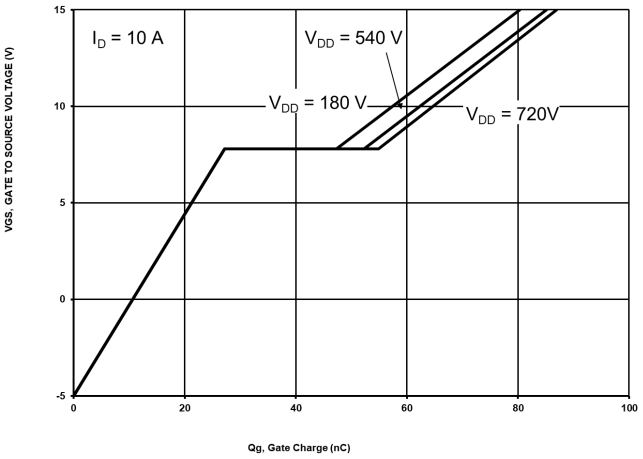


Figure 7. Gate−to−Source Voltage vs. Total Charge

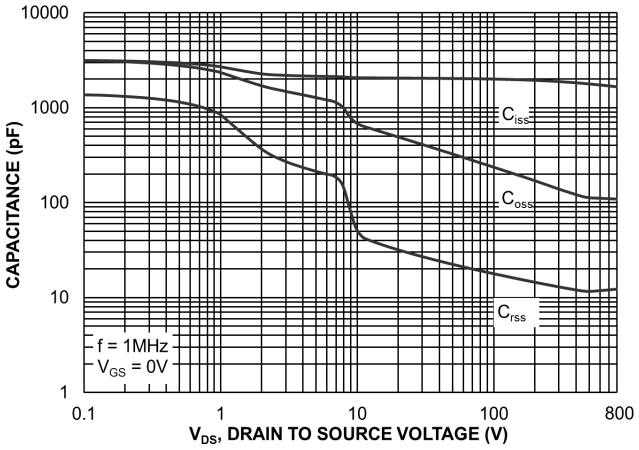


Figure 8. Capacitance vs. Drain−to−Source Voltage

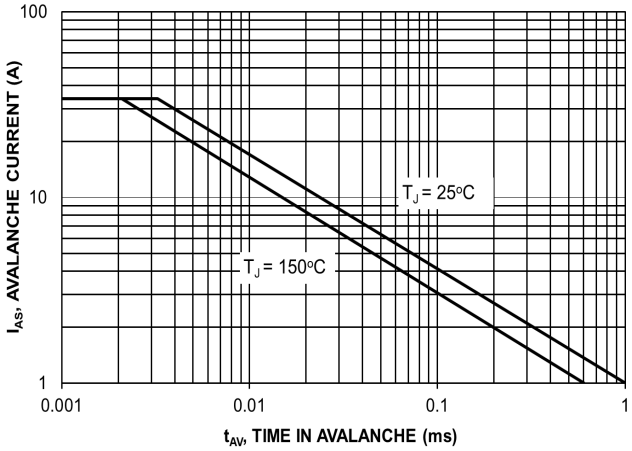


Figure 9. Unclamped Inductive Switching Capability

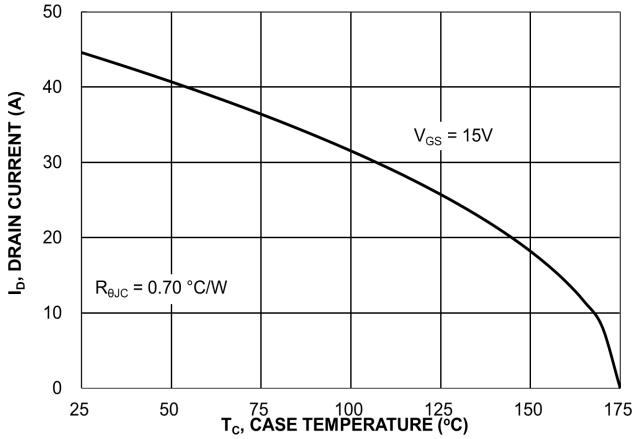


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

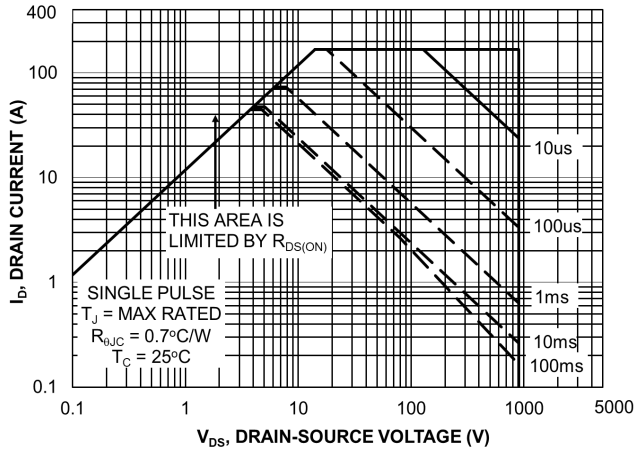


Figure 11. Maximum Rated Forward Biased Safe Operating Area

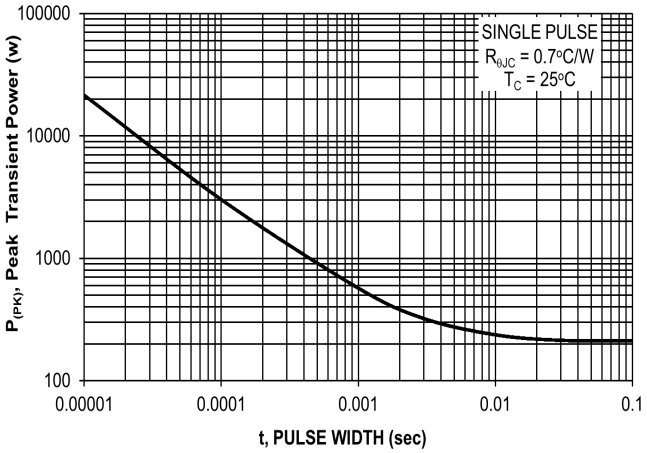


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

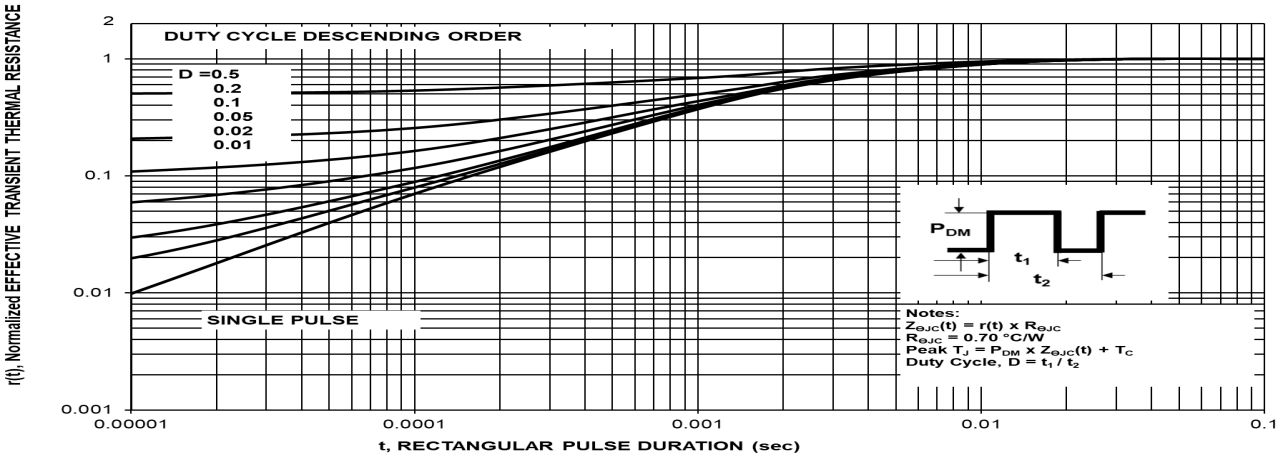
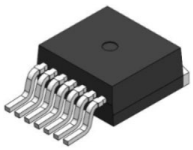
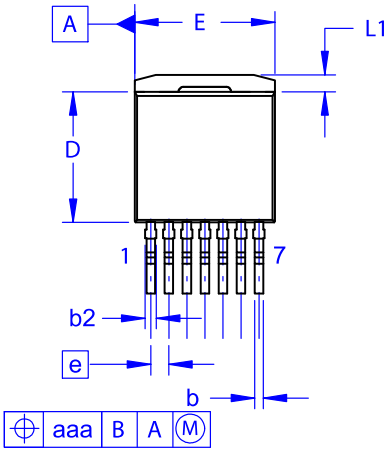


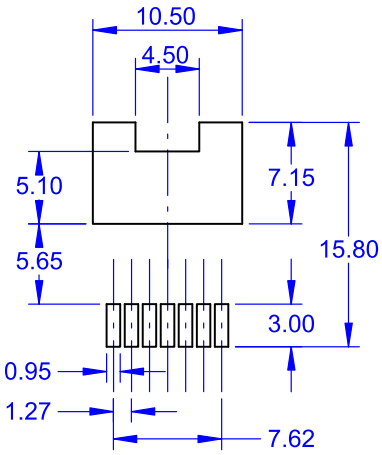
Figure 13. Junction−to−Case Transient Thermal Response Curve



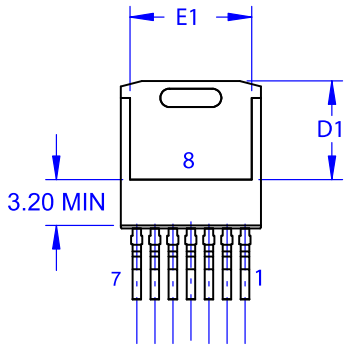
D²PAK7 (TO−263−7L HV)
CASE 418BJ
ISSUE B

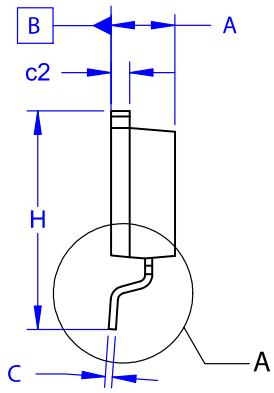
DATE 16 AUG 2019





LAND PATTERN RECOMMENDATION





NOTES:

A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C OUT OF JEDEC STANDARD VALUE.
D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

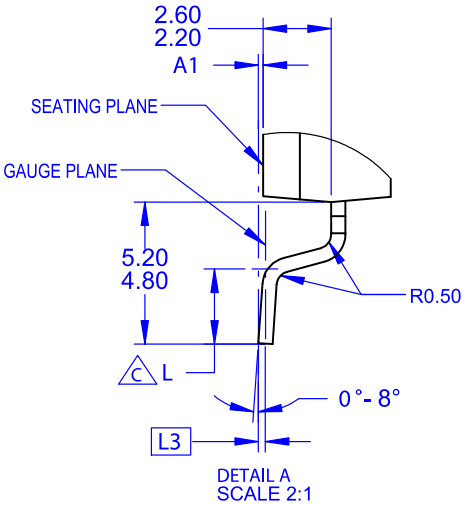
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	MIN	NOM	MAX
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A1	0.00	0.10	0.20
b2	0.60	0.70	0.80
b	0.51	0.60	0.70
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.20	9.40
D1	6.15	6.80	7.15
E	9.70	9.90	10.20
E1	7.15	7.65	8.15
e	~	1.27	~
H	15.10	15.40	15.70
L	2.44	2.64	2.84
L1	1.00	1.20	1.40
L3	~	0.25	~
aaa	~	~	0.25

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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DESCRIPTION:	**D²PAK7 (TO−263−7L HV)**		**PAGE 1 OF 1**

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