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FAIRCHILD SEMICONDUCTOR®

August 2009

FMS6145
Low-Cost Five-Channel 4th-Order Standard Definition Video Filter Driver

Features

- Five 4th-order 8MHz (SD) filters
- Drives single, AC- or DC-coupled, video loads ($2V_{pp}$, 150Ω)
- Drives dual, AC- or DC-coupled, video loads ($2V_{pp}$, 75Ω)
- Transparent input clamping
- AC- or DC-coupled inputs
- AC- or DC-coupled outputs
- DC-coupled outputs eliminate AC-coupling capacitors
- 5V only
- Robust 8kV ESD protection
- Lead-free TSSOP-14 package

Applications

- Cable set-top boxes
- Satellite set-top boxes
- DVD players
- HDTV
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

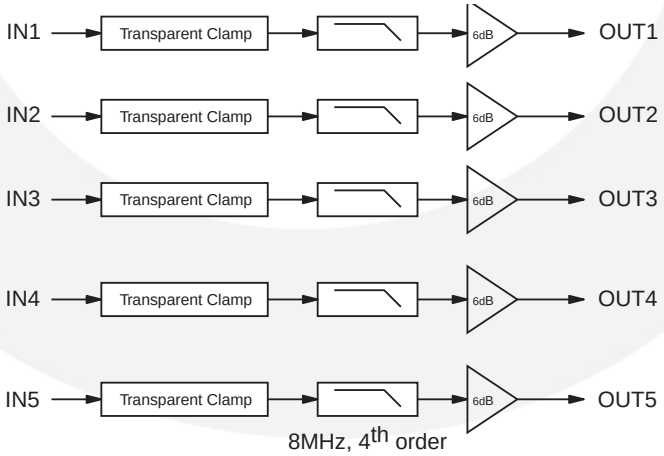
Description

The FMS6145 Low-Cost Video Filter (LCVF) is intended to replace passive LC filters and drivers with a low-cost integrated device. Five 4th-order filters provide improved image quality compared to typical 2nd or 3rd-order passive solutions.

The FMS6145 may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required (see *Applications* section for details).

The outputs can drive AC- or DC-coupled single (150Ω) or dual (75Ω) loads. DC coupling the outputs removes the need for output coupling capacitors. The input DC levels are offset approximately +280mV at the output (see *Applications* section for details).

Functional Block Diagram



8MHz, 4th order

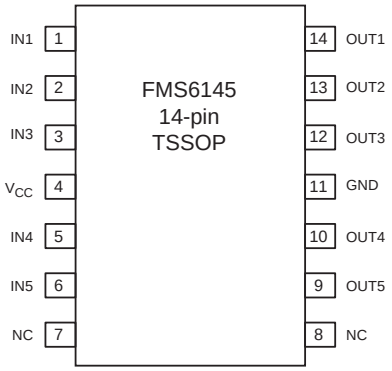
Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packaging Method
FMS6145MTC14X	-40°C to +85°C	RoHS	TSSOP-14	Tape and Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

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Pin Configuration



Pin Assignments

Pin #	Name	Type	Description
1	IN1	Input	Video input, channel 1
2	IN2	Input	Video input, channel 2
3	IN3	Input	Video input, channel 3
4	V_{CC}	Input	+5V supply, do not float
5	IN4	Input	Video input, channel 4
6	IN5	Input	Video input, channel 5
7, 8	NC		No Connect
9	OUT5	Output	Filtered video output, channel 5
10	OUT4	Output	Filtered video output, channel 4
11	GND	Output	Must be tied to ground, do not float
12	OUT3	Output	Filtered video output, channel 3
13	OUT2	Output	Filtered video output, channel 2
14	OUT1	Output	Filtered video output, channel 1

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Absolute Maximum Ratings

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table defines the conditions for actual device operation. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if recommended operating conditions are not exceeded.

Parameter	Min.	Max.	Unit
DC Supply Voltage	-0.3	6	V
Analog and Digital I/O	-0.3	V_{CC} + 0.3	V
Output Channel - Any One Channel (Do Not Exceed)		50	mA

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			150	°C
T_{STSG}	Storage Temperature Range	-65		+150	°C
T_L	Lead Temperature (Soldering, 10s)			300	°C
θ_{JA}	Thermal Resistance, JEDEC Standard Multi-layer Test Boards, Still Air		90		°C/W

Electrostatic Discharge Information

Symbols	Parameter	Max.	Unit
ESD	Human Body Model, JESD22-A114	4	kV
	Charged Device Model, JESD22-C101	2	

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	-40		+85	°C
V_{CC}	V_{CC} Range	+4.75	+5.0	+5.25	V

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DC Electrical Characteristics

T_A = 25°C, V_{CC} = 5V, R_{SOURCE} = 37.5Ω; all inputs are AC-coupled with 0.1µF; all outputs are AC coupled with 220µF into 150Ω loads; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}	Supply Current(1)	FMS6145 (No Load)		30	46	mA
V_{IN}	Video Input Voltage Range	Referenced to GND if DC-coupled		1.4		V_{pp}
PSRR	Power Supply Rejection	DC (All Channels)		-50		dB

Notes:
1.100% tested at 25°C.

AC Electrical Characteristics

T_A = 25°C, V_{IN} = 1V_{pp}, V_{CC} = 5V, R_{SOURCE} = 37.5Ω; all inputs are AC coupled with 0.1µF; all outputs are AC-coupled with 220µF into 150Ω loads; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
AV	Channel Gain(1)	All Channels	6.0	6.2	6.4	dB
f_{1dB}	-1dB Bandwidth(1)	All Channels	4.5	6.7		MHz
f_c	-3dB Bandwidth	All Channels		7.9		MHz
f_{SB}	Attenuation (Stopband Reject)	All Channels at f = 27MHz		48		dB
dG	Differential Gain	All Channels		0.3		%
dϕ	Differential Phase	All Channels		0.6		°
THD	Output Distortion (All Channels)	V_{OUT} = 1.8V_{pp}, 1MHz		0.4		%
X_{TALK}	Crosstalk (Channel-to-Channel)	at 1MHz		-60		dB
SNR	Signal-to-Noise Ratio	All Channels, NTC-7 Weighting: 100kHz to 4.2MHz		75		dB
t_{pd}	Propagation Delay	Delay from Input-to-Output, 4.5MHz		59		ns

Notes:
1.100% tested at 25°C.

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Typical Performance Characteristics

T_A = 25°C, V_{CC} = 5V, R_{SOURCE} = 37.5Ω; all inputs AC coupled with 0.1µF; all outputs are AC coupled with 220µF into 150Ω loads; unless otherwise noted.

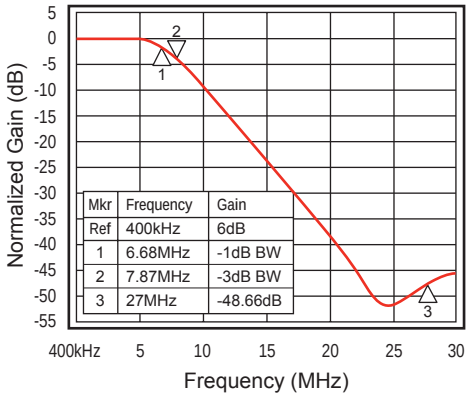


Figure 1. Frequency Response

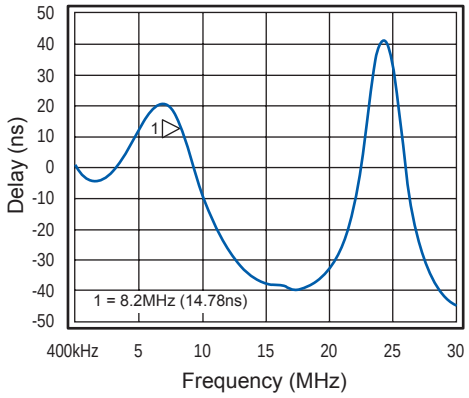


Figure 2. Group Delay vs. Frequency

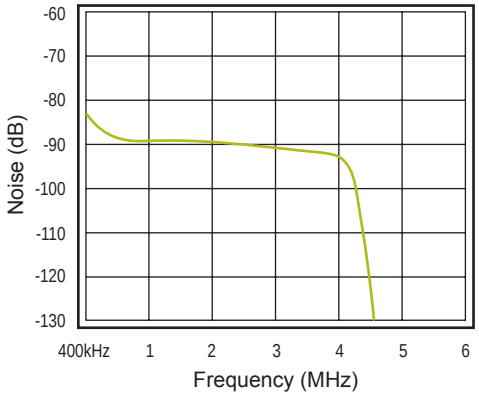


Figure 3. Noise vs. Frequency

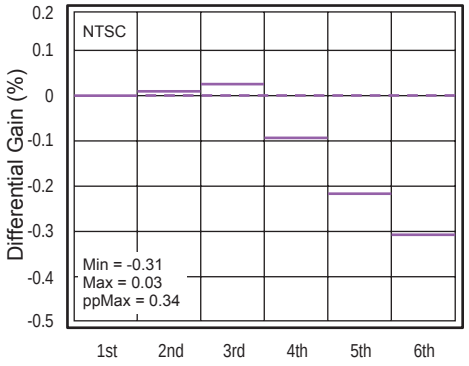


Figure 4. Differential Gain

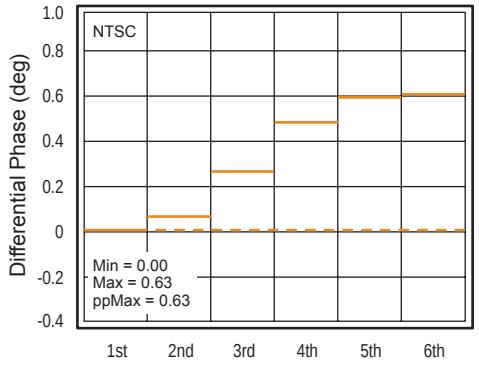


Figure 5. Differential Phase

Typical Application Diagrams

The following circuit may be used for direct DC-coupled drive by DACs with an output voltage range of 0V to 1.4V. AC-coupled or DC-coupled outputs may be used with AC-coupled outputs, offering slightly lower power dissipation.

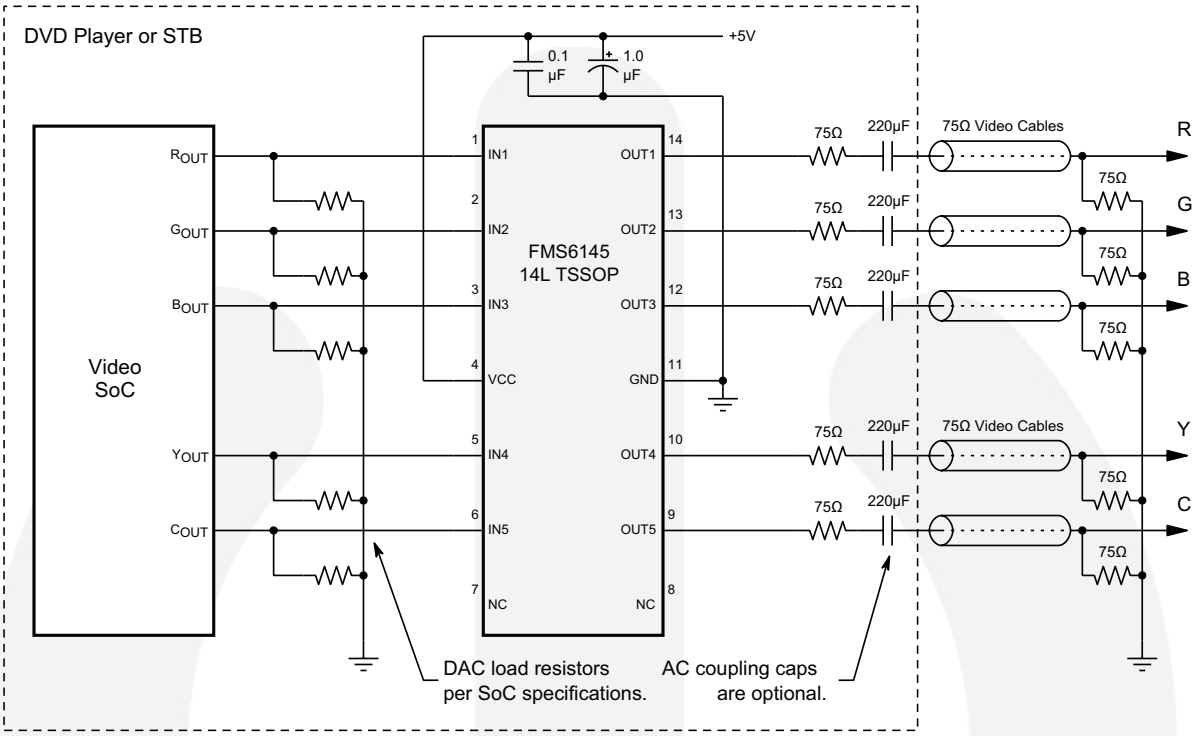
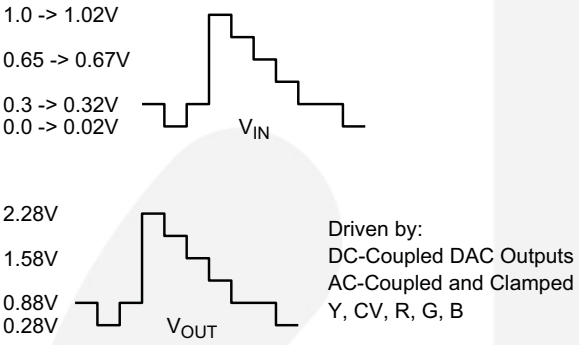


Figure 6. Typical Application Diagram

Application Information

Application Circuits

The FMS6145 Low Cost Video Filter (LCVF) provides 6dB gain from input to output. In addition, the input is slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC-current into the load. Typical voltage levels are shown in the diagram below:



There is a 280mV offset from the DC input level to the DC output level. $V_{OUT} = 2 * V_{IN} + 280mV$.

Figure 7. Typical Voltage Levels

The FMS6145 provides an internal diode clamp to support AC-coupled input signals. If the input signal does not go below ground, the input clamp does not operate. This allows DAC outputs to directly drive the FMS6145 without an AC coupling capacitor. When the input is AC coupled, the diode clamp sets the sync tip (or lowest voltage) just below ground. The worst-case sync tip compression due to the clamp cannot exceed 7mV. The input level set by the clamp, combined with the internal DC offset, keeps the output within its acceptable range.

For symmetric signals like Chroma, U, V, Pb, and Pr, the average DC bias is fairly constant and the inputs can be AC coupled with the addition of a pull-up resistor to set the DC input voltage. DAC outputs can also drive these same signals without the AC coupling capacitor. A conceptual illustration of the input clamp circuit is shown in Figure 8.

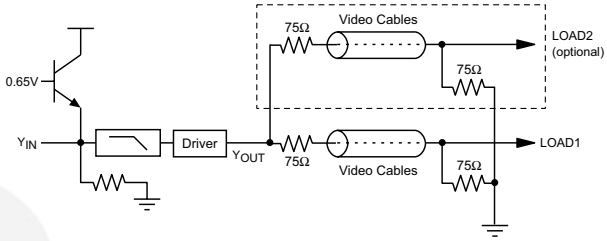


Figure 8. Input Clamp Circuit

I/O Configurations

For a DC-coupled DAC drive with DC-coupled outputs, use the configuration in Figure 9.

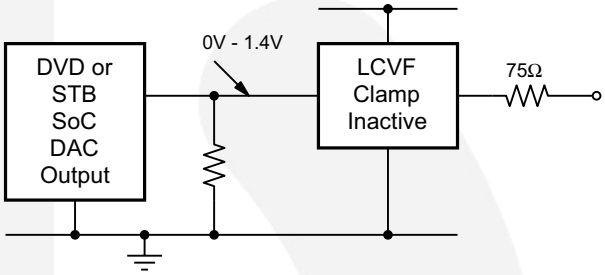


Figure 9. DC-Coupled Inputs and Outputs

Alternatively, if the DAC's average DC output level causes the signal to exceed the range of 0V to 1.4V, it can be AC coupled as shown in FIgure 10.

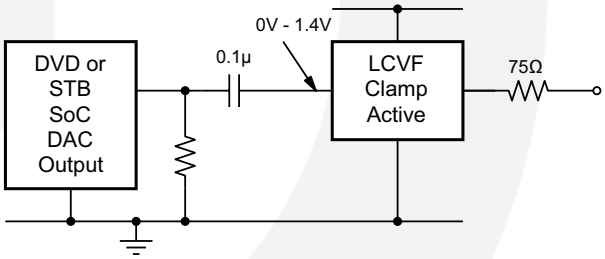


Figure 10. AC-Coupled Inputs, DC-Coupled Outputs

When the FMS6145 is driven by an unknown external source or a SCART switch with its own clamping circuitry, the inputs should be AC coupled as shown in Figure 11.

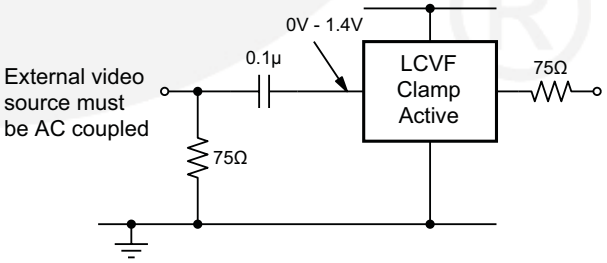


Figure 11. SCART with DC-Coupled Outputs

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The same method can be used for biased signals, with the addition of a pull-up resistor to make sure the clamp never operates. The internal pull-down resistance is 800kΩ ±20%, so the external resistance should be 7.5MΩ to set the DC level to 500mV; as shown in Figure 12.

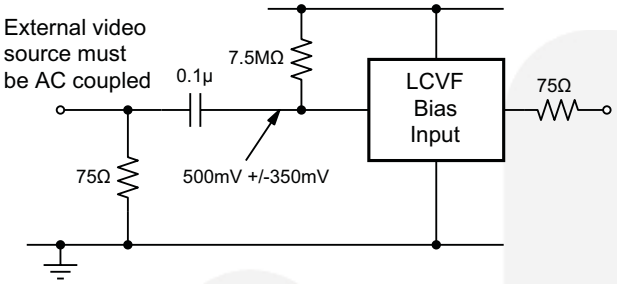


Figure 12. Biased SCART with DC-Coupled Outputs

The same circuits can be used with AC-coupled outputs if desired.

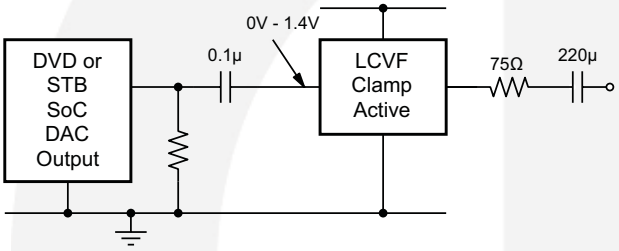


Figure 13. DC-Coupled Inputs, AC-Coupled Outputs

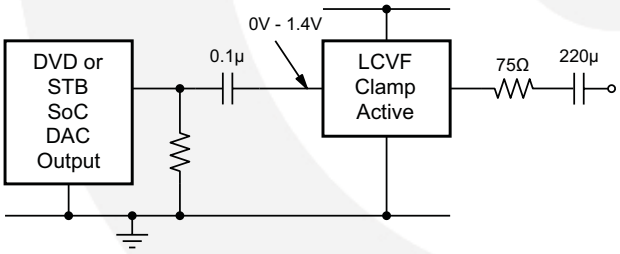


Figure 14. AC-Coupled Inputs and Outputs

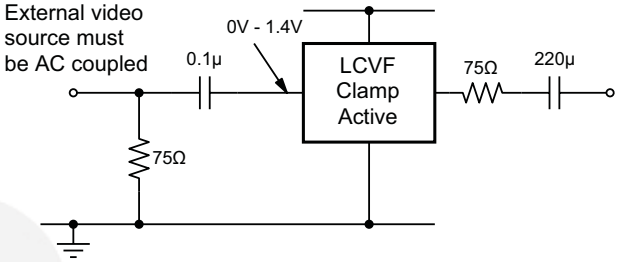


Figure 15. Biased SCART with AC-Coupled Outputs

Note: The video tilt or line time distortion is dominated by the AC-coupling capacitor. The value may need to be increased beyond 220µF to obtain satisfactory operation in some applications.

Power Dissipation

The FMS6145 output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following example can be used to calculate the FMS6146's power dissipation and internal temperature rise.

$T_j = T_A + P_d \bullet q_{JA}$ EQ. 1

where: $P_d = P_{CH1} + P_{CH2} + P_{CH3}$ and EQ. 2

$P_{CHx} = V_{CC} \bullet I_{CH} - (V_O^2/R_L)$ EQ. 3

where: $V_O = 2V_{IN} + 0.280V$ EQ. 4

$I_{CH} = (I_{CC}/3) + (V_O/R_L)$ EQ. 5

V_{IN} = RMS value of input signal

I_{CC} = 30mA

V_{CC} = 5V

R_L = channel load resistance

Board layout can also affect thermal characteristics. Refer to the *Layout Considerations* section for details.

The FMS6145 is specified to operate with output currents typically less than 50mA, more than sufficient for a dual (75Ω) video load. Internal amplifiers are current limited to a maximum of 100mA and should withstand brief-duration short-circuit conditions; this capability is not guaranteed.

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Layout Considerations

General layout and supply bypassing play major roles in high-frequency performance and thermal characteristics. Fairchild offers a demonstration board, FMS6145DEMO, to guide layout and aid device testing and characterization. The FMS6145DEMO is a four-layer board with full power and ground planes. Following this layout configuration provides the optimum performance and thermal characteristics. For optimum results, follow the guidelines below as a basis for high-frequency layout:

- Include 1µF and 0.1µF ceramic bypass capacitors.
- Place the 1µF capacitor within 0.75 inches of the power pin.
- Place the 0.1µF capacitor within 0.1 inches of the power pin.
- For multi-layer boards, use a large ground plane to help dissipate heat.
- For two-layer boards, use a ground plane that extends beyond the device by at least 0.5 inches.
- Minimize all trace lengths to reduce series inductances.

Output Considerations

The FMS6145 outputs are DC offset from the input by 150mV. Therefore, $V_{OUT} = 2 \bullet V_{IN}$ DC+150mV. This offset is required to obtain optimal performance from the output driver and is held at the minimum value to decrease the standing DC current into the load. Since the FMS6145 has a 2x (6dB) gain, the output is typically connected via a 75Ω-series back-matching resistor, followed by the 75Ω video cable. Due to the inherent divide by two of this configuration, the blanking level at the load of the video signal is always less than 1V. When AC-coupling the output, ensure that the coupling capacitor of choice passes the lowest frequency content in the video signal and that line time distortion (video tilt) is kept as low as possible.

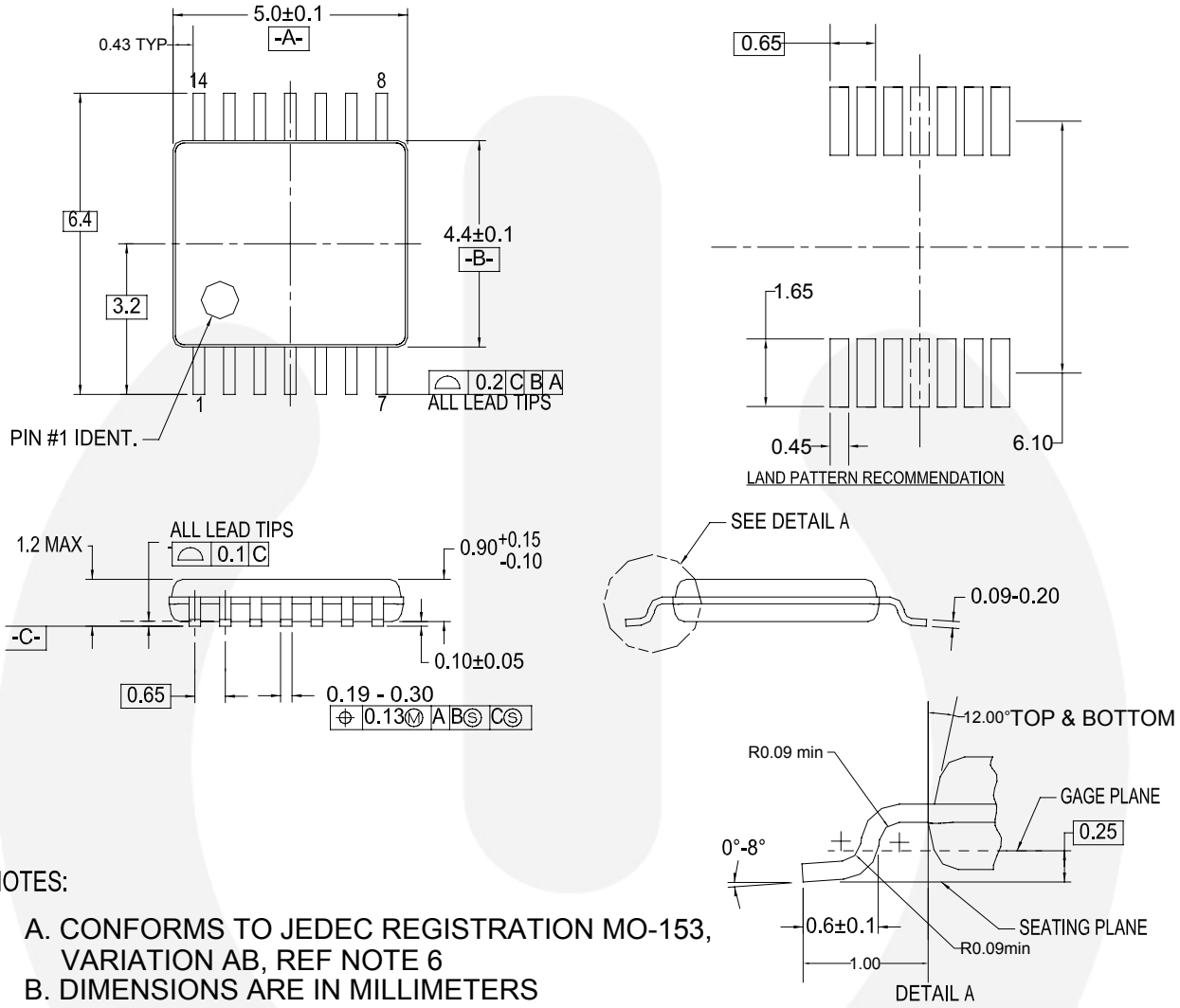
The selection of the coupling capacitor is a function of the subsequent circuit input impedance and the leakage current of the input being driven. To obtain the highest quality output video signal, the series termination resistor must be placed as close to the output pin as possible. This reduces the parasitic capacitance and inductance effect on the output driver. The distance from the device pin to the series termination resistor should be no greater than 0.1 inches.



Figure 16. Distance from Device Pin to Series Termination Resistor

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Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

E. LANDPATTERN STANDARD: SOP65P640X110-14M

F. DRAWING FILE NAME: MTC14REV6

Figure 17. TSSOP-14 Package

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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PowerTrench®
PowerXS™
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SuperSOT™-6
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TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
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