FDMC86244-L701-VB Datasheet

N-Channel 150 V (D-S) MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	150
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.035
Q_g typ. (nC)	8.5
I_D (A)	25.5 [a]
Configuration	Single

FEATURES

- Trench Cell optimizes balance of $R_{DS(on)}$, Q_g, Q_{sw}, and Q_{oss}
- 100 % R_g and UIS tested

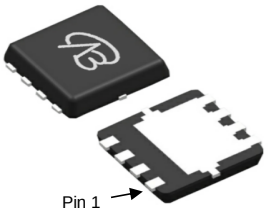
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

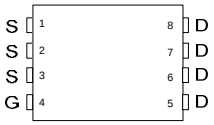
- Primary side switching
- Synchronous rectification
- DC/DC converter
- Motor drive control
- Load switch

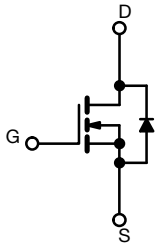
DFN 3x3

Top View Bottom View



Top View





N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	150	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	25.5	A
	T_C = 70 °C		20.4	
	T_A = 25 °C		7 [b, c]	
	T_A = 70 °C		5.6 [b, c]	
Pulsed drain current (t = 100 µs)		I_{DM}	50	
Continuous source-drain diode current	T_C = 25 °C	I_S	54.8	
	T_A = 25 °C		4.2 [b, c]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	20	
Single pulse avalanche energy		E_{AS}	20	mJ
Maximum power dissipation	T_C = 25 °C	P_D	65.8	W
	T_C = 70 °C		42.1	
	T_A = 25 °C		5.1 [b, c]	
	T_A = 70 °C		3.2 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [c]			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [b]	t ≤ 10 s	R_{thJA}	20	25	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.5	1.9	

Notes

a. T_C = 25 °C
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. The DFN3x3 package is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
f. Maximum under steady state conditions is 65 °C/W

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	150	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = 250 mA	-	92	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 µA	-	-7.1	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2	-	4	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 150 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 150 V, V_{GS} = 0 V, T_J = 70 °C	-	-	15	
On-state drain current [a]	$I_{D(on)}$	$V_{DS} \leq$ 10 V, V_{GS} = 10 V	20	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 7 A	-	0.035	-	Ω
Forward transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 7 A	-	16	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = 75 V, V_{GS} = 0 V, f = 1 MHz	-	550	-	pF
Output capacitance	C_{oss}		-	120	-	
Reverse transfer capacitance	C_{rss}		-	6	-	
Total gate charge	Q_g	V_{DS} = 75 V, V_{GS} = 10 V, I_D = 7 A	-	10.85	22	nC
		V_{DS} = 75 V, V_{GS} = 7.5 V, I_D = 7 A	-	8.5	13	
Gate-source charge	Q_{gs}		-	3	-	
Gate-drain charge	Q_{gd}		-	3	-	
Output charge	Q_{oss}	V_{DS} = 75 V, V_{GS} = 0 V	-	27.7	42	
Gate resistance	R_g	f = 1 MHz	0.24	1.2	2.4	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 75 V, R_L = 13.4 Ω, $I_D \cong$ 5.6 A, V_{GEN} = 10 V, R_g = 1 Ω	-	18	36	ns
Rise time	t_r		-	6	12	
Turn-off delay time	$t_{d(off)}$		-	30	60	
Fall time	t_f		-	9	18	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 75 V, R_L = 13.4 Ω, $I_D \cong$ 5.6 A, V_{GEN} = 7.5 V, R_g = 1 Ω	-	20	40	
Rise time	t_r		-	8	16	
Turn-off delay time	$t_{d(off)}$		-	25	50	
Fall time	t_f		-	11	22	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	-	54.8	A
Pulse diode forward current	I_{SM}		-	-	50	
Body diode voltage	V_{SD}	I_S = 5.6 A, V_{GS} = 0 V	-	0.8	1.2	V
Body diode reverse recovery time	t_{rr}	I_F = 5.6 A, di/dt = 100 A/µs, T_J = 25 °C	-	60	120	ns
Body diode reverse recovery charge	Q_{rr}		-	133	266	nC
Reverse recovery fall time	t_a		-	50	-	ns
Reverse recovery rise time	t_b		-	10	-	

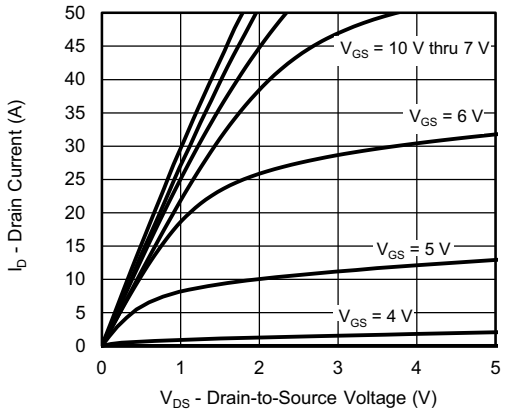
Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

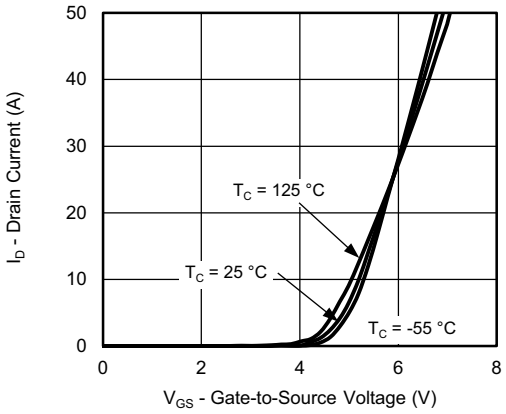
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

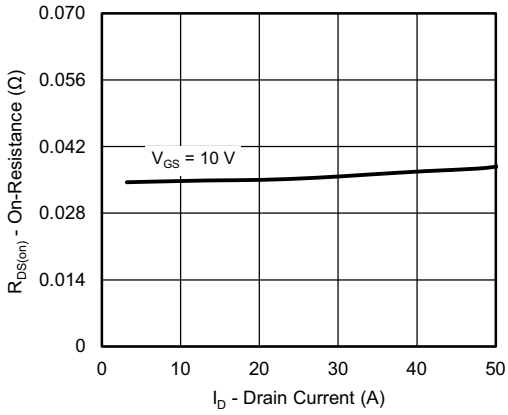
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



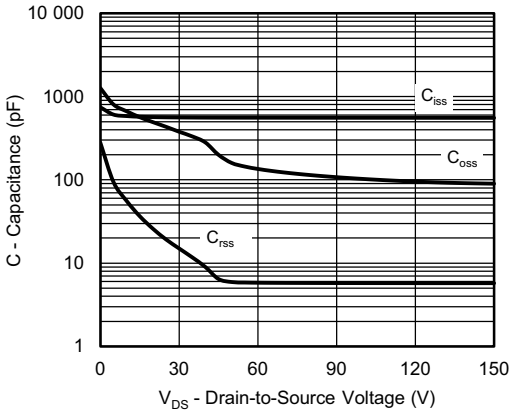
Output Characteristics



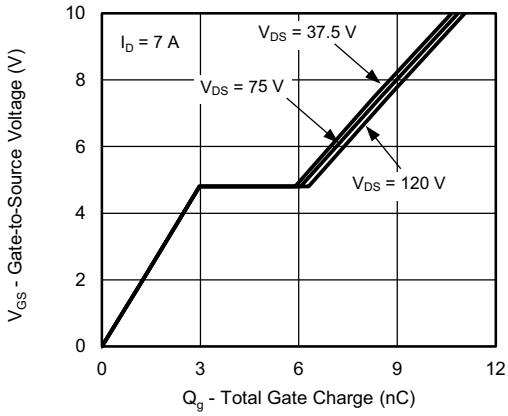
Transfer Characteristics



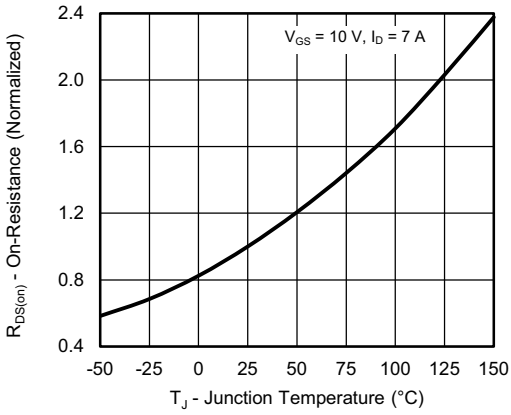
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

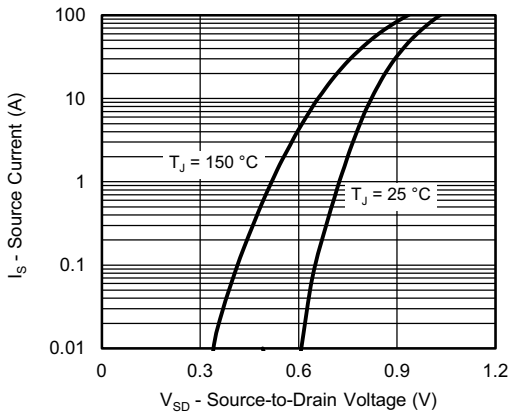


Gate Charge

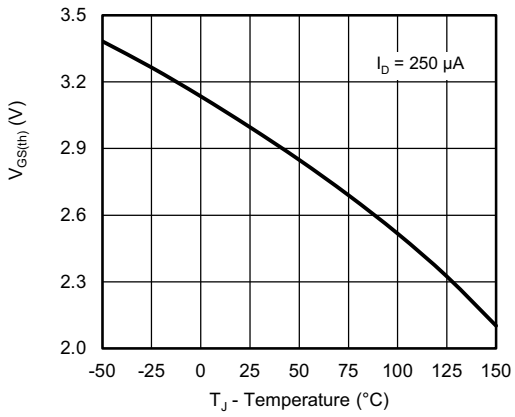


On-Resistance vs. Junction Temperature

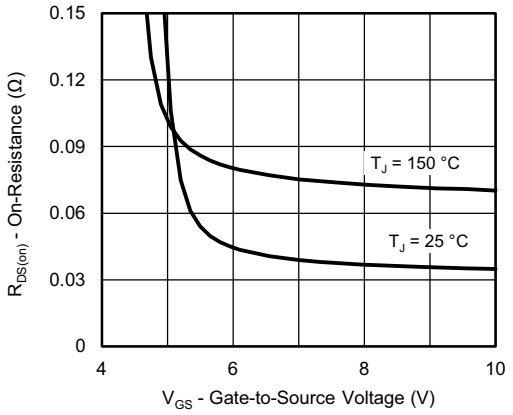
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



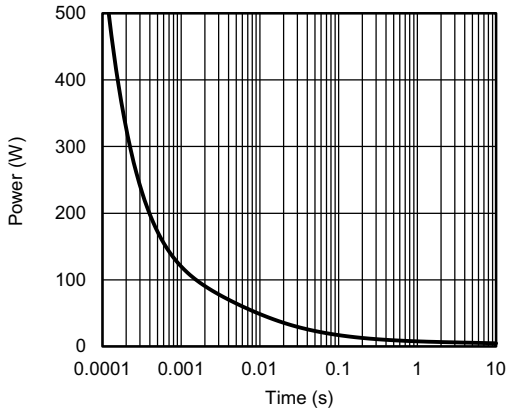
Source-Drain Diode Forward Voltage



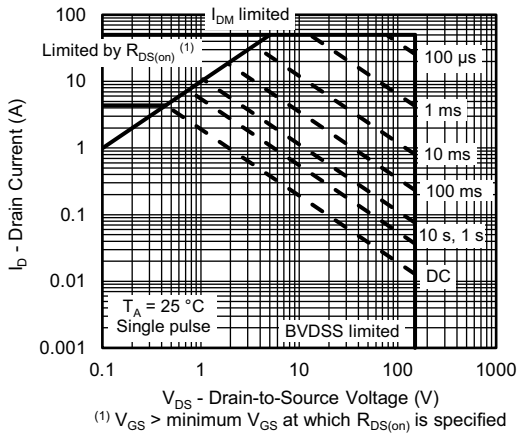
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage

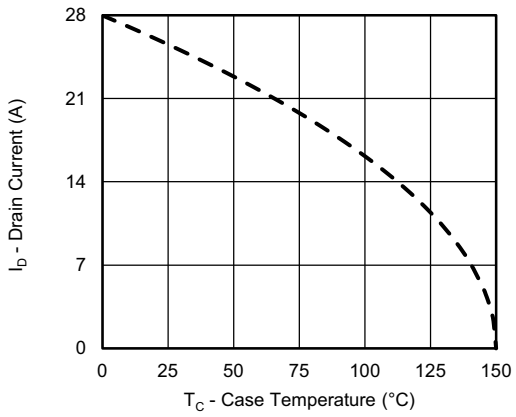


Single Pulse Power, Junction-to-Ambient

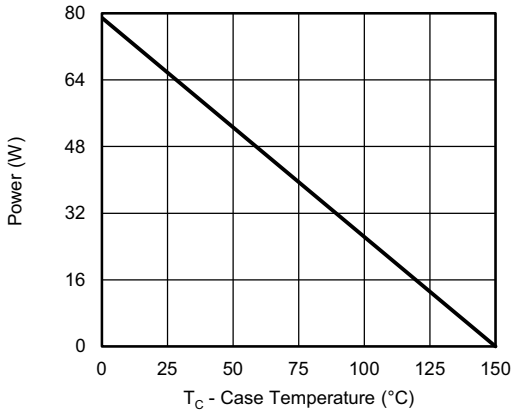


Safe Operating Area, Junction-to-Ambient

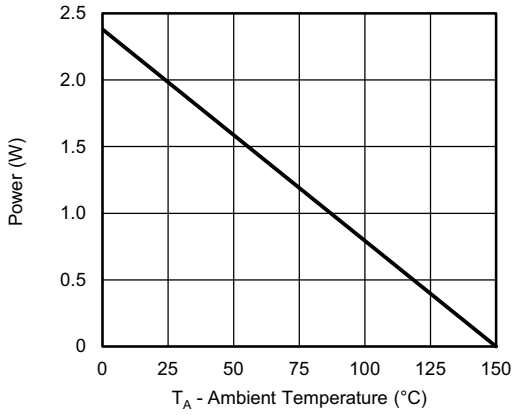
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]



Power, Junction-to-Case

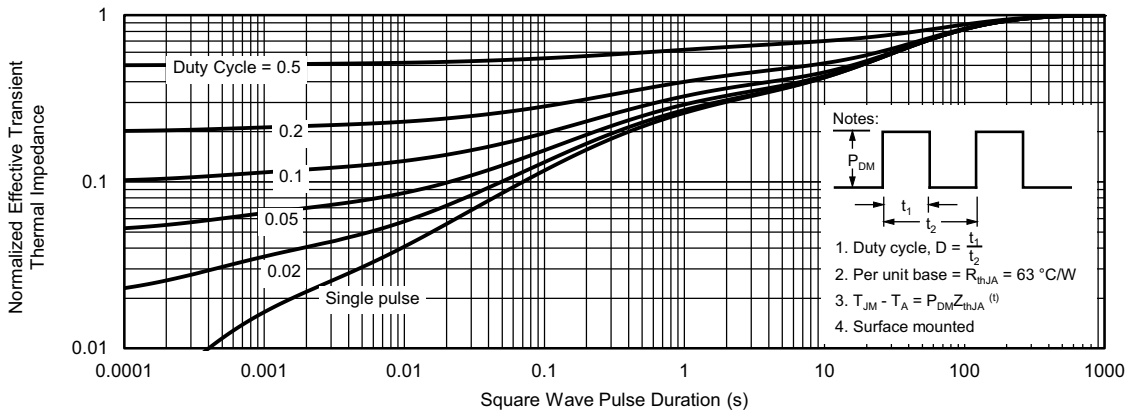


Power, Junction-to-Ambient

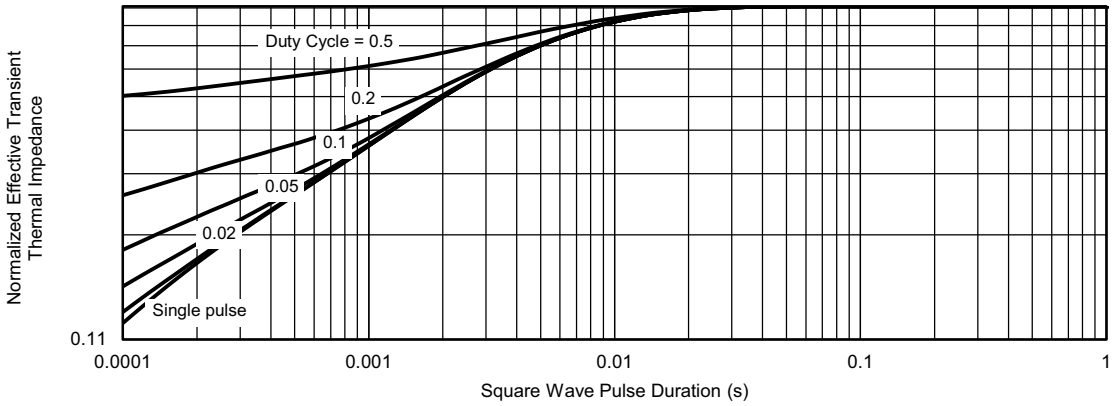
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

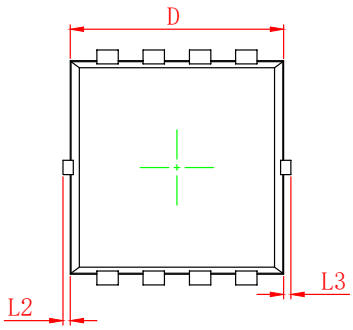


Normalized Thermal Transient Impedance, Junction-to-Ambient

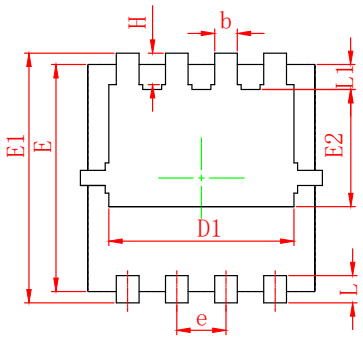


Normalized Thermal Transient Impedance, Junction-to-Case

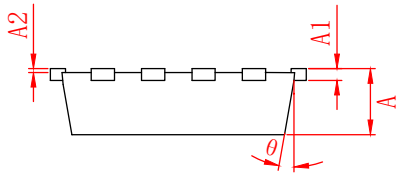
PDFNWB3×3-8L Package Outline Dimensions



Top View
[顶视图]



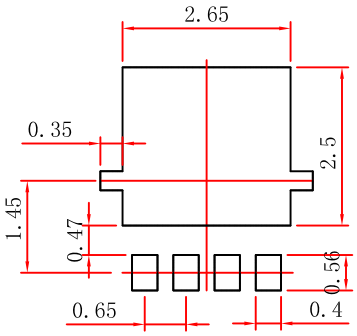
Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.650	0.850	0.026	0.033
A1	0.203REF.		0.008REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.050	2.550	0.081	0.100
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.450	1.650	0.057	0.065
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
Φ	9°	13°	9°	13°

Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

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