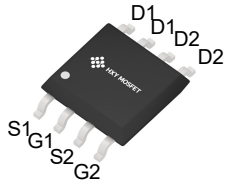
ZXMN2A04DN8

Dual N-Channel Enhancement Mode MOSFET

Description

The ZXMN2A04DN8 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

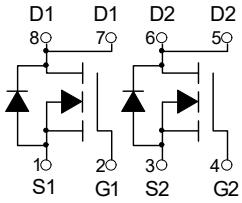


SOP-8
(SO-8)

General Features

V_{DS} = 20V I_D = 6A

$R_{DS(ON)}$ < 25mΩ @ V_{GS}=4.5V



Dual N-Channel MOSFET

Application

Battery protection

Load switch

Uninterruptible power supply

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
ZXMN2A04DN8	SOP-8(SO-8)	HXY MOSFET	3000

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	±12	V
I_D@T_A=25℃	Drain Current, V_{GS} @ 4.5V[3]	6	A
I_D@T_A=70℃	Drain Current, V_{GS} @ 4.5V[3]	4.8	A
I_{DM}	Pulsed Drain Current[1]	26	A
P_D@T_A=25℃	Total Power Dissipation	2	W
	Linear Derating Factor	0.016	W/℃
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	62.5	℃/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	20	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=4.5V, I_D=6A	-	21	25	mΩ
		V_{GS}=2.5V, I_D=4A	-	32	45	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	-	1.2	3	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=6A	-	6	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=20V, V_{GS}=0V	-	-	25	uA
	Drain-Source Leakage Current (T_j=70°C)	V_{DS}=20V ,V_{GS}=0V	-	-	250	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±12V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=6A V_{DS}=16V V_{GS}=4.5V	-	11	17.6	nC
Q_{gs}	Gate-Source Charge		-	1.1	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge		-	4.1	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=10V I_D=1A R_G=3.3Ω,V_{GS}=10V R_D=10Ω	-	4.2	-	ns
t_r	Rise Time		-	9	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	23	-	ns
t_f	Fall Time		-	3.5	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V V_{DS}=20V f=1.0MHz	-	570	910	pF
C_{oss}	Output Capacitance		-	90	-	pF
C_{rss}	Reverse Transfer Capacitance		-	85	-	pF
R_g	Gate Resistance	f=1.0MHz	-	1.6	2.4	Ω
V_{SD}	Forward On Voltage[2]	I_S=1.7A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time[2]	I_S=6A, V_{GS}=0V, dI/dt=100A/μs	-	21	-	ns
Q_{rr}	Reverse Recovery Charge		-	14	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec ; 135 ℃/W when mounted on Min. copper pad.

Typical Characteristics

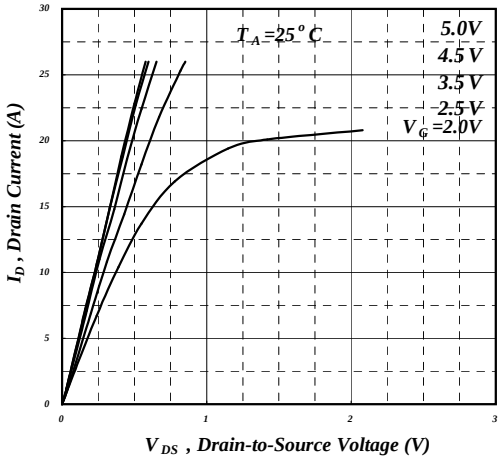


Fig 1. Typical Output Characteristics

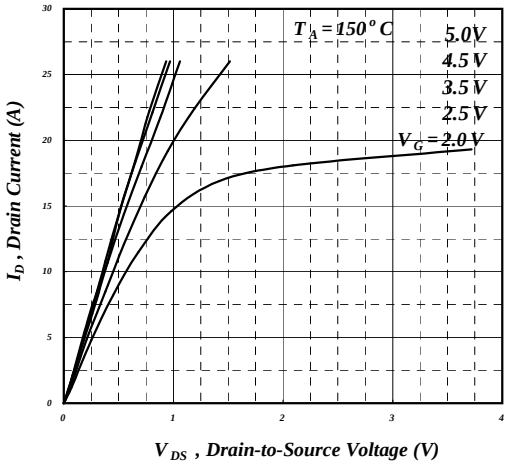


Fig 2. Typical Output Characteristics

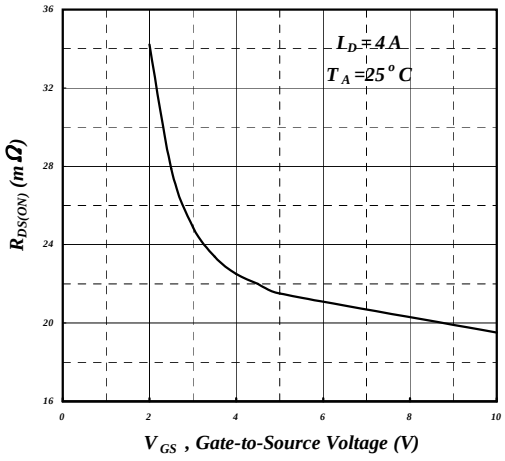


Fig 3. On-Resistance v.s. Gate Voltage

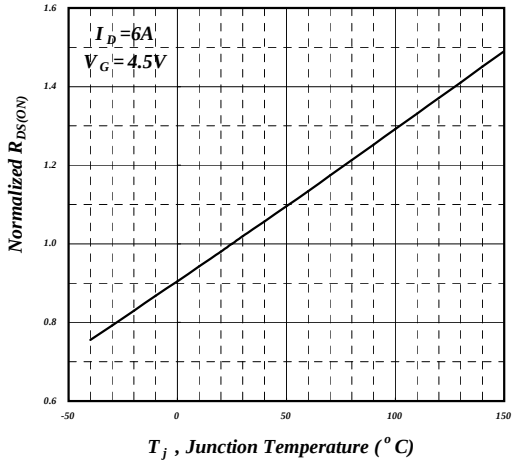


Fig 4. Normalized On-Resistance v.s. Temperature

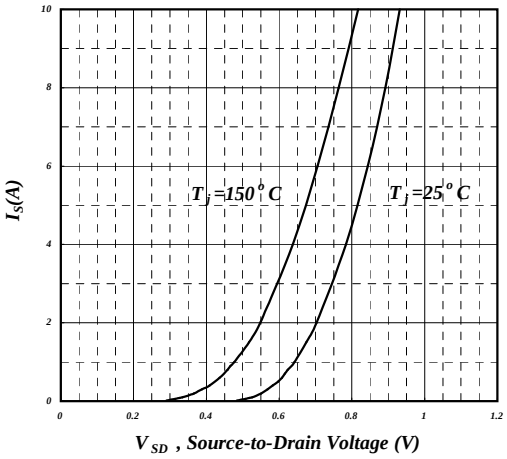


Fig 5. Forward Characteristic of Reverse Diode

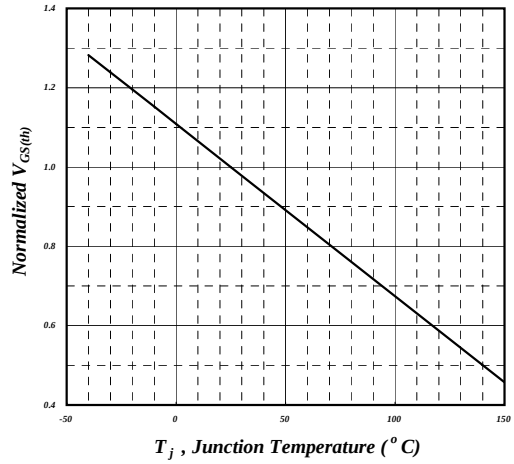


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

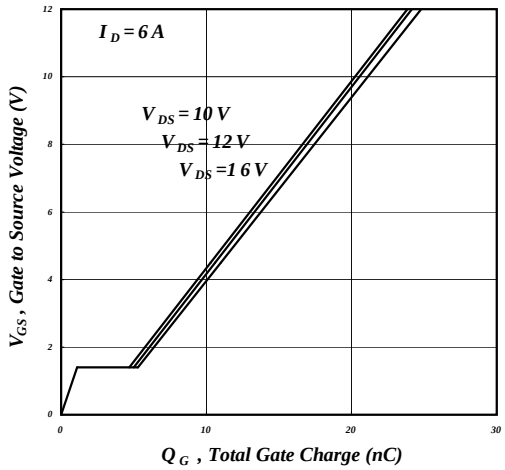


Fig 7. Gate Charge Characteristics

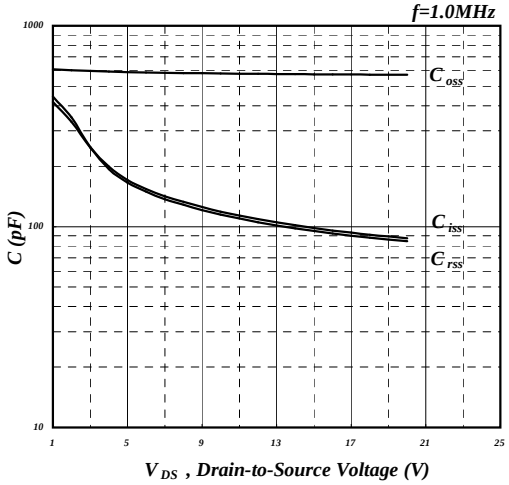


Fig 8. Typical Capacitance Characteristics

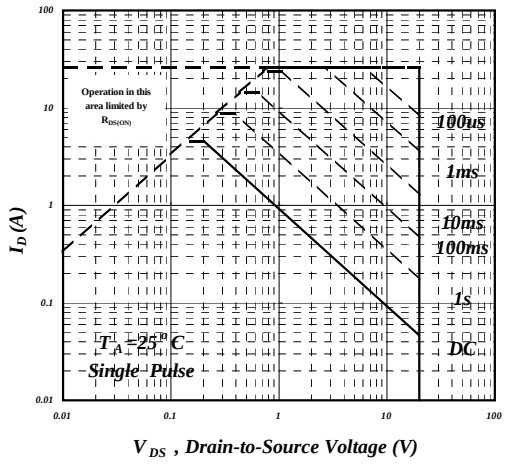


Fig 9. Maximum Safe Operating Area

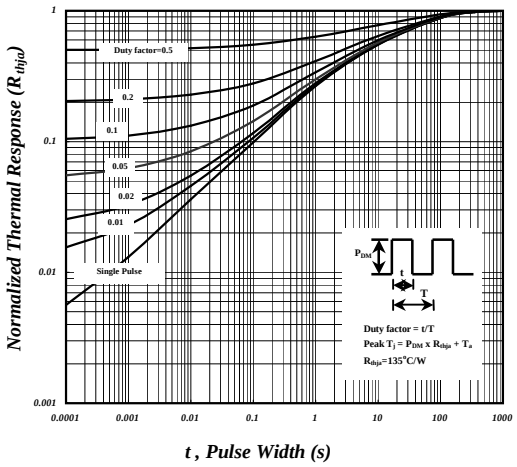


Fig 10. Effective Transient Thermal Impedance

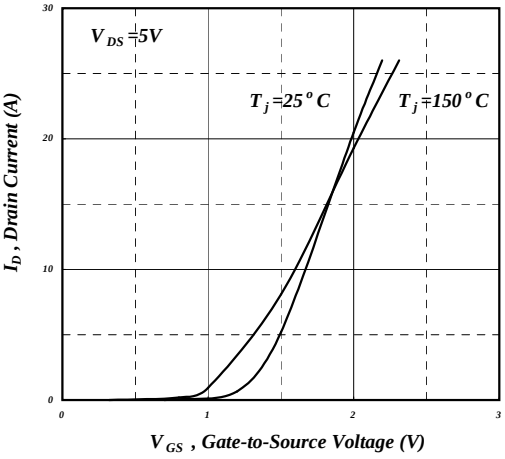


Fig 11. Transfer Characteristics

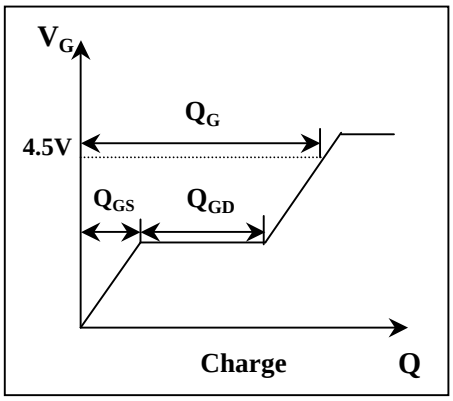
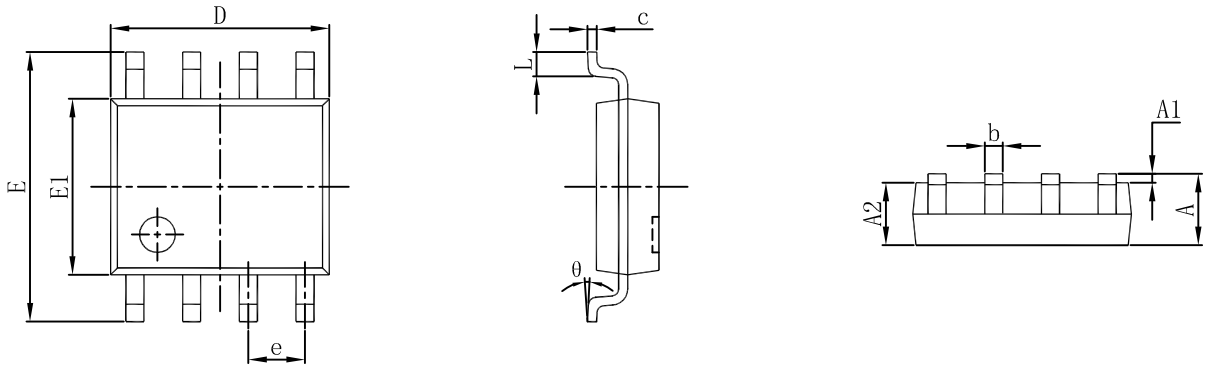
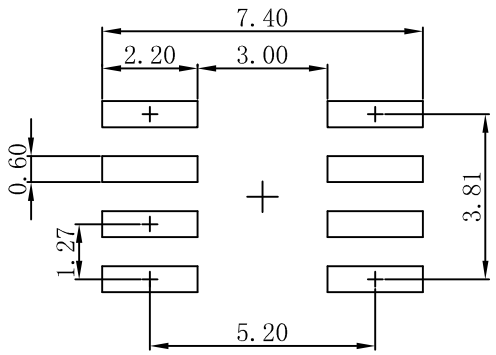


Fig 12. Gate Charge Waveform

SOP-8(SO-8) Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

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