# I²C-Compatible, Wide Bandwidth, Five 2:1 Multiplexer

# ADG795A/ADG795G

OBSOLETE

## FEATURES

- Bandwidth: 325 MHz
- Low insertion loss and on resistance: 2.6 Ω typical
- On resistance flatness: 0.3 Ω typical
- Single 3 V/5 V supply operation
- 3.3 V analog signal range (5 V supply, 75 Ω load)
- Low quiescent supply current: 1 nA typical
- Fast switching times: $t_{ON}$ = 186 ns, $t_{OFF}$ = 177 ns
- ESD protection
  - 4 kV human body model (HBM)
  - 200 V machine model (MM)
  - 1 kV field-induced charged device model (FICDM)
- I²C®-compatible interface
- Compact 24-lead LFCSP

## APPLICATIONS

- S-Video RGB/YPbPr video switches
- HDTV
- Projection TV
- DVD-R/RW
- AV receivers

## FUNCTIONAL BLOCK DIAGRAMS

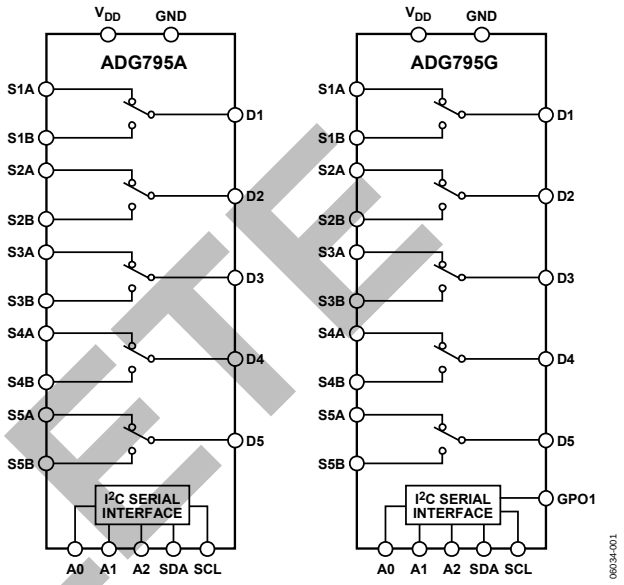



*Figure 1.*

## GENERAL DESCRIPTION

The ADG795A/ADG795G are monolithic CMOS devices comprising five 2:1 multiplexers/demultiplexers controllable via a standard I²C serial interface. The CMOS process provides ultralow power dissipation, yet gives high switching speed and low on resistance.

The on-resistance profile is very flat over the full analog input range and wide bandwidth ensures excellent linearity and low distortion. These features, combined with a wide input signal range make the ADG795A/ADG795G the ideal switching solution for a wide range of TV applications including S-video, RGB and YPbPr video switches.

The switches conduct equally well in both directions when on. In the off condition, signal levels up to the supplies are blocked. The ADG795A/ADG795G switches exhibit break-before-make switching action. The ADG795G has one general-purpose logic output pins controlled by the I²C interface that can also be used to control other non-I²C-compatible devices such as video filters. The integrated I²C interface provides a large degree of flexibility in the system design. It has three configurable I²C address pins that allow up to eight devices on the same bus. This allows the user to expand the capability of the device by increasing the size of the switching array.

The ADG795A/ADG795G operate from a single 3 V or 5 V supply voltage and are available in a compact 4 mm × 4 mm body, 24-lead, lead-free package (LFCSP).

## PRODUCT HIGHLIGHTS

1. Wide bandwidth: 325 MHz.
2. Ultralow power dissipation.
3. Extended input signal range.
4. Integrated I²C serial interface.
5. Compact 4 mm × 4 mm, 24-lead, lead-free LFCSP.
6. ESD protection tested as per ESD Association standards:
   4 kV HBM (ANSI/ESD STM5.1-2001)
   200 V MM (ANSI/ESD STM5.2-1999)
   1 kV FICDM (ANSI/ESDSTM5.3.1-1999)

**Rev. 0**

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113
©2006 Analog Devices, Inc. All rights reserved.

# TABLE OF CONTENTS

Features ..... 1
Applications ..... 1
Functional Block Diagrams ..... 1
General Description ..... 1
Product Highlights ..... 1
Specifications ..... 3
I²C Timing Specifications ..... 7
Timing Diagram ..... 8
Absolute Maximum Ratings ..... 9
ESD Caution ..... 9
Pin Configuration and Function Descriptions ..... 10
Typical Performance Characteristics ..... 11
Test Circuits ..... 14
Terminology ..... 16
Theory of Operation ..... 17
I²C Serial Interface ..... 17
I²C Address ..... 17
Write Operation ..... 17
LDSW bit ..... 19
Power On/Software Reset ..... 19
Read Operation ..... 19
Evaluation Board ..... 20
Using the ADG795G Evaluation Board ..... 20
Outline Dimensions ..... 23
Ordering Guide ..... 23

## REVISION HISTORY

**7/06—Revision 0: Initial Version**

OBSOLETE

# SPECIFICATIONS

$V_{DD}$ = 5 V ± 10%, GND = 0 V, $T_A$ = −40°C to +85°C, unless otherwise noted.

**Table 1.**

| Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range[2] | $V_S = V_{DD}$, $R_L$ = 1 MΩ | 0 | | 4 | V |
| | $V_S = V_{DD}$, $R_L$ = 75 Ω | 0 | | 3.3 | V |
| On Resistance, $R_{ON}$ | $V_D$ = 0 V, $I_{DS}$ = −10 mA, see Figure 22 | | 2.2 | 3.5 | Ω |
| | $V_D$ = 0 V to 1 V, $I_{DS}$ = −10 mA, see Figure 22 | | | 4 | Ω |
| On-Resistance Matching Between Channels, $\Delta R_{ON}$ | $V_D$ = 0 V, $I_{DS}$ = −10 mA | | 0.15 | 0.5 | Ω |
| | $V_D$ = 1 V, $I_{DS}$ = −10 mA | | | 0.6 | Ω |
| On-Resistance Flatness, $R_{FLAT(ON)}$ | $V_D$ = 0 V to 1 V, $I_{DS}$ = −10 mA | | 0.3 | 0.55 | Ω |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage ($I_{S(OFF)}$) | $V_D$ = 4 V/1 V, $V_S$ = 1 V/4 V, see Figure 23 | | ±0.25 | | nA |
| Drain Off Leakage ($I_{D(OFF)}$) | $V_D$ = 4 V/1 V, $V_S$ = 1 V/4 V, see Figure 23 | | ±0.25 | | nA |
| Channel On Leakage ($I_{D(ON)}$, $I_{S(ON)}$) | $V_D = V_S$ = 4 V/1 V, see Figure 24 | | ±0.25 | | nA |
| DYNAMIC CHARACTERISTICS[3] | | | | | |
| $t_{ON}$, $t_{ENABLE}$ | $C_L$ = 35 pF, $R_L$ = 50 Ω, $V_S$ = 2 V, see Figure 28 | | 186 | 250 | ns |
| $t_{OFF}$, $t_{DISABLE}$ | $C_L$ = 35 pF, $R_L$ = 50 Ω, $V_S$ = 2 V, see Figure 28 | | 177 | 240 | ns |
| Break-Before-Make Time Delay, $t_D$ | $C_L$ = 35 pF, $R_L$ = 50 Ω, $V_{S1} = V_{S2}$ = 2 V, see Figure 29 | 1 | 3 | | ns |
| $I^2C$-to-GPO Propagation Delay, $t_H$, $t_L$ | ADG795G only | | | 130 | ns |
| Off Isolation | $f$ = 10 MHz, $R_L$ = 50 Ω, see Figure 26 | | −60 | | dB |
| Channel-to-Channel Crosstalk | $f$ = 10 MHz, $R_L$ = 50 Ω, see Figure 27 | | | | |
| Same Multiplexer | | | −55 | | dB |
| Different Multiplexer | | | −70 | | dB |
| −3 dB Bandwidth | $R_L$ = 50 Ω, see Figure 25 | | 325 | | MHz |
| THD + N | $R_L$ = 100 Ω | | 0.14 | | % |
| Charge Injection | $C_L$ = 1 nF, $V_S$ = 0 V, see Figure 30 | | 5 | | pC |
| $C_{S(OFF)}$ | | | 10 | | pF |
| $C_{D(OFF)}$ | | | 13 | | pF |
| $C_{D(ON)}$, $C_{S(ON)}$ | | | 27 | | pF |
| Power Supply Rejection Ratio, PSRR | $f$ = 20 kHz | | 70 | | dB |
| Differential Gain Error | CCIR330 test signal | | 0.32 | | % |
| Differential Phase Error | CCIR330 test signal | | 0.44 | | Degrees |
| LOGIC INPUTS[3] | | | | | |
| A0, A1, A2 | | | | | |
| Input High Voltage, $V_{INH}$ | | 2.0 | | | V |
| Input Low Voltage, $V_{INL}$ | | | | 0.8 | V |
| Input Current, $I_{INL}$ or $I_{INH}$ | $V_{IN}$ = 0 V to $V_{DD}$ | | 0.005 | ±1 | μA |
| Input Capacitance, $C_{IN}$ | | | 3 | | pF |
| SCL, SDA | | | | | |
| Input High Voltage, $V_{INH}$ | | 0.7 × $V_{DD}$ | | $V_{DD}$ + 0.3 | V |
| Input Low Voltage, $V_{INL}$ | | −0.3 | | +0.3 × $V_{DD}$ | V |
| Input Leakage Current, $I_{IN}$ | $V_{IN}$ = 0 V to $V_{DD}$ | | 0.005 | ±1 | μA |
| Input Hysteresis | | | 0.05 × $V_{DD}$ | | V |
| Input Capacitance, $C_{IN}$ | | | 3 | | pF |

OBSOLETE

| Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|
| LOGIC OUTPUTS[3] | | | | | |
| SDA Pin | | | | | |
| Output Low Voltage, $V_{OL}$ | $I_{SINK}$ = 3 mA | | | 0.4 | V |
| | $I_{SINK}$ = 6 mA | | | 0.6 | V |
| Floating-State Leakage Current | | | | ±1 | μA |
| Floating-State Output Capacitance | | | | 10 | pF |
| GPO1 Pin and GPO2 Pin | | | | | |
| Output Low Voltage, $V_{OL}$ | $I_{LOAD}$ = +2 mA | | | 0.4 | V |
| Output High Voltage, $V_{OH}$ | $I_{LOAD}$ = −2 mA | 2.0 | | | V |
| POWER REQUIREMENTS | | | | | |
| $I_{DD}$ | Digital inputs = 0 V or $V_{DD}$, $I^2C$ interface inactive | | 0.001 | 1 | μA |
| | $I^2C$ interface active, $f_{SCL}$ =400 kHz | | | 0.2 | mA |
| | $I^2C$ interface active, $f_{SCL}$ =3.4 MHz | | | 0.7 | mA |

[1]All typical values are at $T_A$ = 25°C, unless otherwise stated.
[2]Guaranteed by initial characterization, not subject to production test.
[3]Guaranteed by design, not subject to production test.

OBSOLETE

$V_{DD}$ = 3 V ± 10%, GND = 0 V, $T_A$ = −40°C to +85°C, unless otherwise noted.

**Table 2.**

| Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range[2] | $V_S$=$V_{DD}$, $R_L$=1MΩ | 0 | | 2.2 | V |
| | $V_S$=$V_{DD}$, $R_L$=75Ω | 0 | | 1.7 | V |
| On Resistance, $R_{ON}$ | $V_D$ = 0 V, $I_{DS}$ = −10 mA, see Figure 22 | | 2.2 | 4 | Ω |
| | $V_D$ = 0 V to 1 V, $I_{DS}$ = −10 mA, see Figure 22 | | | 6 | Ω |
| On-Resistance Matching Between Channels, $\Delta R_{ON}$ | $V_D$ = 0 V, $I_{DS}$ = −10 mA | | 0.15 | 0.6 | Ω |
| | $V_D$ = 1 V, $I_{DS}$ = −10 mA | | | 1.1 | Ω |
| On-Resistance Flatness, $R_{FLAT(ON)}$ | $V_D$ = 0 V to 1 V, $I_{DS}$ = −10 mA | | 0.3 | 2.8 | Ω |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage ($I_{S(OFF)}$) | $V_D$ = 2 V/1 V, $V_S$ = 1 V/2 V, see Figure 23 | | ±0.25 | | nA |
| Drain Off Leakage ($I_{D(OFF)}$) | $V_D$ = 2 V/1 V, $V_S$ = 1 V/2 V, see Figure 23 | | ±0.25 | | nA |
| Channel On Leakage ($I_{D(ON)}$, $I_{S(ON)}$) | $V_D$ = $V_S$ = 2 V/1 V, see Figure 24 | | ±0.25 | | nA |
| DYNAMIC CHARACTERISTICS[3] | | | | | |
| $t_{ON}$, $t_{ENABLE}$ | $C_L$ = 35 pF, $R_L$ = 50 Ω, $V_S$ = 2 V, see Figure 28 | | 198 | 270 | ns |
| $t_{OFF}$, $t_{DISABLE}$ | $C_L$ = 35 pF, $R_L$ = 50 Ω, $V_S$ = 2 V, see Figure 28 | | 195 | 260 | ns |
| Break-Before-Make Time Delay, $t_D$ | $C_L$ = 35 pF, $R_L$ = 50 Ω, $V_{S1}$ = $V_{S2}$ = 2 V, see Figure 29 | 1 | 3 | | ns |
| $I^2C$-to-GPO Propagation Delay, $t_H$, $t_L$ | ADG795G only | | | 121 | ns |
| Off Isolation | *f* = 10 MHz, $R_L$ = 50 Ω, see Figure 26 | | −60 | | dB |
| Channel-to-Channel Crosstalk | *f* = 10 MHz, $R_L$ = 50 Ω, see Figure 27 | | | | |
| Same Multiplexer | | | −55 | | dB |
| Different Multiplexer | | | −70 | | dB |
| −3 dB Bandwidth | $R_L$ = 50 Ω, see Figure 25 | | 310 | | MHz |
| THD + N | $R_L$ = 100 Ω | | 0.14 | | % |
| Charge Injection | $C_L$ = 1 nF, $V_S$ = 0 V, see Figure 30 | | 2.5 | | pC |
| $C_{S(OFF)}$ | | | 10 | | pF |
| $C_{D(OFF)}$ | | | 13 | | pF |
| $C_{D(ON)}$, $C_{S(ON)}$ | | | 27 | | pF |
| Power Supply Rejection Ratio, PSRR | *f* = 20 kHz | | 70 | | dB |
| Differential Gain Error | CCIR330 test signal | | 0.28 | | % |
| Differential Phase Error | CCIR330 test signal | | 0.28 | | Degrees |
| LOGIC INPUTS[3] | | | | | |
| A0, A1, A2 | | | | | |
| Input High Voltage, $V_{INH}$ | | 2.0 | | | V |
| Input Low Voltage, $V_{INL}$ | | | | 0.8 | V |
| Input Current, $I_{INL}$ or $I_{INH}$ | $V_{IN}$ = 0 V to $V_{DD}$ | | 0.005 | ±1 | μA |
| Input Capacitance, $C_{IN}$ | | | 3 | | pF |
| SCL, SDA | | | | | |
| Input High Voltage, $V_{INH}$ | | 0.7 × $V_{DD}$ | | $V_{DD}$ + 0.3 | V |
| Input Low Voltage, $V_{INL}$ | | −0.3 | | +0.3 × $V_{DD}$ | V |
| Input Leakage Current, $I_{IN}$ | $V_{IN}$ = 0 V to $V_{DD}$ | | 0.005 | ±1 | μA |
| Input Hysteresis | | | 0.05 × $V_{DD}$ | | V |
| Input Capacitance, $C_{IN}$ | | | 3 | | pF |

OBSOLETE

| Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|
| LOGIC OUTPUTS[3] | | | | | |
| SDA Pin | | | | | |
| Output Low Voltage, $V_{OL}$ | $I_{SINK}$ = 3 mA | | | 0.4 | V |
| | $I_{SINK}$ = 6 mA | | | 0.6 | V |
| Floating-State leakage Current | | | | ±1 | µA |
| Floating-State Output Capacitance | | | 3 | | pF |
| GPO1 Pin and GPO2 Pin | | | | | |
| Output Low Voltage, $V_{OL}$ | $I_{LOAD}$ = +2 mA | | | 0.4 | V |
| Output High Voltage, $V_{OH}$ | $I_{LOAD}$ = −2 mA | 2.0 | | | V |
| POWER REQUIREMENTS | | | | | |
| $I_{DD}$ | Digital inputs = 0 V or $V_{DD}$, $I^2C$ interface inactive | | 0.001 | 1 | µA |
| | $I^2C$ interface active, $f_{SCL}$ = 400 kHz | | | 0.1 | mA |
| | $I^2C$ interface active, $f_{SCL}$ = 3.4 MHz | | | 0.2 | mA |

[1]All typical values are at $T_A$ = 25°C, unless otherwise stated.
[2]Guaranteed by initial characterization, not subject to production test.
[3]Guaranteed by design, not subject to production test.

OBSOLETE

# I²C TIMING SPECIFICATIONS

$V_{DD}$ = 2.7 V to 5.5 V; GND = 0 V; $T_A$ = −40°C to +85°C, unless otherwise noted. See Figure 2 for timing diagram.

**Table 3.**

| Parameter[1] | Conditions | Min | Max | Unit | Description |
|---|---|---|---|---|---|
| $f_{SCL}$ | Standard mode | | 100 | kHz | Serial clock frequency |
| | Fast mode | | 400 | kHz | |
| | High speed mode | | | | |
| | $C_B$ = 100 pF max | | 3.4 | MHz | |
| | $C_B$ = 400 pF max | | 1.7 | MHz | |
| $t_1$ | Standard mode | 4 | | µs | $t_{HIGH}$, SCL high time |
| | Fast mode | 0.6 | | µs | |
| | High speed mode | | | | |
| | $C_B$ = 100 pF max | 60 | | ns | |
| | $C_B$ = 400 pF max | 120 | | ns | |
| $t_2$ | Standard mode | 4.7 | | µs | $t_{LOW}$, SCL low time |
| | Fast mode | 1.3 | | µs | |
| | High speed mode | | | | |
| | $C_B$ = 100 pF max | 160 | | ns | |
| | $C_B$ = 400 pF max | 320 | | ns | |
| $t_3$ | Standard mode | 250 | | ns | $t_{SU;DAT}$, data setup time |
| | Fast mode | 100 | | ns | |
| | High speed mode | 10 | | ns | |
| $t_4$[2] | Standard mode | 0 | 3.45 | µs | $t_{HD;DAT}$, data hold time |
| | Fast mode | 0 | 0.9 | µs | |
| | High speed mode | | | | |
| | $C_B$ = 100 pF max | 0 | 703 | ns | |
| | $C_B$ = 400 pF max | 0 | 150 | ns | |
| $t_5$ | Standard mode | 4.7 | | µs | $t_{SU;STA}$, setup time for a repeated start condition |
| | Fast mode | 0.6 | | µs | |
| | High speed mode | 160 | | ns | |
| $t_6$ | Standard mode | 4 | | µs | $t_{HD;STA}$, hold time (repeated) start condition |
| | Fast mode | 0.6 | | µs | |
| | High speed mode | 160 | | ns | |
| $t_7$ | Standard mode | 4.7 | | µs | $t_{BUF}$, bus free time between a stop and a start condition |
| | Fast mode | 1.3 | | µs | |
| $t_8$ | Standard mode | 4 | | µs | $t_{SU;STO}$, setup time for stop condition |
| | Fast mode | 0.6 | | µs | |
| | High speed mode | 160 | | ns | |
| $t_9$ | Standard mode | | 1000 | ns | $t_{RDA}$, rise time of SDA signal |
| | Fast mode | 20 + 0.1 $C_B$ | 300 | ns | |
| | High speed mode | | | | |
| | $C_B$ = 100 pF max | 10 | 80 | ns | |
| | $C_B$ = 400 pF max | 20 | 160 | ns | |
| $t_{10}$ | Standard mode | | 300 | ns | $t_{FDA}$, fall time of SDA signal |
| | Fast mode | 20 + 0.1 $C_B$ | 300 | ns | |
| | High speed mode | | | | |
| | $C_B$ = 100 pF max | 10 | 80 | ns | |
| | $C_B$ = 400 pF max | 20 | 160 | ns | |

OBSOLETE

| Parameter[1] | Conditions | Min | Max | Unit | Description |
|---|---|---|---|---|---|
| $t_{11}$ | Standard mode | | 1000 | ns | $t_{RCL}$, rise time of SCL signal |
| | Fast mode | 20 + 0.1 $C_B$ | 300 | ns | |
| | High speed mode | | | | |
| | $C_B$ = 100 pF max | 10 | 40 | ns | |
| | $C_B$ = 400 pF max | 20 | 80 | ns | |
| $t_{11A}$ | Standard mode | | 1000 | ns | $t_{RCL1}$, rise time of SCL signal after a repeated start condition and after an acknowledge bit |
| | Fast mode | 20 + 0.1 $C_B$ | 300 | ns | |
| | High speed mode | | | | |
| | $C_B$ = 100 pF max | 10 | 80 | ns | |
| | $C_B$ = 400 pF max | 20 | 160 | ns | |
| $t_{12}$ | Standard mode | | 300 | ns | $t_{FCL}$, fall time of SCL signal |
| | Fast mode | 20 + 0.1 $C_B$ | 300 | ns | |
| | High speed mode | | | | |
| | $C_B$ = 100 pF max | 10 | 40 | ns | |
| | $C_B$ = 400 pF max | 20 | 80 | ns | |
| $t_{SP}$ | Fast mode | 0 | 50 | ns | Pulse width of suppressed spike |
| | High speed mode | 0 | 10 | ns | |

[1]Guaranteed by initial characterization. CB refers to capacitive load on the bus line, tr and tf measured between 0.3 $V_{DD}$ and 0.7 $V_{DD}$.
[2]A device must provide a data hold time for SDA in order to bridge the undefined region of the SCL falling edge.

## TIMING DIAGRAM

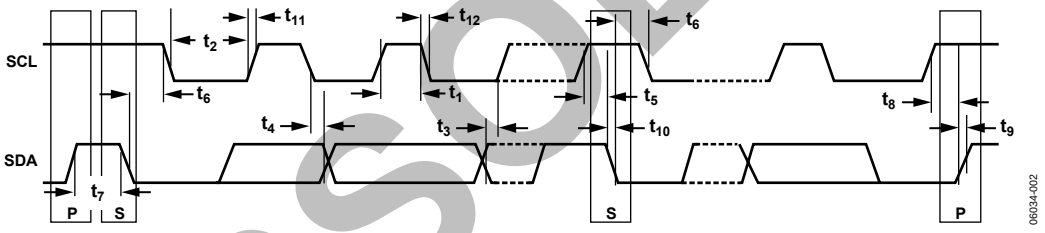



*Figure 2. Timing Diagram for 2-Wire Serial Interface*

OBSOLETE

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 4.**

| Parameters | Ratings |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +6 V |
| Analog, Digital Inputs | −0.3 V to $V_{DD}$ + 0.3 V or 30 mA, whichever occurs first |
| Continuous Current, S or D | 100 mA |
| Peak Current, S or D | 300 mA (pulsed at 1 ms, 10% duty cycle max) |
| Operating Temperature Range | |
| Industrial (B Version) | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| $\theta_{JA}$ Thermal Impedance | |
| 24-Lead LFCSP | 30°C/W |
| Lead Temperature, Soldering (10 sec) | 300°C |
| IR Reflow, Peak Temperature (<20 sec) | 260°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

OBSOLETE

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

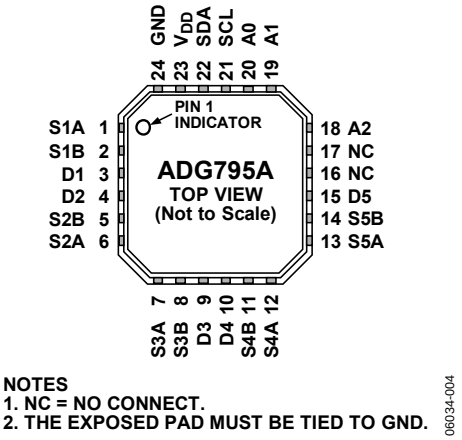



*Figure 3. ADG795G Pinout*

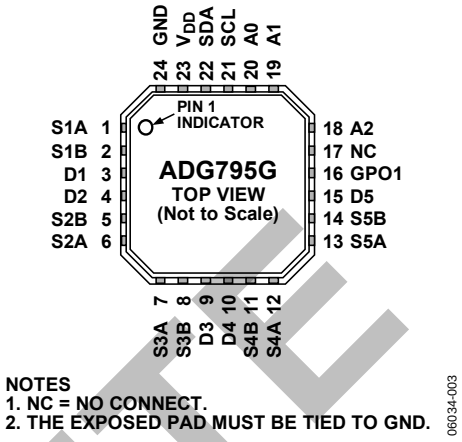



*Figure 4. ADG795A Pinout*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | S1A | A-Side Source Terminal for Mux 1. Can be an input or output. |
| 2 | S1B | B-Side Source Terminal for Mux 1. Can be an input or output. |
| 3 | D1 | Drain Terminal for Mux 1. Can be an input or output. |
| 4 | D2 | Drain Terminal for Mux 2. Can be an input or output. |
| 5 | S2B | B-Side Source Terminal for Mux 2. Can be an input or output. |
| 6 | S2A | A-Side Source Terminal for Mux 2. Can be an input or output. |
| 7 | S3A | A-Side Source Terminal for Mux 3. Can be an input or output. |
| 8 | S3B | B-Side Source Terminal for Mux 3. Can be an input or output. |
| 9 | D3 | Drain Terminal for Mux 3. Can be an input or output. |
| 10 | D4 | Drain Terminal for Mux 4. Can be an input or output. |
| 11 | S4B | B-Side Source Terminal for Mux 4. Can be an input or output. |
| 12 | S4A | A-Side Source Terminal for Mux 4. Can be an input or output. |
| 13 | S5A | A-Side Source Terminal for Mux 5. Can be an input or output |
| 14 | S5B | B-Side Source Terminal for Mux 5. Can be an input or output |
| 15 | D5 | Drain Terminal for Mux 5. Can be an input or output. |
| 16 | NC/GPO1 | Not internally connected for ADG795A/General Purpose Logic Output 1 for ADG795G. |
| 17 | NC | Not internally connected. |
| 18 | A2 | Logic Input. Sets Bit A2 from the least significant bit of the 7-bit slave address. |
| 19 | A1 | Logic Input. Sets Bit A1 from the least significant bit of the 7-bit slave address. |
| 20 | A0 | Logic Input. Sets Bit A0 from the least significant bit of the 7-bit slave address. |
| 21 | SCL | Digital Input, Serial Clock Line. Open-drain input that is used in conjunction with SDA to clock data into the device. External pull-up resistor required. |
| 22 | SDA | Digital I/O. Bi-directional open-drain data line. External pull-up resistor required. |
| 23 | $V_{DD}$ | Positive Power Supply Input. |
| 24 | GND | Ground (0 V) Reference. |

OBSOLETE

# TYPICAL PERFORMANCE CHARACTERISTICS

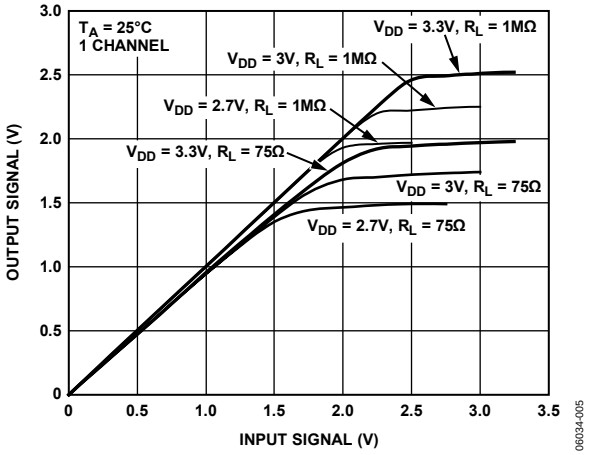



Figure 5. Analog Signal Range, 3 V Supply

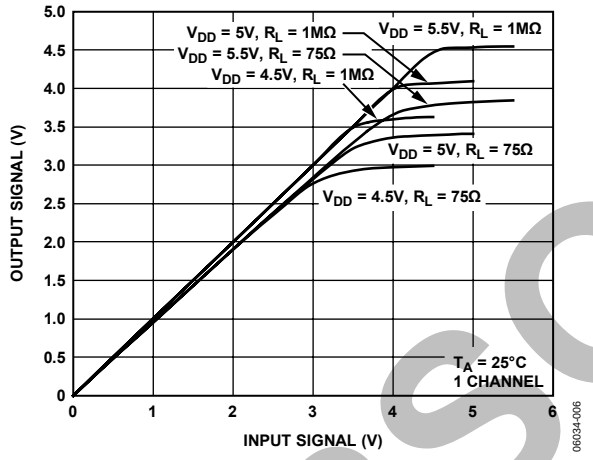



Figure 6. Analog Signal Range, 5 V Supply

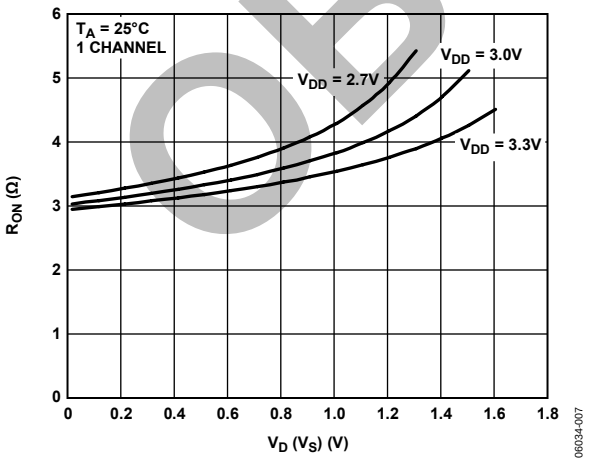



Figure 7. On Resistance vs. $V_D$ ($V_S$), 3 V Supply

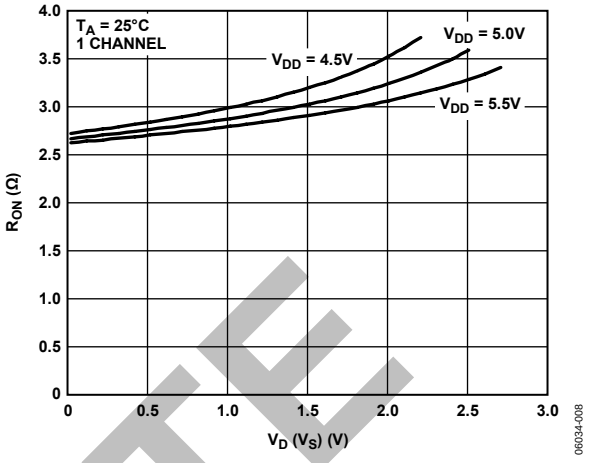



Figure 8. On Resistance vs. $V_D$ ($V_S$), 5 V Supply

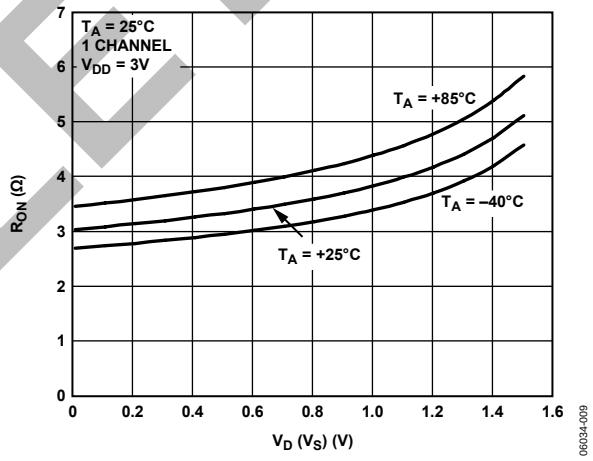



Figure 9. On Resistance vs. $V_D$ ($V_S$) for Various Temperatures, 3 V Supply

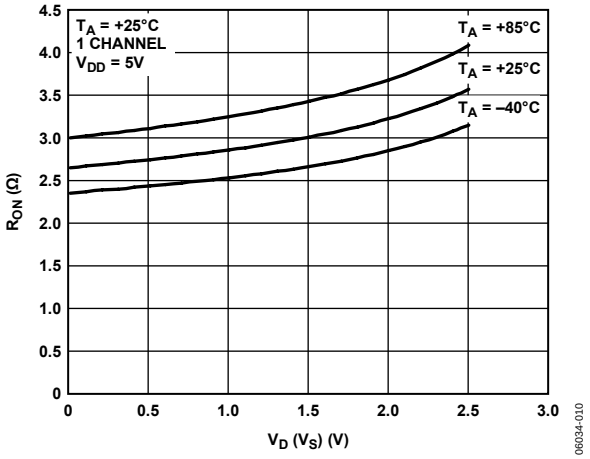



Figure 10. On Resistance vs. $V_D$ ($V_S$) for Various Temperatures, 5 V Supply

OBSOLETE

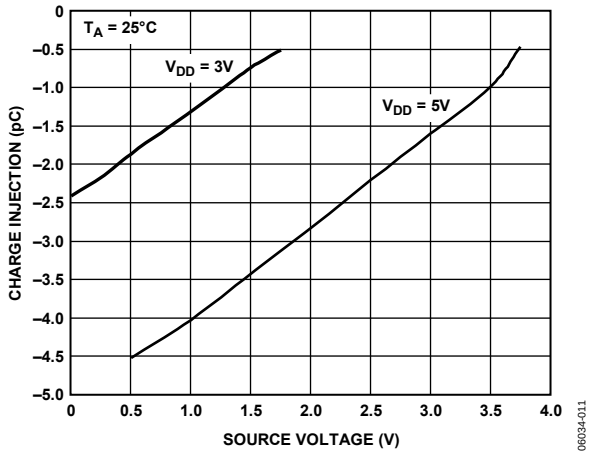



Figure 11. Charge Injection vs. Source Voltage

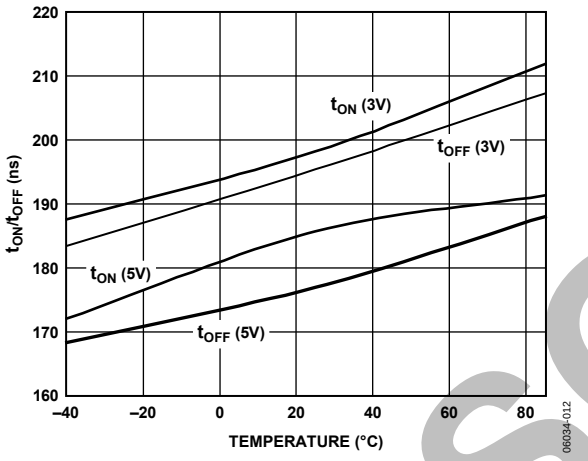



Figure 12. $t_{ON}/t_{OFF}$ vs. Temperature

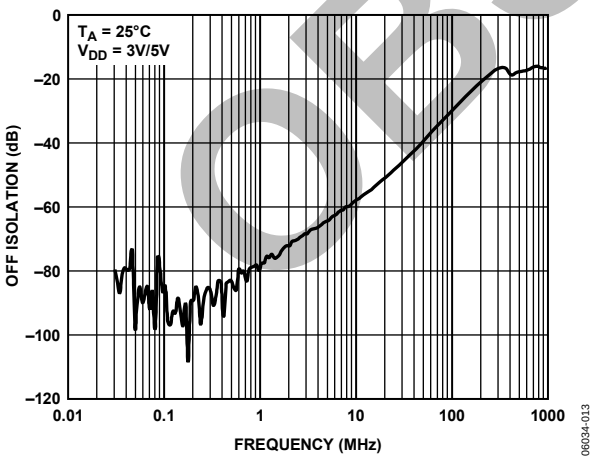



Figure 13. Off Isolation vs. Frequency

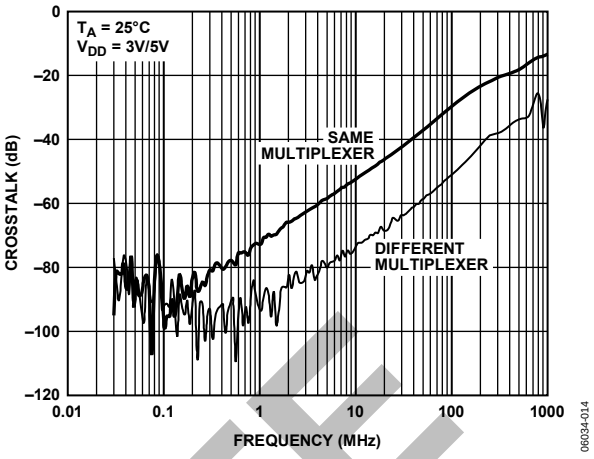



Figure 14. Crosstalk vs. Frequency

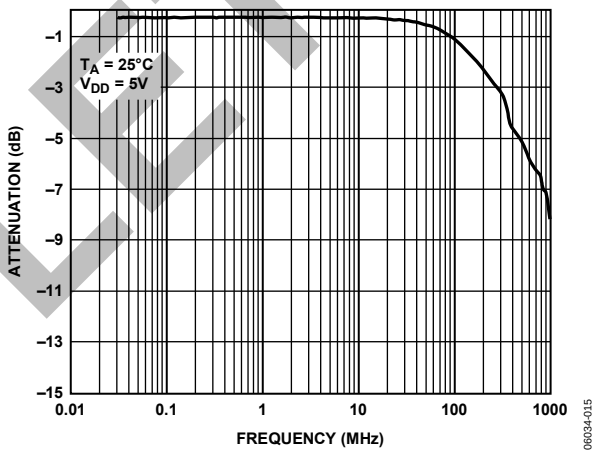



Figure 15. Bandwidth

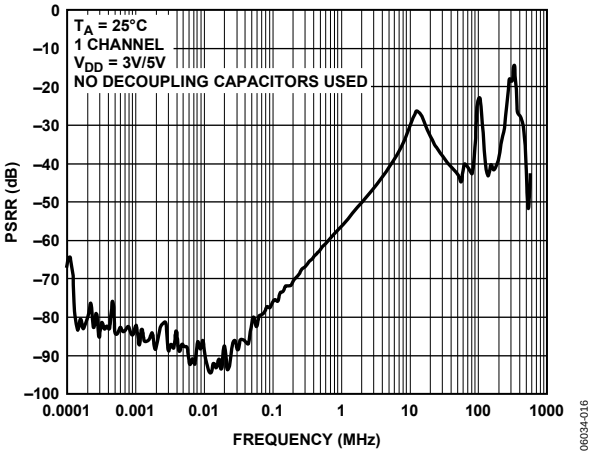



Figure 16. PSRR vs. Frequency

OBSOLETE

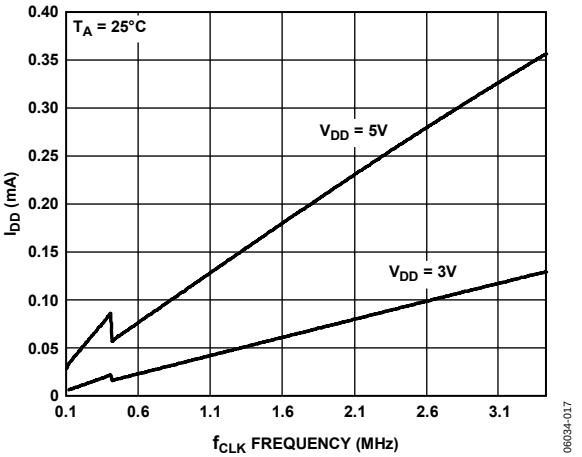



*Figure 17. $I_{DD}$ vs. $f_{CLK}$ Frequency*

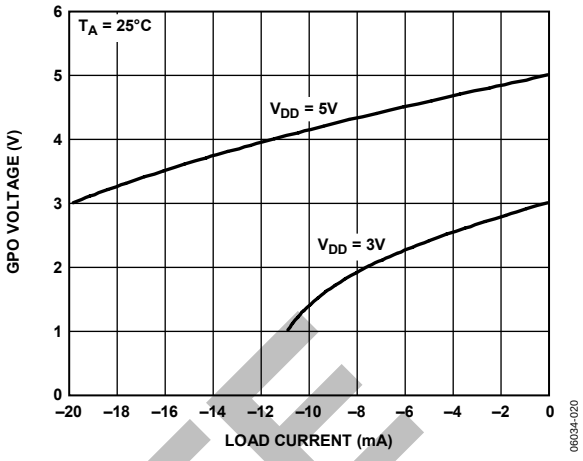



*Figure 20. GPO $V_{OH}$ vs. Load Current*

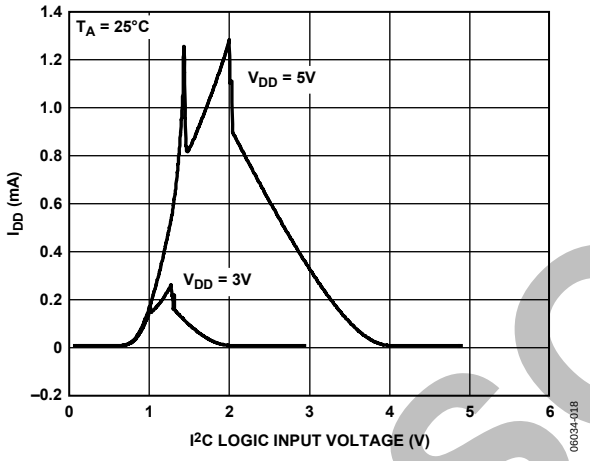



*Figure 18. $I_{DD}$ vs. $I^2C$ Logic Input Voltage (SDA, SCL)*

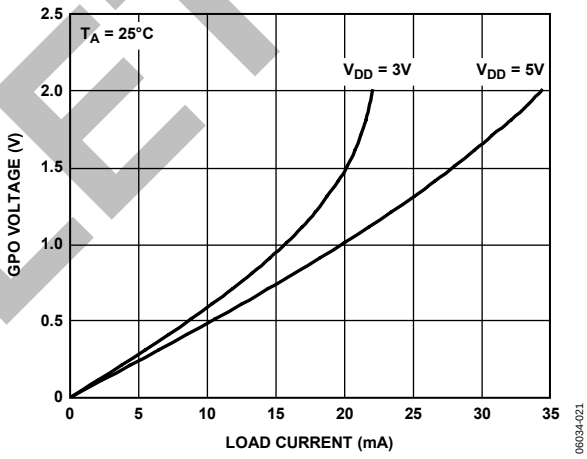



*Figure 21. GPO $V_{OL}$ vs. Load Current*

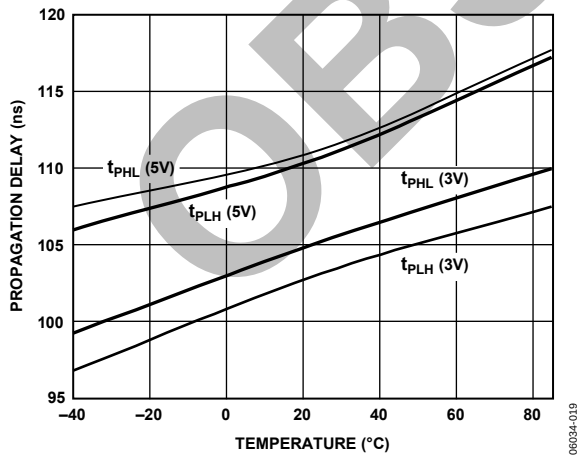



*Figure 19. $I^2C$ to GPO Propagation Delay vs. Temperature*

OBSOLETE

# TEST CIRCUITS

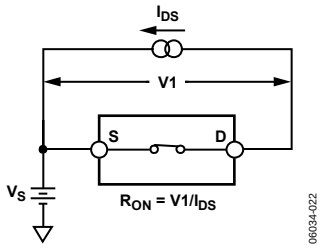



Figure 22. On Resistance

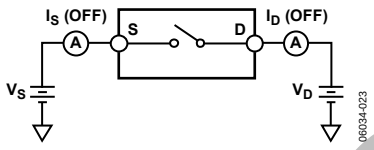



Figure 23. Off Leakage

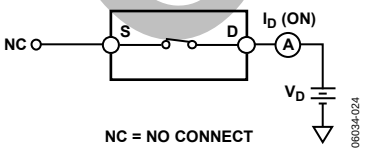



Figure 24. On Leakage

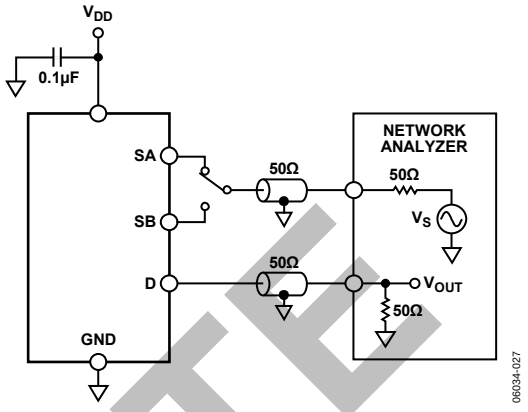



Figure 25. Bandwidth

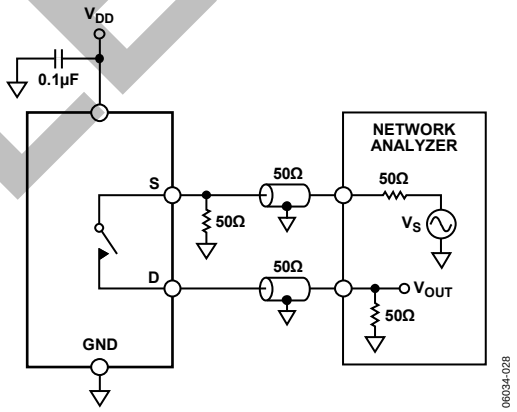



Figure 26. Off Isolation

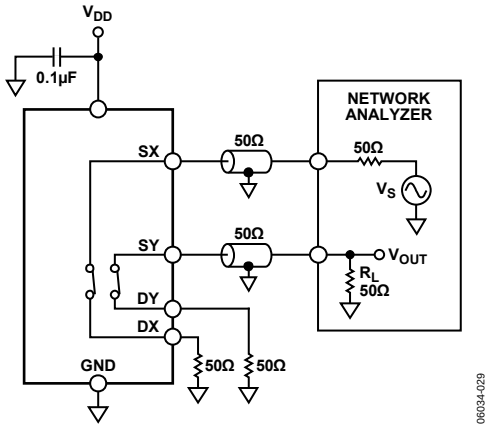



Figure 27. Channel-to-Channel Crosstalk

OBSOLETE

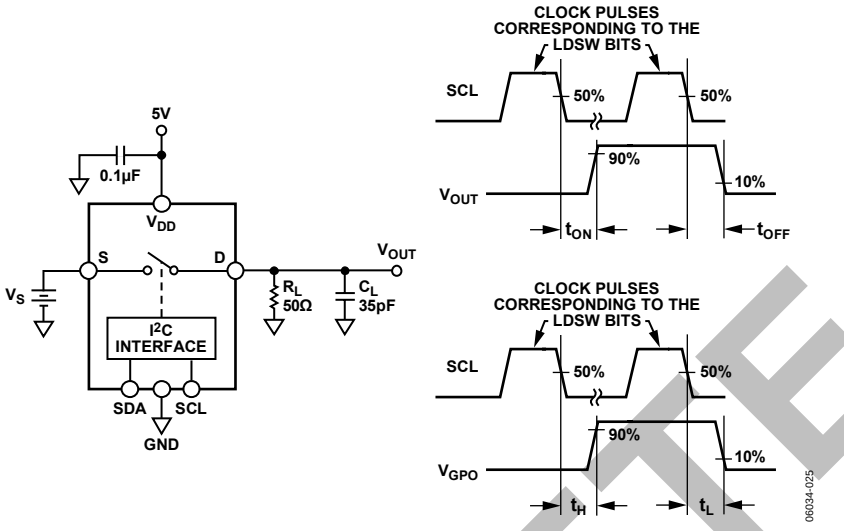



*Figure 28. Switching Times*

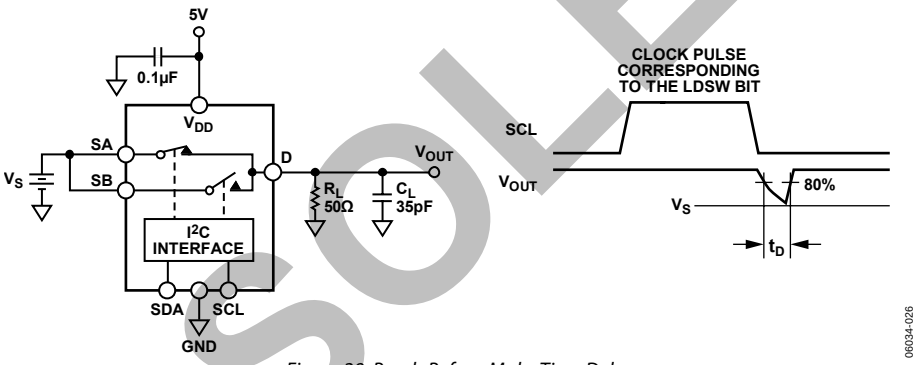



*Figure 29. Break-Before-Make Time Delay*

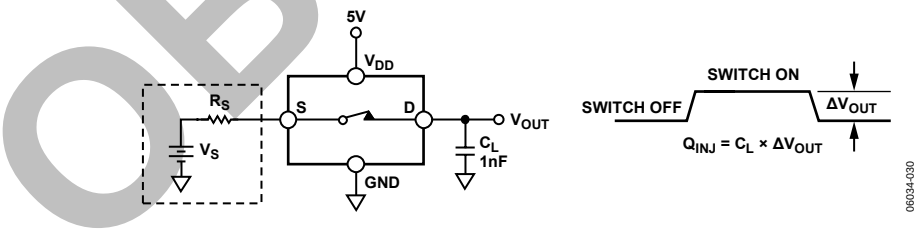



*Figure 30. Charge Injection*

OBSOLETE

# TERMINOLOGY

**On Resistance ($R_{ON}$)**
The series on-channel resistance measured between the S pin and D pin.

**On Resistance Match ($\Delta R_{ON}$)**
The channel-to-channel matching of on resistance when channels are operated under identical conditions.

**On Resistance Flatness ($R_{FLAT(ON)}$)**
The variation of on resistance over the specified range produced by the specified analog input voltage change with a constant load current.

**Channel Off Leakage ($I_{OFF}$)**
The sum of leakage currents into or out of an off channel input.

**Channel On Leakage ($I_{ON}$)**
The current loss/gain through an on-channel resistance, creating a voltage offset across the device.

**Input Leakage Current ($I_{IN}$, $I_{INL}$, $I_{INH}$)**
The current flowing into a digital input when a specified low level or high level voltage is applied to that input.

**Input/Output Off Capacitance ($C_{OFF}$)**
The capacitance between an analog input and ground when the switch channel is off.

**Input/Output On Capacitance ($C_{ON}$)**
The capacitance between the inputs or outputs and ground when the switch channel is on.

**Digital Input Capacitance ($C_{IN}$)**
The capacitance between a digital input and ground.

**Output On Switching Time ($t_{ON}$)**
The time required for the switch channel to close. The time is measured from 50% of the falling edge of the LDSW bit to the time the output reaches 90% of the final value.

**Output Off Switching Time ($t_{OFF}$)**
The time required for the switch to open. The time is measured from 50% of the falling edge of the LDSW bit to the time the output reaches 10% of the final value.

**$I^2C$ to GPO propagation delay ($t_H$, $t_L$)**
The time required for the logic value at the GPO pin to settle after loading a GPO command. The time is measured from 50% of the falling edge of the LDSW bit to the time the output reaches 90% of the final value for high and 10% for low.

**Total Harmonic Distortion + Noise (THD + N)**
The ratio of the harmonic amplitudes plus noise of a signal to the fundamental.

**−3 dB Bandwidth**
The frequency at which the output is attenuated by 3 dB.

**Off Isolation**
The measure of unwanted signal coupling through an off switch.

**Crosstalk**
The measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

**Charge Injection**
The measure of the glitch impulse transferred from the digital input to the analog output during on/off switching.

**Differential Gain Error**

The measure of how much color saturation shift occurs when the luminance level changes. Both attenuation and amplification can occur; therefore, the largest amplitude change between any two levels is specified and expressed in percent (%).

**Differential Phase Error**

The measure of how much hue shift occurs when the luminance level changes. It can be a negative or positive value and is expressed in degrees of subcarrier phase.

**Input High Voltage ($V_{INH}$)**
The minimum input voltage for Logic 1.

**Input Low Voltage ($V_{INL}$)**
The maximum input voltage for Logic 0.

**Output High Voltage ($V_{OH}$)**
The minimum output voltage for Logic 1.

**Output Low Voltage ($V_{OL}$)**
The maximum output voltage for Logic 0.

**$I_{DD}$**
Positive supply current.

OBSOLETE

# THEORY OF OPERATION

The ADG795A/ADG795G are monolithic CMOS devices comprising five 2:1 multiplexers controllable via a standard I²C serial interface. The CMOS process provides ultralow power dissipation, yet offers high switching speed and low on resistance.

The on resistance profile is very flat over the full analog input range, and wide bandwidth ensures excellent linearity and low distortion. These features, combined with a wide input signal range, make the ADG795A/ADG795G an ideal switching solution for a wide range of TV applications.

The switches conduct equally well in both directions when on. In the off condition, signal levels up to the supplies are blocked. The integrated serial I²C interface controls the operation of the switches (ADG795A/ADG795G) and general-purpose logic pins (ADG795G only).

The ADG795A/ADG795G have many attractive features, such as the ability to individually control each multiplexer, the option of reading back the status of any switch. The ADG795G has one general-purpose logic output pin controllable through the I²C interface. The following sections describe these features in detail.

## I²C SERIAL INTERFACE

The ADG795A/ADG795G are controlled via an I²C-compatible serial bus interface (refer to the *I²C-Bus Specification* available from Philips Semiconductor) that allows the part to operate as a slave device (no clock is generated by the ADG795A/ADG795G). The communication protocol between the I²C master and the device operates as follows:

1. The master initiates data transfer by establishing a start condition (defined as a high-to-low transition on the SDA line while SCL is high). This indicates that an address/data stream follows. All slave devices connected to the bus respond to the start condition and shift in the next eight bits, consisting of a seven bit address (MSB first) plus an R/$\overline{W}$ bit. This bit determines the direction of the data flow during the communication between the master and the addressed slave device.

2. The slave device whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is called the acknowledge bit).

   At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its serial register. If the R/$\overline{W}$ bit is set high, the master reads from the slave device. However, if the R/$\overline{W}$ bit is set low, the master writes to the slave device.

3. Data transmits over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of the clock signal, SCL, and remain stable during the high period of SCL. Otherwise, a low-to-high transition when the clock signal is high can be interpreted as a stop event that ends the communication between the master and the addressed slave device.

4. After transferring all data bytes, the master establishes a stop condition, defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10$^{th}$ clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the ninth clock pulse (the SDA line remains high). The master then brings the SDA line low before the 10$^{th}$ clock pulse, and then high during the 10$^{th}$ clock pulse to establish a stop condition.

## I²C ADDRESS

The ADG795A/ADG795G have a 7-bit I²C address. The four most significant bits are internally hardwired and last three bits (A0, A1, and A2) are user-adjustable. This allows the user to connect up to eight ADG795As/ADG795Gs to the same bus. The I²C bit map shows the configuration of the 7-bit address.

***7-Bit I²C Address Configuration***

| MSB | | | | | | LSB |
|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | A2 | A1 | A0 |

## WRITE OPERATION

When writing to the ADG795A/ADG795G, the user must begin with an address byte and R/$\overline{W}$ bit, after which time the switch acknowledges that it is prepared to receive data by pulling SDA low. Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCL. Figure 31 illustrates the entire write sequence for the ADG795A/ADG795G. The first data byte (AX7 to AX0) controls the status of the switches while the LDSW and RESETB bits from the second byte control the operation mode of the device. Table 6 shows a list of all commands supported by the ADG795A/ADG795G with the corresponding byte that needs to be loaded during a write operation.

To achieve the desired configuration, one or more commands can be loaded into the device. Any combination of the commands in Table 6 can be used with these restrictions:

- Only one switch from a given multiplexer can be on at any given time.
- When a sequence of successive commands affect the same element (that is, the switch or GPO pin), only the last command is executed.

OBSOLETE

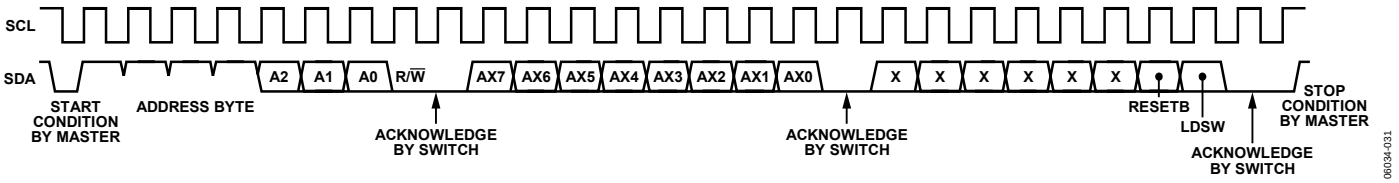



*Figure 31. Write Operation*

**Table 6. ADG795A/ADG795G Command List**

| AX7 | AX6 | AX5 | AX4 | AX3 | AX2 | AX1 | AX0 | Addressed Switch |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | S1A/D1, S2A/D2, S3A/D3, S4A/D4, S5A/D5 off |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | S1A/D1, S2A/D2, S3A/D3, S4A/D4, S5A/D5 on |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | S1B/D1, S2B/D2, S3B/D3, S4B/D4, S5B/D5 off |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | S1B/D1, S2B/D2, S3B/D3, S4B/D4, S5B/D5 on |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | S1A/D1 off |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | S1A/D1 on |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | S1B/D1 off |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | S1B/D1 on |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | S2A/D2 off |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | S2A/D2 on |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | S2B/D2 off |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | S2B/D2 on |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | S3A/D3 off |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | S3A/D3 on |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | S3B/D3 off |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | S3B/D3 on |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | S4A/D4 off |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | S4A/D4 on |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | S4B/D4 off |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | S4B/D4 on |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | S5A/D5 off |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | S5A/D5 on |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | S5B/D5 off |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | S5B/D5 on |
| X[1] | 0 | 0 | 0 | 1 | 1 | 0 | 0 | Reserved |
| X[1] | 0 | 0 | 0 | 1 | 1 | 0 | 1 | Reserved |
| X[1] | 0 | 0 | 0 | 1 | 1 | 1 | 0 | Mux 1 disabled (all switches connected to D1 are off) |
| X[1] | 0 | 0 | 0 | 1 | 1 | 1 | 1 | Mux 2 disabled (all switches connected to D2 are off) |
| X[1] | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Mux 3 disabled (all switches connected to D3 are off) |
| X[1] | 0 | 0 | 1 | 0 | 0 | 0 | 1 | Mux 4 disabled (all switches connected to D4 are off) |
| X[1] | 0 | 0 | 1 | 0 | 0 | 1 | 0 | Mux 5 disabled (all switches connected to D5 are off) |
| X[1] | 0 | 0 | 1 | 0 | 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | GPO1 high for ADG795G/reserved for ADG795A |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | GPO1 low for ADG795G/reserved for ADG795A |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | All muxes disabled |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | Reserved |

[1]X = Logic state does not matter.

OBSOLETE

## LDSW BIT

The LDSW bit allows the user to control the way the device executes the commands loaded during the write operations. The ADG795A/ADG795G execute all the commands loaded between two successive write operations that have set the LDSW bit high.

Setting the LDSW high for every write cycle ensures that the device executes the command right after the LDSW bit was loaded into the device. This setting can be used when the desired configuration can be achieved by sending a single command or when the switches and/or GPO pin are not required to be updated at the same time. When the desired configuration requires multiple commands with simultaneous updated, the LDSW bit should be set low while loading the commands (except the last one when the LDSW bit should be set high). Once the last command with LDSW = high is loaded, the device executes all commands received since the last update simultaneously.

## POWER ON/SOFTWARE RESET

The ADG795A/ADG795G has a software reset function implemented by the RESETB bit from the second data byte written to the device. For normal operation of the multiplexers and GPO pin, this bit should be set high. When RESETB = low or after power-up, the switches from all multiplexers are turned off (open) and the GPO pin is set low.

## READ OPERATION

When reading data back from the ADG795A/ADG795G, the user must begin with an address byte and R/$\overline{W}$ bit. The switch then acknowledges that it is prepared to transmit data by pulling SDA low. Following this acknowledgement, the ADG795A/ADG795G transmit two bytes on the next clock edges. These bytes contain the status of the switches, and each byte is followed by an acknowledge bit. A logic high bit represents a switch in the on (close) state while a low represents a switch in the off (open) state. For the GPO pin (ADG795G only), the bit represents the logic value of the pin. Figure 32 illustrates the entire read sequence.

The bit maps accompanying Figure 32 show the relationship between the elements of the ADG795A and ADG795G (that it, the switches and GPO pins) and the bits that represent their status after a completed read operation.

OBSOLETE

***Bit Map of the ADG795A***

| RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S1A/D1 | S1B/D1 | S2A/D2 | S2B/D2 | S3A/D3 | S3B/D3 | S4A/D4 | S4B/D4 | S5A/D5 | S5B/D5 | - | - | - | - | - | - |

***Bit Map of the ADG795G***

| RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S1A/D1 | S1B/D1 | S2A/D2 | S2B/D2 | S3A/D3 | S3B/D3 | S4A/D4 | S4B/D4 | S5A/D5 | S5B/D5 | - | - | GPO1 | - | - | - |

***Read Operation***

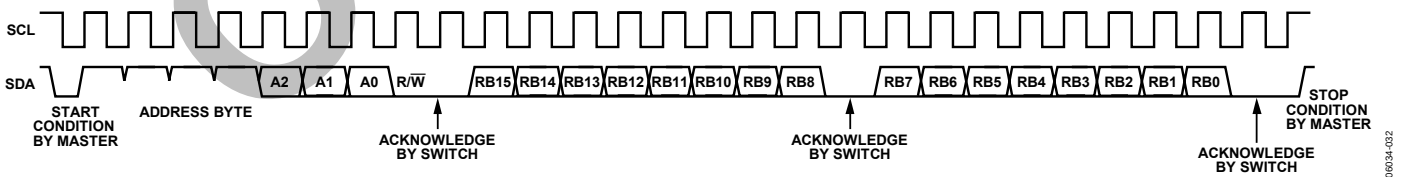



*Figure 32. ADG795A/ADG795G Read Operation*

# EVALUATION BOARD

The ADG795G evaluation kit allows designers to evaluate the high performance of the device with a minimum of effort.

The evaluation kit includes a printed circuit board populated with the ADG795G. The evaluation board can be used to evaluate the performance of both the ADG795A and ADG795G. It interfaces to the USB port of a PC, or it can be used as a standalone evaluation board.

Software for the evaluation board allows the user to program the ADG795G easily through the USB port. The software runs on any PC that has Microsoft® Windows® 2000 or Windows XP installed with a minimum screen resolution of 1200 × 768. See Figure 33 and Figure 34 for schematics of the evaluation board.

## USING THE ADG795G EVALUATION BOARD

The ADG795G evaluation kit is a test system designed to simplify the evaluation of the device. Each input/output of the part comes with a socket specifically chosen for easy audio/video evaluation. An evaluation board data sheet is also available and provides full instructions for operating the evaluation board.

OBSOLETE

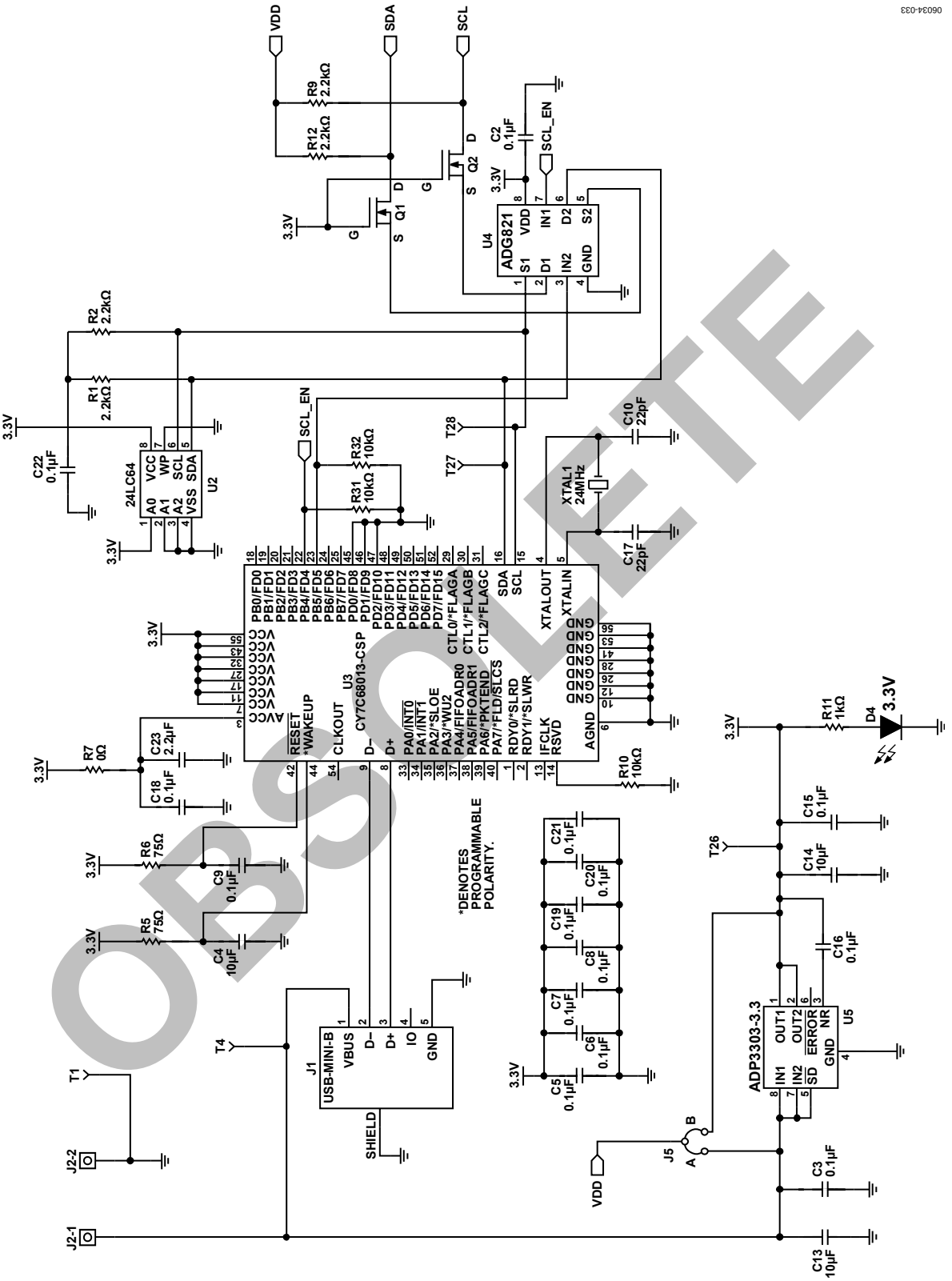
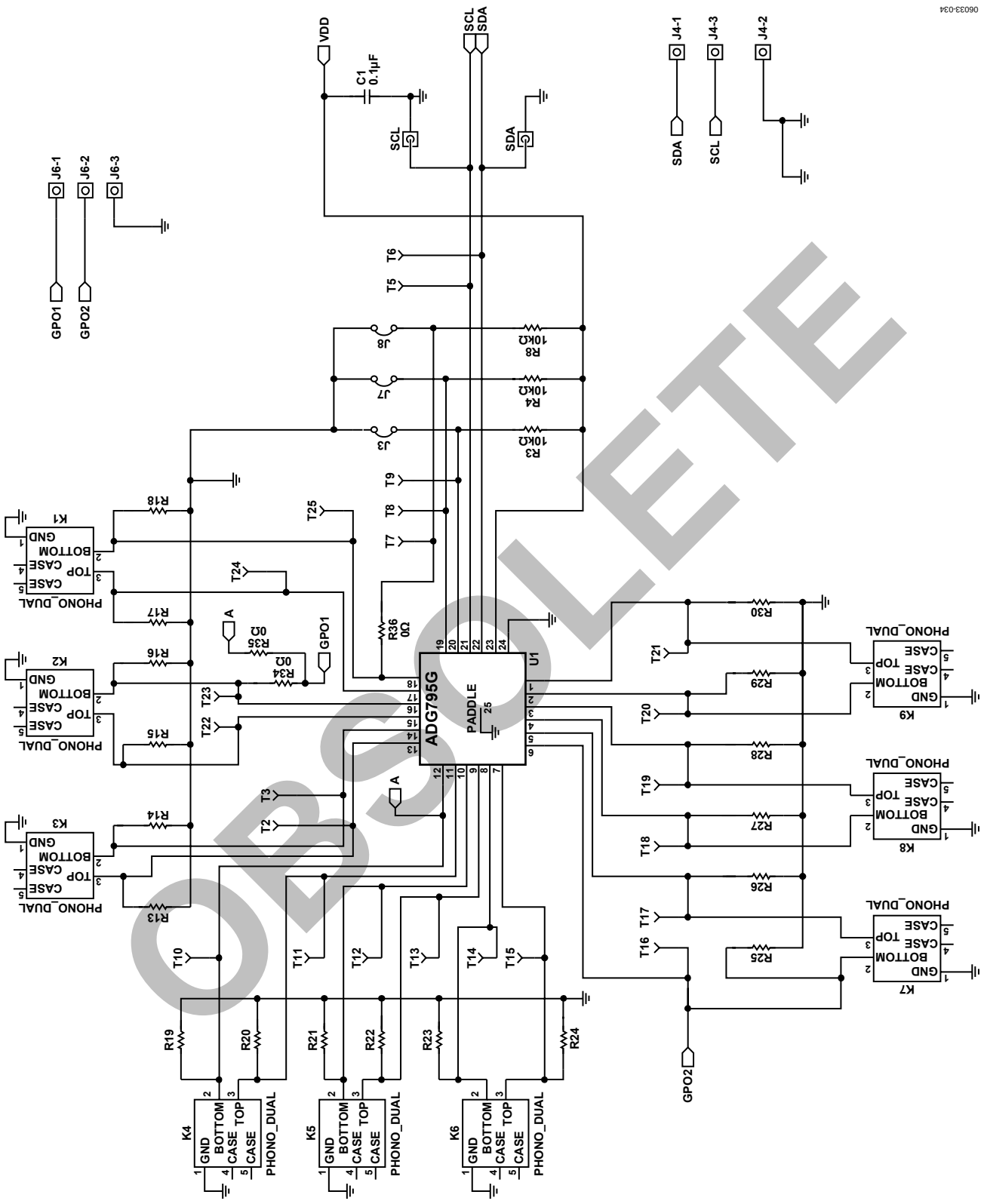



*Figure 33. Eval-ADG795GEB Schematic, USB Controller Section*

OBSOLETE




OBSOLETE

*Figure 34. Eval-ADG795GEB Schematic, Chip Section*

# OUTLINE DIMENSIONS

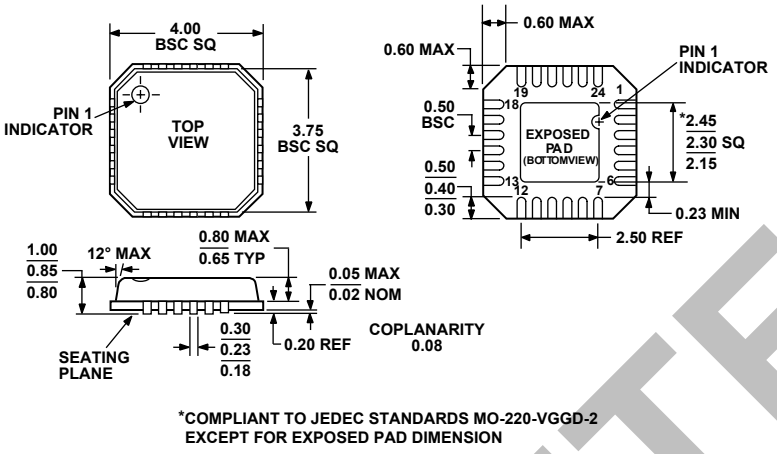



*Figure 35. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]*
*4 mm x 4 mm Body, Very Thin Quad*
*(CP-24-2)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | I²C Speed | Package Description | Package Option |
|---|---|---|---|---|
| ADG795ABCPZ-REEL[1] | −40°C to +85°C | 100 kHz, 400 kHz | 24-Lead LFCSP_VQ | CP-24-2 |
| ADG795ABCPZ-500RL7[1] | −40°C to +85°C | 100 kHz, 400 kHz | 24-Lead LFCSP_VQ | CP-24-2 |
| ADG795ACCPZ-REEL[1] | −40°C to +85°C | 100 kHz, 400 kHz, 3.4 MHz | 24-Lead LFCSP_VQ | CP-24-2 |
| ADG795ACCPZ-500RL7[1] | −40°C to +85°C | 100 kHz, 400 kHz, 3.4 MHz | 24-Lead LFCSP_VQ | CP-24-2 |
| ADG795GBCPZ-REEL[1] | −40°C to +85°C | 100 kHz, 400 kHz | 24-Lead LFCSP_VQ | CP-24-2 |
| ADG795GBCPZ-500RL7[1] | −40°C to +85°C | 100 kHz, 400 kHz | 24-Lead LFCSP_VQ | CP-24-2 |
| ADG795GCCPZ-REEL[1] | −40°C to +85°C | 100 kHz, 400 kHz, 3.4 MHz | 24-Lead LFCSP_VQ | CP-24-2 |
| ADG795GCCPZ-500RL7[1] | −40°C to +85°C | 100 kHz, 400 kHz, 3.4 MHz | 24-Lead LFCSP_VQ | CP-24-2 |
| EVAL-ADG795GEB[2] | | | Evaluation Board | |

[1] Z = Pb-free part.
[2] Evaluation board is RoHS compliant.

OBSOLETE

## NOTES

OBSOLETE

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

**©2006 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.**
**D06034-0-7/06(0)**

ANALOG DEVICES

www.analog.com

# Unikeyic Electronics

Global Electronic Components Distributor

Click to view pricing, inventory, delivery, and lifecycle information:

## Analog Devices:

MAX4186EEE MAX4503CUK-T MAX6008AEUR+T MAX6716UTVDD3+ AD8009AR MAX6720UTSYD3 MAX6338LUB MAX6428DHUR-T ADM2582EBRWZ-REEL7 ADV3221ARZ MAX693MLP LT3470ETS8#TRPBF MAX14819ATM+T MAX6743XKSDD3+ MAX6781LTB+T MAX805RCSA+ DS3153 LT1080IN#PBF LT8610ACEMSE#TRPBF LTM2892IY-I#PBF MAX3087EESA+T PD42-2-1240-TMCL AD7798BRUZ-REEL ADR430ARMZ LTM4643EV#PBF MAX296CPA+ LTC1799HS5#WTRMPBF MAX4514EUK+T MAX6715UTZGD3 DS275SN+