General Description

The RT8059GJ5 is high-efficiency,high frequency synchronous step-down DC-DC regulator ICs capable of delivering up to 1.2A output currents.The RT8059GJ5 can operate over a wide input voltage range from 2.3V to 6V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

It is ideal for powering portable equipment that runs from a single cell Lithium-Ion(Li+) battery.The output voltage can be regulated as low as 0.6V.The RT8059GJ5 can also run at 100% duty cycle for low dropout operation,extending battery life in portable system.This device offers two operation modes PWM mode and PFM mode switching control,which allows a high efficiency over the wide range of the load.

The RT8059GJ5 is offered in a low profile 5-pin SOT package,and is available in an adjustable version.

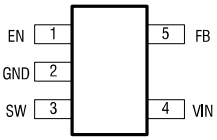
Features

- High Efficiency:Up to 96%
- 1.2MHz Constant Frequency Operation
- 1.2A Output Current
- No Schotky Diode Required
- 2.3Vto 6V Input Voltage Range
- Output Voltage as Low as 0.6V
- PFM Mode for High Efficiency in Light Load
- 100%Duty Cycle in Dropout Operation
- Low Quiescent Current:35μA
- Slope Compensated Current Mode Control for Excellent Line and Load Transient Response
- Short Circuit Protection
- Thermal Fault Protection
- Inrush Current Limit and Soft Start
- <1μA Shutdown Current
- SOT23-5 package

Applications

- Cellular and Smart Phones
- Wireless and DSL Modems
- PDAs
- Portable Instruments
- Digital Still and Video Cameras
- Set Top Box

Pinning and Marking

Pin Configuration	Marking
TOP VIEW  5-LEAD PLASTIC T_{JMAX} = 150°C, θ_{JA} = 250°C/ W, θ_{JC} = 130°C/W	 x :Inside Code,y : year, z : Week.

Pin Description

Pin Name	Pin Number	Description
EN	1	Chip Enable Pin.Drive EN above 1.5V to turn on the part.Drive EN below 0.3V to turn it off.Do not leave EN floating.
GND	2	Analog ground pin.
SW	3	Power Switch Output.It is the switch node connection to Inductor.This pin connects to the drains of the internal P-ch and N-ch MOSFET Switches.
VIN	4	Power Supply Input.Must be closely decoupled to GND with a 10μF or greater ceramic capacitor.
FB	5	Output Voltage Feedback Pin.An internal resistive divider divides the output voltage down for comparison to the internal reference voltage.

Order information

Orderable Device	Package	Packing Option
RT8059GJ5	SOT23-5	3000PCS

TYPICAL APPLICATION

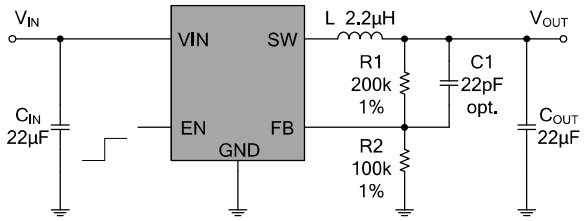
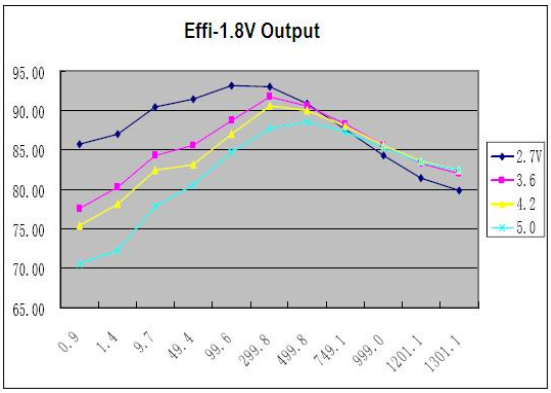


Figure 1. Basic Application Circuit



ABSOLUTE MAXIMUM RATINGS (Note 1)

Input SupplyVoltage.....-0.3V to 6.5V
EN,FB Voltages.....-0.3V to (V_{IN}+0.3V)
SW Voltage.....-0.3V to (V_{IN}+0.3V)
Power Dissipation.....0.4W
Thermal Resistance θ_{JC}.....130℃/W
Thermal Resistance θ_{JA}.....250℃/W
Junction Temperature(Note2).....150℃
Operating Temperature Range.....-40℃to85℃
Lead Temperature(Soldering,10s).....300℃
Storage Temperature Range.....-60℃ to 150℃
ESD HBM(Human Body Mode).....2kV
ESD MM(Machine Mode).....200V

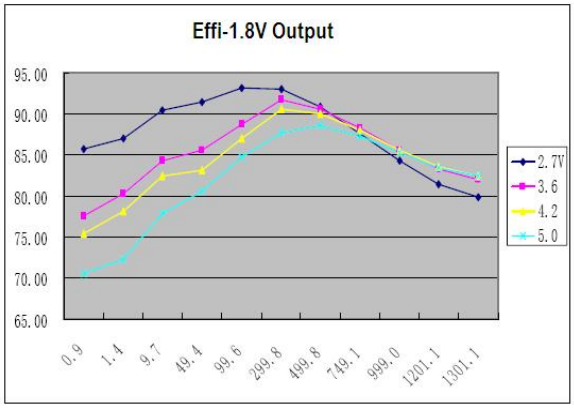
ELECTRICAL CHARACT ERISTICS (Note 3)

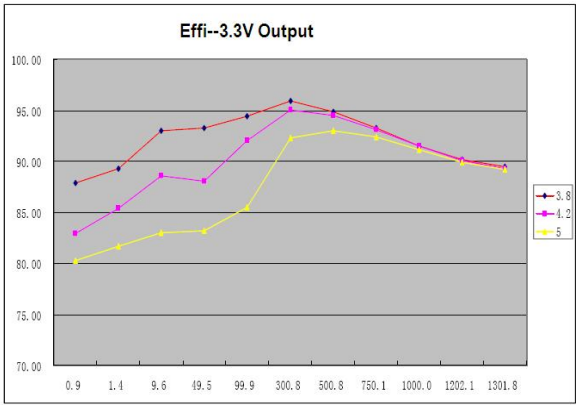
(V_{IN}=V_{EN}=3.6V,V_{OUT}=1.8V,T_A=25℃,unless otherwise noted.)

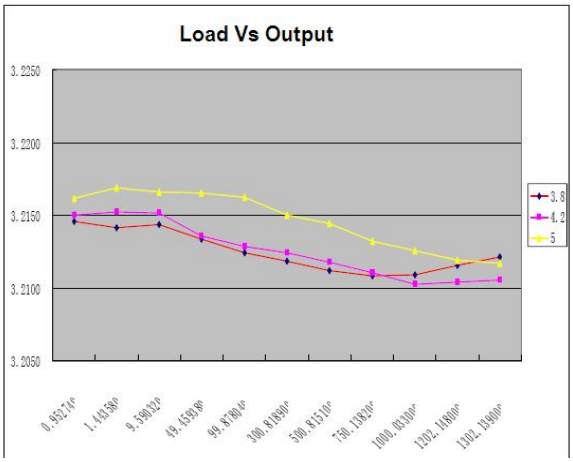
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		2.3		6	V
UVLO Threshold		1.7	1.9	2.1	V
Input DC Supply Current	(Note 4)				μA
PWM Mode	V_{OUT} = 90%, I_{LOAD}=0mA		140	300	μA
PFM Mode	V_{OUT} = 105%, I_{LOAD} =0mA		35	70	μA
Shutdown Mode	V_{EN} = 0V, V_{IN}=4.2V		0.1	1.0	μA
Regulated Feedback Voltage V_{FB}	T_A = 25°C	0.588	0.600	0.612	V
	T_A = 0°C ≤T_A ≤85°C	0.586	0.600	0.613	V
	T_A = -40°C ≤T_A ≤85°C	0.585	0.600	0.615	V
Reference Voltage Line Regulation	V_{IN} =2.5V to 5.5V		0.04	0.40	%/V
Output Voltage Line Regulation	V_{IN} =2.5V to 5.5V		0.04	0.40	%
Output Voltage Load Regulation			0.5		%
Oscillation Frequency	V_{OUT} =100%		1.2		MHz
	V_{OUT} =0V		300		kHz
On Resistance of PMOS	I_{SW}=100mA		300	450	mΩ
On Resistance of NMOS	I_{SW}=-100mA		300	450	mΩ
Peak Current Limit	V_{IN}= 3V, V_{OUT} =90%		2		A
Turn on delay time	RT8059		1		mS
OVP	RT8059		6.5		V
EN Threshold		0.30	1.0	1.50	V
EN Leakage Current			±0.01	±1.0	μA
SW Leakage Current	V_{EN}=0V,V_{IN}=V_{SW}=5V		±0.01	±1.0	μA

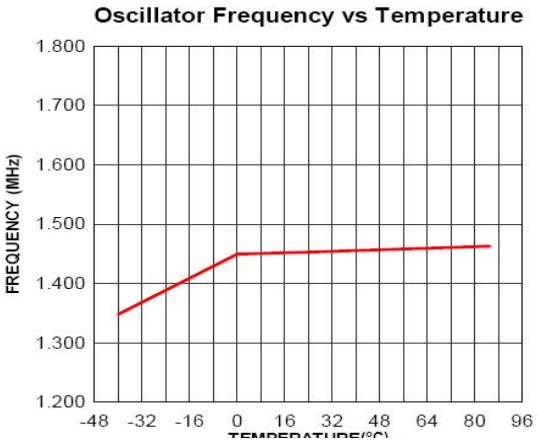
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.
Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D)$ x (250°C/W).
Note 3: 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.
Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

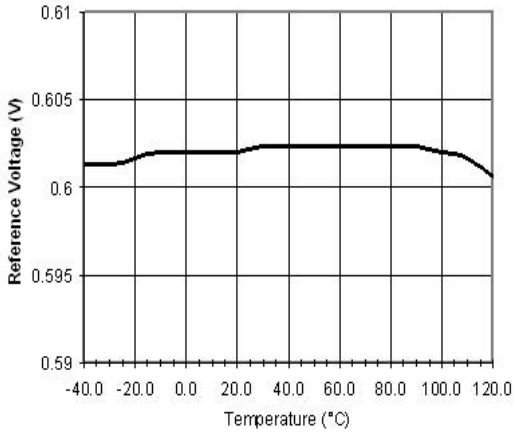
TYPICAL PERFORMANCE CHARACTERISTICS

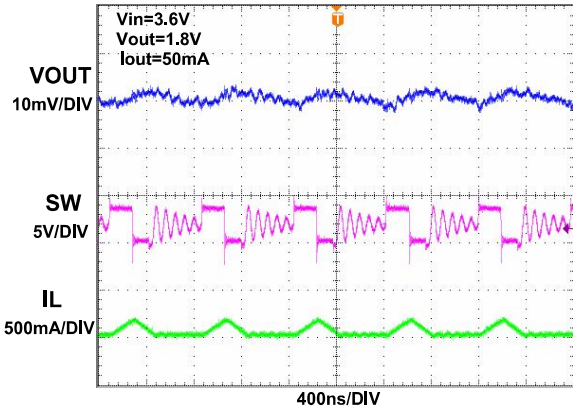












FUNCTIONAL BLOCK DIAGRAM

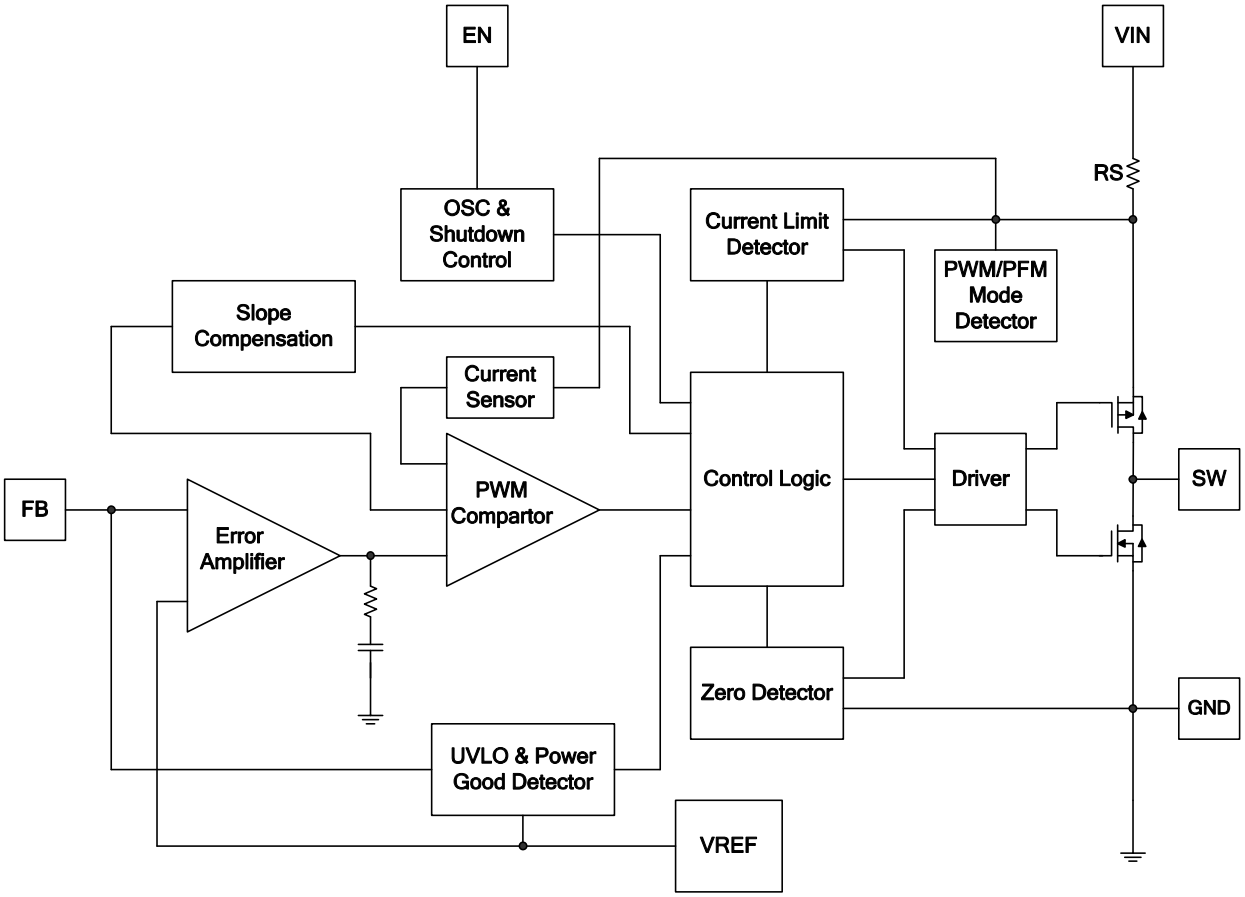


Figure 2. RT8059GJ5 Block Diagram

FUNCTIONAL DESCRIPTION

RT8059GJ5 is a synchronous buck regulator IC that integrates the PWM/PFM control , high-side and low-side MOSFETs on the same die to minimize the switching transition loss and conduction loss.With ultra low $R_{DS(ON)}$ power switches and proprietary PWM control,this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size,and thus achieving the minimum solution footprint.The RT8059GJ5 requires only three external power components (C_{IN},C_{OUT} and L) .The adjustable version can be programmed with external feedback to any voltage,ranging from 0.6V to the input voltage.At dropout operation,the converter duty cycle increases to 100% and the output voltage tracks the input voltage minus the $R_{DS(ON)}$ drop of the high-side MOSFET.The internal error amplifier and compensation provides excellent transient response, load and line regulation.Soft start function prevents input inrush current and output overshoot during start up.

APPUICATIONS INFORMATION

Setting the Output Voltage

The internal reference voltage V_{REF} is 0.6V (typical), the output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R1}{R2}\right)$$

The external resistive divider is connected to the output, allowing remote voltage sensing as shown in Figure 1.

Inductor Selection

For most designs, the RT8059GJ5 operates with inductors of 1μH to 4.7μH . Low inductance values are physically smaller but require faster switching, which results in some efficiency loss. The inductor value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is inductor Ripple Current. Large value inductors result in lower ripple current and small value inductors result in high ripple current. For optimum voltage-positioning load transients, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range.

Input Capacitor Selection

With the maximum load current at 1.2A,the maximum ripple current through input capacitor is about 0.6Arms.A typical X7R or better grade ceramic capacitor with 6V rating and greater than 10μF capacitance can handle this ripple current well. To minimize the potential noise problem,place this ceramic capacitor really close to VIN and GND pins.Care should be taken to minimize the loop aera formed by C_{IN},and VIN/GND pins.

Output Capacitor Selection

The output capacitor is required to keep the output voltage ripple small and to ensure regulation loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and high ripple current ratings. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \leq \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{OSC} \times L} \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}}\right)$$

A 10μF ceramic can satisfy most applications.

PCB Layout Recommendations

When laying out the printed circuit board, the following checking should be used to ensure proper operation of the RT8059GJ5 .
Check the following in your layout:

- The power traces, consisting of the GND trace, the SW trace and the VIN trace should be kept short, direct and wide
- Does the (+) plates of C_{IN} connect to VIN as closely as possible. This capacitor provides the AC current to the internal power MOSFETs.
- Keep the switching node, SW, away from the sensitive V_{OUT} node.
- Keep the (-) plates of C_{IN} and C_{OUT} as close as possible

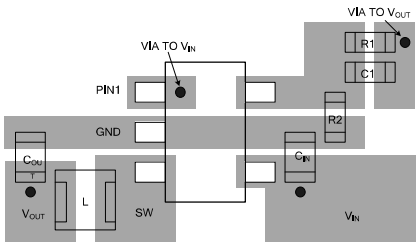
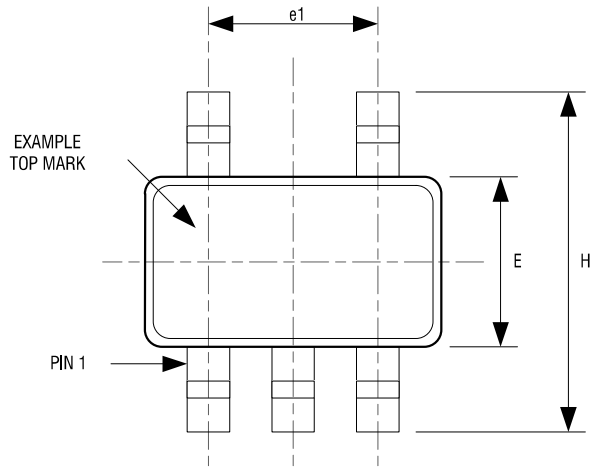


Figure 3. RT8059GJ5 Suggested Layout

PACKAGE DESCRIPTION

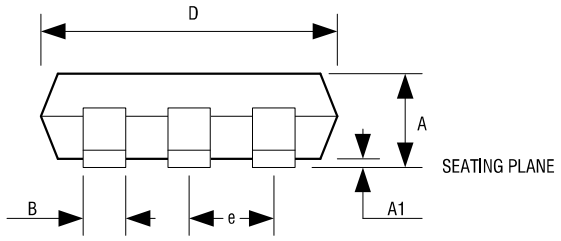
SOT23-5



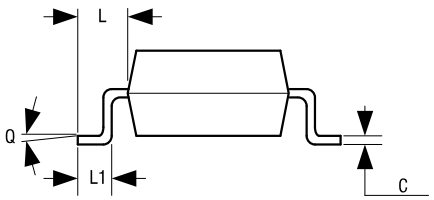
TOP VIEW

5LD SOT-23 PACKAGE OUTLINE DIMENSIONS

Dimension	Min.	Max.
A	1.05	1.35
A1	0.04	0.15
B	0.3	0.5
C	0.09	0.2
D	2.8	3.0
H	2.5	3.1
E	1.5	1.7
e	0.95 REF.	
e1	1.90 REF.	
L1	0.2	0.55
L	0.35	0.8
Q	0°	10°



FRONT VIEW



SIDE VIEW

NOTE:
1.DIMENSIONS ARE IN MILLIMETERS
2.DRAWING NOT TO SCALE
3.DIMENSIONS ARE INCLUSIVE OF PLATING
4.DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR