## OptiMOS™-5 Power-Transistor

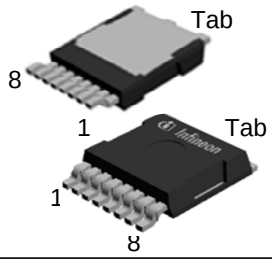
**Product Summary**

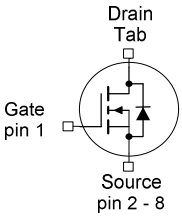
| | | |
|---|---|---|
| $V_{DS}$ | 80 | V |
| $R_{DS(on)}$ | 2.9 | mΩ |
| $I_D$ | 165 | A |

**Features**

- N-channel - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- Ultra low Rds(on)
- 100% Avalanche tested

PG-HSOG-8-1




| Type | Package | Marking |
|---|---|---|
| IAUS165N08S5N029 | PG-HSOG-8-1 | A08S5N29 |

**Maximum ratings,** at $T_j$=25 °C, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| Continuous drain current | $I_D$ | $T_C$=25°C, $V_{GS}$=10V[1] | 165 | A |
| | | $T_C$=100 °C, $V_{GS}$=10 V[2] | 120 | |
| Pulsed drain current[2] | $I_{D,pulse}$ | $T_C$=25 °C | 660 | |
| Avalanche energy, single pulse[2] | $E_{AS}$ | $I_D$=83 A | 225 | mJ |
| Avalanche current, single pulse | $I_{AS}$ | - | 165 | A |
| Gate source voltage | $V_{GS}$ | - | ±20 | V |
| Power dissipation | $P_{tot}$ | $T_C$=25 °C | 167 | W |
| Operating and storage temperature | $T_j$, $T_{stg}$ | - | -55 ... +175 | °C |
| IEC climatic category; DIN IEC 68-1 | - | - | 55/175/56 | |

| Parameter | Symbol | Conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| **Thermal characteristics**[2] | | | | | | |
| Thermal resistance, junction - case | $R_{thJC}$ | - | - | - | 0.9 | K/W |
| **Electrical characteristics,** at $T_j$=25 °C, unless otherwise specified | | | | | | |
| **Static characteristics** | | | | | | |
| Drain-source breakdown voltage[2] | $V_{(BR)DSS}$ | $V_{GS}$=0 V, $I_D$=1 mA | 80 | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$, $I_D$=108 µA | 2.2 | 3 | 3.8 | |
| Zero gate voltage drain current[2] | $I_{DSS}$ | $V_{DS}$=80 V, $V_{GS}$=0 V, $T_j$=25 °C | - | 0.1 | 1 | µA |
| | | $V_{DS}$=50 V, $V_{GS}$=0 V, $T_j$=85 °C[2] | - | 1 | 20 | |
| Gate-source leakage current | $I_{GSS}$ | $V_{GS}$=20 V, $V_{DS}$=0 V | - | - | 100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}$=6 V, $I_D$=40 A | - | 2.9 | 4.4 | mΩ |
| | | $V_{GS}$=10 V, $I_D$=80 A | - | 2.4 | 2.9 | |

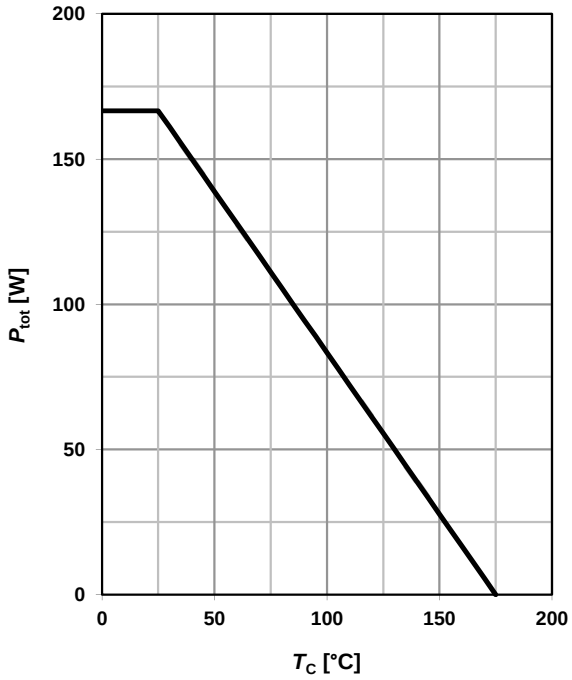
| Parameter | Symbol | Conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| **Dynamic characteristics**[2] | | | | | | |
| Input capacitance | $C_{iss}$ | $V_{GS}$=0 V, $V_{DS}$=40 V, $f$=1 MHz | - | 4900 | 6370 | pF |
| Output capacitance | $C_{oss}$ | | - | 790 | 1027 | |
| Reverse transfer capacitance | $C_{rss}$ | | - | 36 | 54 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$=40 V, $V_{GS}$=10 V, $I_D$=100 A, $R_G$=3.5 Ω | - | 13 | - | ns |
| Rise time | $t_r$ | | - | 9 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 23 | - | |
| Fall time | $t_f$ | | - | 29 | - | |
| **Gate Charge Characteristics**[2] | | | | | | |
| Gate to source charge | $Q_{gs}$ | $V_{DD}$=40 V, $I_D$=100 A, $V_{GS}$=0 to 10 V | - | 24 | 31 | nC |
| Gate to drain charge | $Q_{gd}$ | | - | 15 | 23 | |
| Gate charge total | $Q_g$ | | - | 70 | 90 | |
| Gate plateau voltage | $V_{plateau}$ | | - | 5.0 | - | V |
| **Reverse Diode** | | | | | | |
| Diode continous forward current[2] | $I_S$ | $T_C$=25 °C | - | - | 165 | A |
| Diode pulse current[2] | $I_{S,pulse}$ | | - | - | 660 | |
| Diode forward voltage | $V_{SD}$ | $V_{GS}$=0 V, $I_F$=100 A, $T_j$=25 °C | - | 0.9 | 1.2 | V |
| Reverse recovery time[2] | $t_{rr}$ | $V_R$=40 V, $I_F$=50A, d$i_F$/d$t$=100 A/µs | - | 60 | - | ns |
| Reverse recovery charge[2] | $Q_{rr}$ | | - | 96 | - | nC |

[1] Current is limited by bondwire; with an $R_{thJC}$ = 0.9 K/W the chip is able to carry 171A at 25°C.

[2] Defined by design. Not subject to production test.

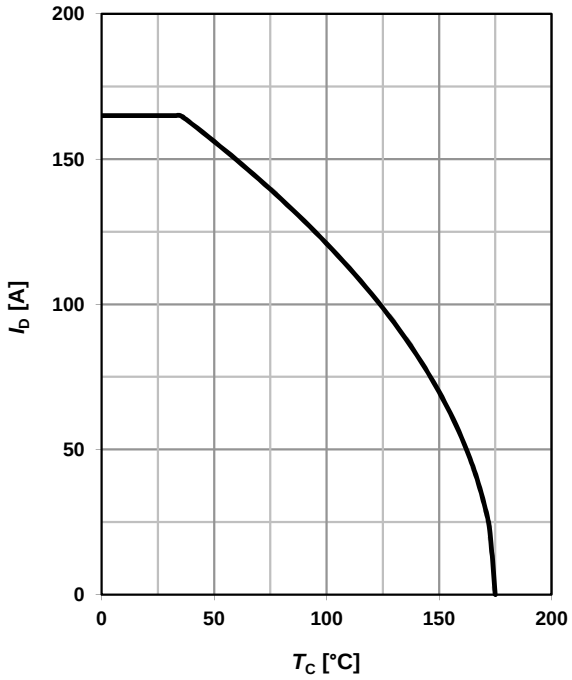
## 1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V




## 2 Drain current

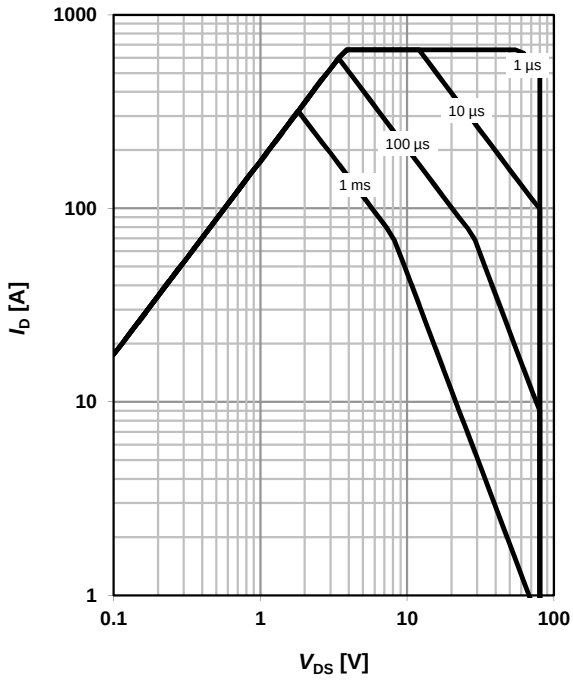
$I_D = f(T_C)$; $V_{GS} \geq 6$ V




## 3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$

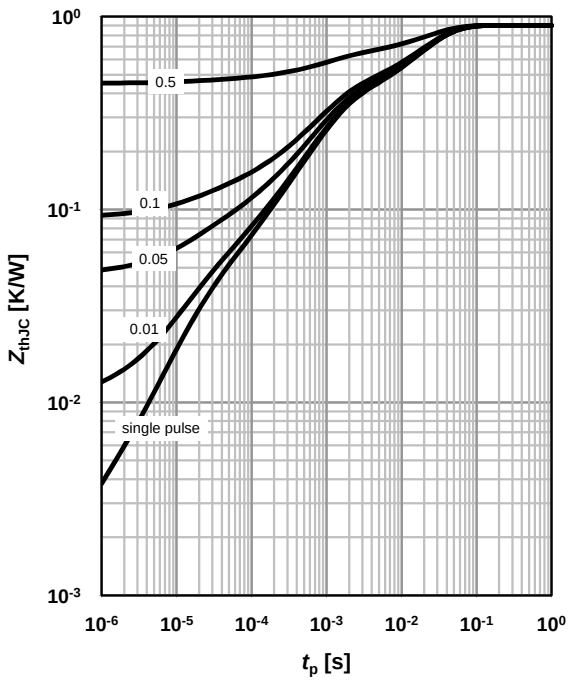
parameter: $t_p$




## 4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

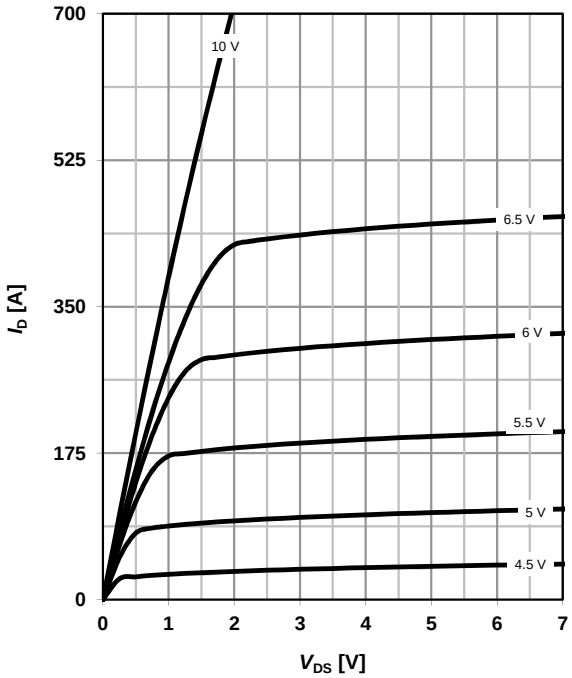
parameter: $D = t_p/T$



## 5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C

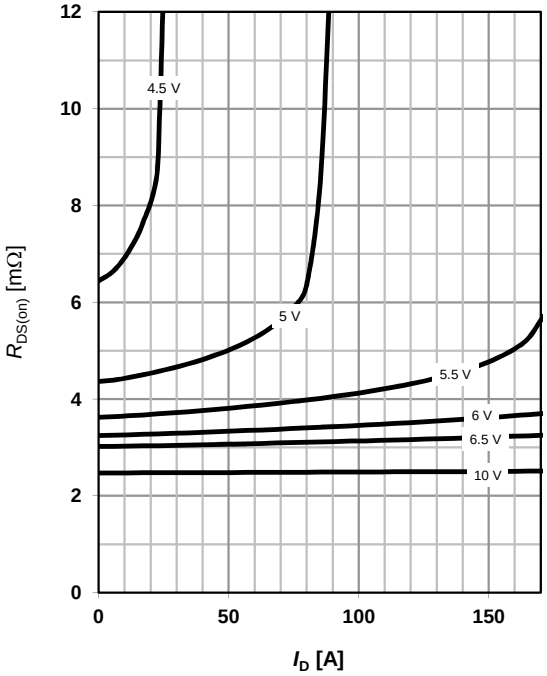
parameter: $V_{GS}$




## 6 Typ. drain-source on-state resistance

$R_{DS(on)} = (I_D)$; $T_j = 25$ °C

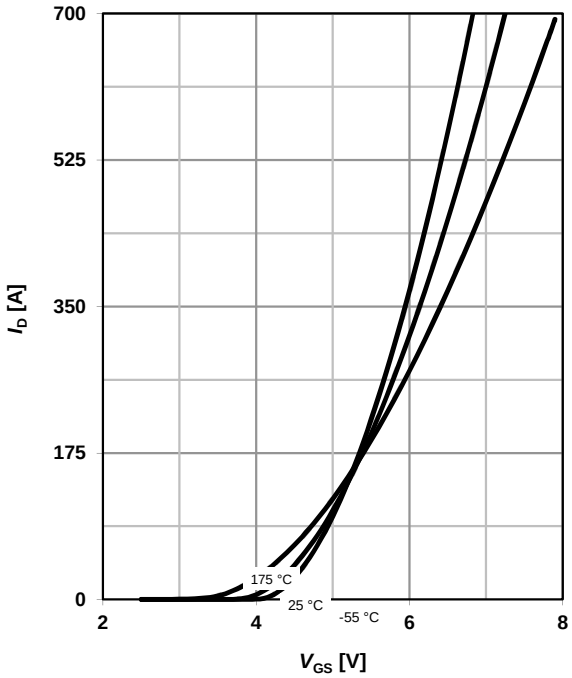
parameter: $V_{GS}$




## 7 Typ. transfer characteristics

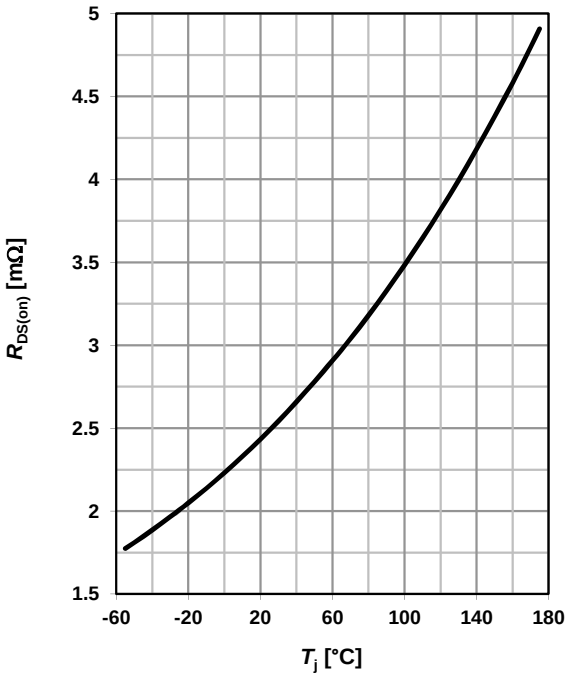
$I_D = f(V_{GS})$; $V_{DS} = 6$V

parameter: $T_j$




## 8 Typ. drain-source on-state resistance

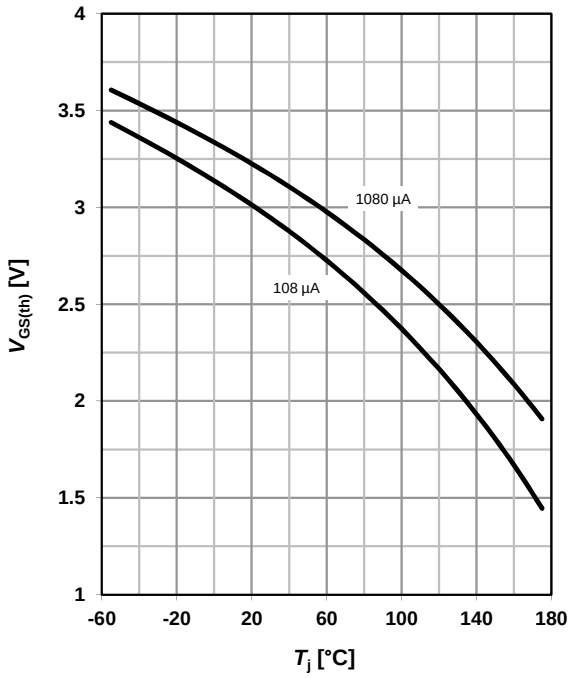
$R_{DS(on)} = f(T_j)$; $I_D = 80$ A; $V_{GS} = 10$ V



## 9 Typ. gate threshold voltage

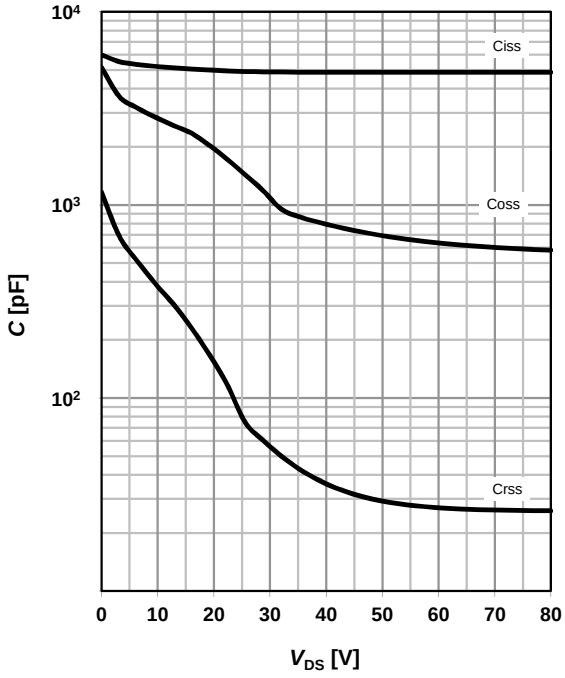
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: $I_D$




## 10 Typ. capacitances

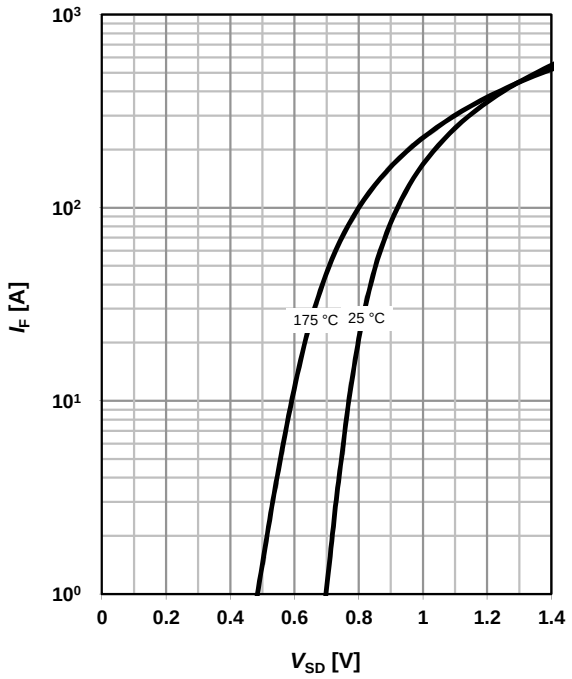
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz




## 11 Typical forward diode characteristicis

IF = f($V_{SD}$)

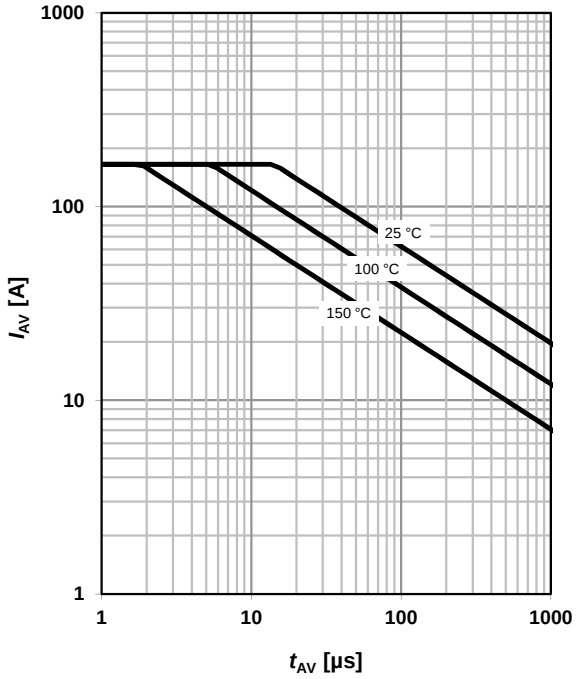
parameter: $T_j$




## 12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$

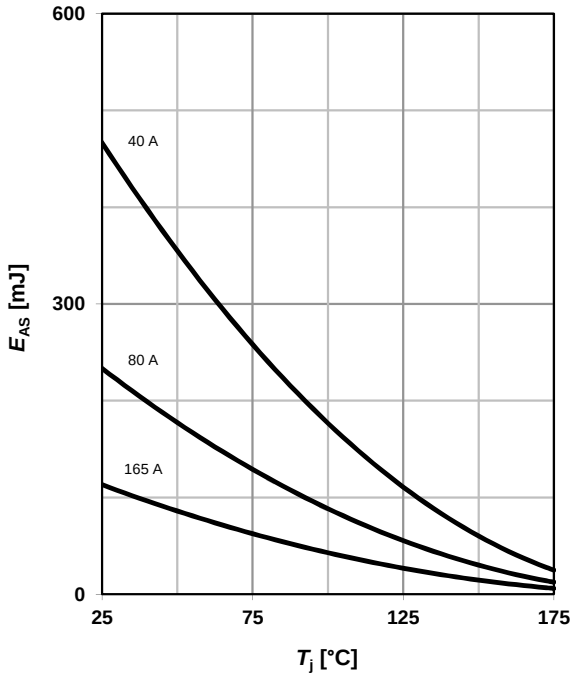
parameter: $T_{j(start)}$



## 13 Typical avalanche energy

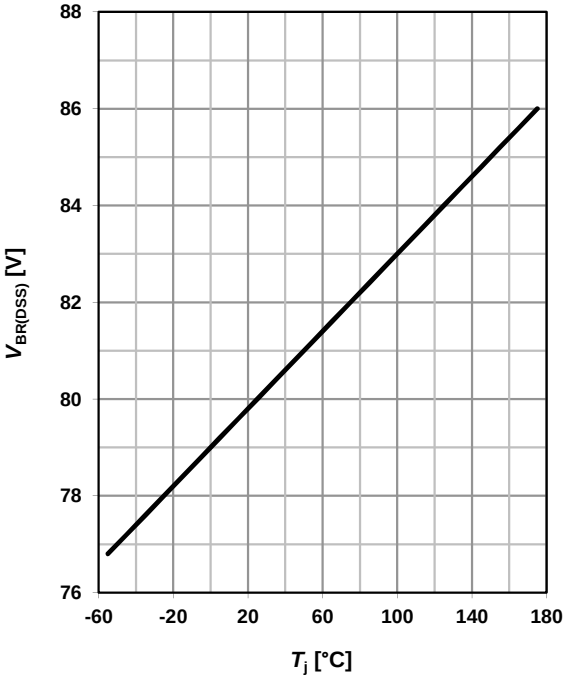
$E_{AS} = f(T_j)$

parameter: $I_D$




## 14 Drain-source breakdown voltage

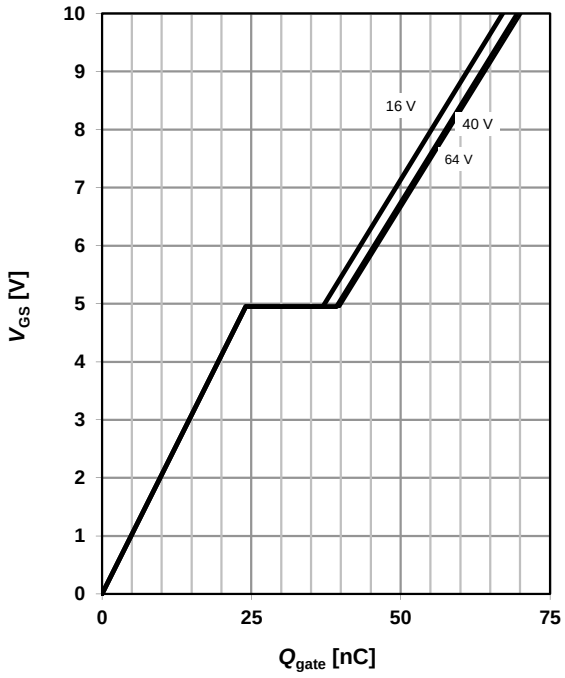
$V_{BR(DSS)} = f(T_j)$; $I_{D_typ}$ = 1 mA

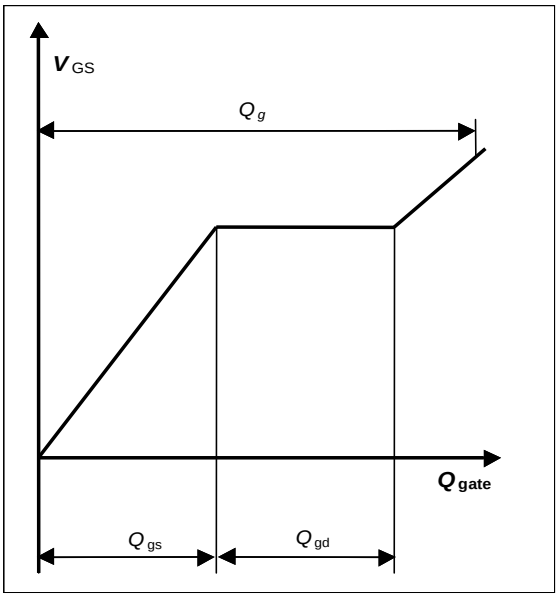



## 15 Typ. gate charge

$V_{GS} = f(Q_{gate})$; $I_D$ = 100 A pulsed

parameter: $V_{DD}$



**Published by**
**Infineon Technologies AG**
**81726 Munich, Germany**

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Revision History

| **Version** | Date | Changes |
|---|---|---|
| Version 1.0 | 4/10/2018 | Final Data Sheet |

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