74LVC1T45
Single-Bit Dual-Supply Bus Transceiver with Configurable Voltage Translation

GENERAL DESCRIPTION

The 74LVC1T45 is a single-bit, dual-supply bus transceiver with configurable voltage translation. The device has two separate configurable power-supply rails. The A and B ports track the V_{CCA} supply and V_{CCB} supply respectively. The supply voltage pins accept voltage range from 1.65V to 5.5V, which makes the device suitable for low voltage bidirectional translation voltage nodes of 1.8V, 2.5V, 3.3V, and 5V.

The 74LVC1T45 features that two data buses can communicate asynchronously. Either the A port outputs or the B port outputs can be activated by DIR logic levels. The DIR input circuit is supplied by V_{CCA}. When B port outputs are activated, the device allows the data to transmit from A bus to B bus. On the contrary, when A port outputs are activated, the device allows the data to transmit from B bus to A bus. The input circuit is always active on the two ports. A logic level of high or low must be set to avoid excessive supply current.

FEATURES

- **V_{CCA} Supply Voltage Range: 1.65V to 5.5V**
- **V_{CCB} Supply Voltage Range: 1.65V to 5.5V**
- **DIR Input Circuit Referenced to V_{CCA}**
- **+32mA/-32mA Output Current**
- **Data Rates**
  - **420Mbps (3.3V to 5V Translation)**
  - **210Mbps (Translate to 3.3V)**
  - **140Mbps (Translate to 2.5V)**
  - **75Mbps (Translate to 1.8V)**
- **Outputs in High-Impedance State when V_{CCA} or V_{CCB} = 0V**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SC70-6, SOT-23-6 Packages**

APPLICATIONS

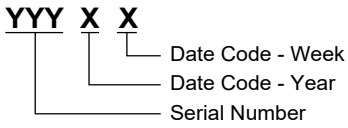
Personal Electronic Devices
Industrial and Enterprise Devices
Telecommunications

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74LVC1T45	SC70-6	-40℃ to +125℃	74LVC1T45XC6G/TR	MCTXX	Tape and Reel, 3000
	SOT-23-6	-40℃ to +125℃	74LVC1T45XN6G/TR	MCSXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XX = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage Range, V_{CCA} ..... -0.5V to 6.5V
Supply Voltage Range, V_{CCB} ..... -0.5V to 6.5V
Input Voltage Range, V_I (2) ..... -0.5V to 6.5V
Output Voltage Range, V_O (2)
High-Impedance State ..... -0.5V to 6.5V
High-State or Low-State
A Ports .....-0.5V to MIN (6.5V, V_{CCA} + 0.5V)
B Ports .....-0.5V to MIN (6.5V, V_{CCB} + 0.5V)
Input Clamp Current, I_{IK} (V_I < 0).....-50mA
Output Clamp Current, I_{OK} (V_O < 0).....-50mA
Output Current, I_O
High-State or Low-State.....±50mA
Supply Current, I_{CCA} or I_{CCB} 100mA
Ground Current, I_{GND}.....-100mA
Junction Temperature (3).....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....4000V
CDM.....1000V

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

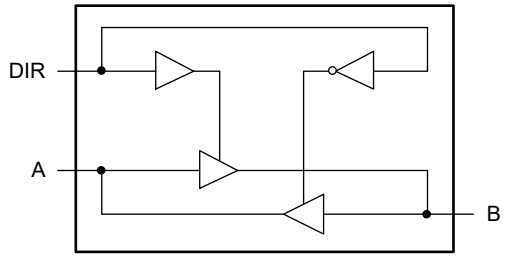
DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CCA} ..... 1.65V to 5.5V
Supply Voltage Range, V_{CCB} ..... 1.65V to 5.5V
Input Voltage Range, V_I ..... 0V to 5.5V
Output Voltage Range, V_O
High-Impedance State ..... 0V to 5.5V
High-State or Low-State
A Ports ..... 0V to V_{CCA}
B Ports ..... 0V to V_{CCB}
High-State or Low-State ..... ±32mA
Input Transition Rise or Fall Rate, Δt/ΔV
Data Inputs
V_{CCI} = 1.65V to 1.95V ..... 20ns/V (MAX)
V_{CCI} = 2.3V to 2.7V ..... 20ns/V (MAX)
V_{CCI} = 3V to 3.6V ..... 10ns/V (MAX)
V_{CCI} = 4.5V to 5.5V ..... 5ns/V (MAX)
Control Input
V_{CCI} = 1.65V to 5.5V ..... 5ns/V (MAX)
Operating Temperature Range ..... -40℃ to +125℃

LOGIC DIAGRAM



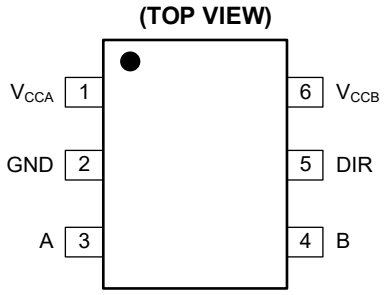
FUNCTION TABLE

SUPPLY VOLTAGE	CONTROL INPUT	INPUT/OUTPUT (1)	
V_{CCA}, V_{CCB}	DIR (2)	A	B
1.65V to 5.5V	L	A = B	Input
1.65V to 5.5V	H	Input	B = A
GND (3)	*X*	Z	Z

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High-Impedance State

NOTES:
1. The input circuit of the data I/O is always active.
2. The DIR input circuit is referenced to V_{CCA}.
3. If at least one of V_{CCA} or V_{CCB} is at GND level, the outputs in High-Impedance State.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
SOT-23-6/SC70-6		
1	V_{CCA}	Supply Voltage on A Port.
2	GND	Ground.
3	A	Input/Output. It tracks the V_{CCA} supply.
4	B	Input/Output. It tracks the V_{CCB} supply.
5	DIR	Direction Control Input. It tracks the V_{CCA} supply.
6	V_{CCB}	Supply Voltage on B Port.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, typical values are at T_A = +25℃. V_{CCI} is the supply voltage associated with the data input port. V_{CCO} is the supply voltage associated with the data output port, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CCA}			Full	1.65		5.5	V
	V_{CCB}			Full	1.65		5.5	
High-Level Input Voltage	V_{IH}	Data and DIR inputs	V_{CCI} = 1.65V to 1.95V	Full	0.65 × V_{CCI}			V
			V_{CCI} = 2.3V to 2.7V	Full	1.7			
			V_{CCI} = 3V to 3.6V	Full	2			
			V_{CCI} = 4.5V to 5.5V	Full	0.7 × V_{CCI}			
Low-Level Input Voltage	V_{IL}	Data and DIR inputs	V_{CCI} = 1.65V to 1.95V	Full			0.35 × V_{CCI}	V
			V_{CCI} = 2.3V to 2.7V	Full			0.7	
			V_{CCI} = 3V to 3.6V	Full			0.8	
			V_{CCI} = 4.5V to 5.5V	Full			0.3 × V_{CCI}	
High-Level Output Voltage	V_{OH}	V_I = V_{IH}	V_{CCO} = 1.65V to 4.5V, I_{OH} = -100μA	Full	V_{CCO} - 0.03	V_{CCO} - 0.01		V
			V_{CCO} = 1.65V, I_{OH} = -4mA	Full	1.37	1.53		
			V_{CCO} = 2.3V, I_{OH} = -8mA	Full	2.00	2.17		
			V_{CCO} = 3V, I_{OH} = -24mA	Full	2.44	2.69		
			V_{CCO} = 4.5V, I_{OH} = -32mA	Full	3.98	4.2		
			V_{CCO} = 5.5V, I_{OH} = -32mA	Full	5.04	5.23		
Low-Level Output Voltage	V_{OL}	V_I = V_{IL}	V_{CCO} = 1.65V to 4.5V, I_{OL} = 100μA	Full		0.01	0.03	V
			V_{CCO} = 1.65V, I_{OL} = 4mA	Full		0.07	0.24	
			V_{CCO} = 2.3V, I_{OL} = 8mA	Full		0.1	0.25	
			V_{CCO} = 3V, I_{OL} = 24mA	Full		0.25	0.45	
			V_{CCO} = 4.5V, I_{OL} = 32mA	Full		0.28	0.50	
			V_{CCO} = 5.5V, I_{OL} = 32mA	Full		0.27	0.47	
Input Leakage Current	I_I	V_I = V_{CCA} or GND, V_{CCA} = V_{CCB} = 1.65V to 5.5V		Full		±0.01	±1	μA
Power-Off Leakage Current	I_{OFF}	V_I or V_O = 0V to 5.5V	A port, V_{CCA} = 0V, V_{CCB} = 0V to 5.5V	Full		±0.01	±1	μA
			B port, V_{CCB} = 0V, V_{CCA} = 0V to 5.5V	Full		±0.01	±1	
Off-State Output Current (1)	I_{OZ}	V_{CCA} = V_{CCB} = 1.65V to 5.5V, V_O = V_{CCO} or GND		Full		±0.01	±1	μA
Supply Current	I_{CCA}	V_I = V_{CCI} or GND, I_O = 0A	V_{CCA} = V_{CCB} = 1.65V to 5.5V	Full		0.4	2	μA
			V_{CCA} = 5V, V_{CCB} = 0V	Full		0.01	2	
			V_{CCA} = 0V, V_{CCB} = 5V	Full	-2	-0.01		
	I_{CCB}		V_{CCA} = V_{CCB} = 1.65V to 5.5V	Full		0.4	2	
			V_{CCA} = 5V, V_{CCB} = 0V	Full	-2	-0.01		
			V_{CCA} = 0V, V_{CCB} = 5V	Full		0.01	2	
	I_{CCA} + I_{CCB}	V_I = V_{CCI} or GND, I_O = 0A	V_{CCA} = V_{CCB} = 1.65V to 5.5V	Full		0.4	4	
Additional Supply Current	ΔI_{CCA}	A port at V_{CCA} - 0.6V, DIR at V_{CCA}, B port = open, V_{CCA} = V_{CCB} = 3V to 5.5V		Full		0.2	10	μA
		DIR at V_{CCA} - 0.6V, A port at V_{CCA} or GND, B port = open, V_{CCA} = V_{CCB} = 3V to 5.5V		Full		0.2	10	
	ΔI_{CCB}	B port at V_{CCB} - 0.6V, DIR at GND, A port = open, V_{CCA} = V_{CCB} = 3V to 5.5V		Full		0.2	10	
Input Capacitance	C_I	V_{CCA} = V_{CCB} = 3.3V, DIR input, V_I = V_{CCA} or GND		+25℃		4		pF
Input/Output Capacitance	C_{IO}	V_{CCA} = V_{CCB} = 3.3V, A and B ports, V_O = $V_{CCA/B}$ or GND		+25℃		5		pF

NOTE:

1. For I/O ports, the parameter I_{OZ} includes the input leakage current.

DYNAMIC CHARACTERISTICS

(For test circuit see Figure 1. Minimum and maximum values are at T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	V_{CCB}												UNITS
			1.8V ± 0.15V			2.5V ± 0.2V			3.3V ± 0.3V			5V ± 0.5V			
			MIN (1)	TYP	MAX (1)	MIN (1)	TYP	MAX (1)	MIN (1)	TYP	MAX (1)	MIN (1)	TYP	MAX (1)	
V_{CCA} = 1.8V ± 0.15V															
Propagation Delay	t_{PLH}	A to B	1.5	6	13	1	4.5	9	1	4	7.5	1	4	7	ns
	t_{PHL}		1.5	6	13	1	4.5	8.5	1	4	7.5	1	4	7	
	t_{PLH}	B to A	1.5	6	13	1	5	12	1	5	11.5	1	5	11	
	t_{PHL}		1.5	6	13	1	5	12	1	5	11.5	1	5	11.5	
Disable Time	t_{PHZ}	DIR to A	3	10.5	16	3	10.5	16	3	10.5	16	3	10.5	16	ns
	t_{PLZ}		2.5	7	11.5	2.5	7.5	11.5	2.5	7	12	2.5	8.5	13	
	t_{PHZ}	DIR to B	3	14	22	2.5	9	14	2.5	6	11	2.5	5.5	9	
	t_{PLZ}		3	10	17	2	6	11	2.5	6.5	10	2	5	8	
Enable Time (2)	t_{PZH}	DIR to A		16	30		11	23		11.5	21.5		10	19	ns
	t_{PZL}			20	35		14	26		11	22.5		10.5	20.5	
	t_{PZH}	DIR to B		13	24.5		12	20.5		11	19.5		12.5	20	
	t_{PZL}			16.5	29		15	24.5		14.5	23.5		14.5	23	
V_{CCA} = 2.5V ± 0.2V															
Propagation Delay	t_{PLH}	A to B	1	5	12	1	3.5	7.5	1	3	6	0.7	3	5.5	ns
	t_{PHL}		1	5	12	1	3.5	7.5	1	3	6	0.7	3	5.5	
	t_{PLH}	B to A	1	4.5	9	1	3.5	7.5	1	3.5	7	1	3.5	7	
	t_{PHL}		1	4.5	8.5	1	3.5	7.5	1	3.5	7	0.9	3.5	7	
Disable Time	t_{PHZ}	DIR to A	2	7	10	2	7	10	2	7	10	2	7.5	11	ns
	t_{PLZ}		1.5	3.5	8	1.5	3.5	8	1.5	3.5	8	1.5	4	8	
	t_{PHZ}	DIR to B	3.5	12.5	20.5	2.5	7.5	12	2.5	5	10	2	4	7.5	
	t_{PLZ}		3	9	16	2	5	10	2.5	5.5	9	2	4	7	
Enable Time (2)	t_{PZH}	DIR to A		13.5	25		8.5	17.5		9	16		7.5	14	ns
	t_{PZL}			17	29		11	19.5		8.5	17		7.5	14.5	
	t_{PZH}	DIR to B		8.5	20		7	15.5		6.5	14		7	13.5	
	t_{PZL}			12	22		10.5	17.5		10	16		10.5	16.5	

DYNAMIC CHARACTERISTICS (continued)

(For test circuit see Figure 1. Minimum and maximum values are at T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	V_{CCB}												UNITS
			1.8V ± 0.15V			2.5V ± 0.2V			3.3V ± 0.3V			5V ± 0.5V			
			MIN (1)	TYP	MAX (1)	MIN (1)	TYP	MAX (1)	MIN (1)	TYP	MAX (1)	MIN (1)	TYP	MAX (1)	
V_{CCA} = 3.3V ± 0.3V															
Propagation Delay	t_{PLH}	A to B	1	5	11.5	1	3.5	7	0.7	3	5.5	0.7	2.5	5	ns
	t_{PHL}		1	5	11.5	1	3.5	7	0.8	3	5.5	0.7	2.5	5	
	t_{PLH}	B to A	1	4	7.5	1	3	6	0.7	3	5.5	0.6	3	5.5	
	t_{PHL}		1	4	7.5	1	3	6	0.8	3	5.5	0.7	3	5.5	
Disable Time	t_{PHZ}	DIR to A	2	4	8.5	2	4	8.5	2	4	8.5	2	4	8.5	ns
	t_{PLZ}		1.5	3.5	8	1.5	3.5	8	1.5	4	8	1.5	4	8	
	t_{PHZ}	DIR to B	3.5	12.5	20	2.5	8	12	2.5	5	10	2	4	7.5	
	t_{PLZ}		3	8	15.5	2	4.5	10	2	5.5	8.5	1.5	3.5	7.5	
Enable Time (2)	t_{PZH}	DIR to A		12	23		7.5	16		8.5	14		6.5	13	ns
	t_{PZL}			16.5	27.5		11	18		8	15.5		7	13	
	t_{PZH}	DIR to B		8.5	19.5		7	15		7	13.5		6.5	13	
	t_{PZL}			9	20		7.5	15.5		7	14		6.5	13.5	
V_{CCA} = 5V ± 0.5V															
Propagation Delay	t_{PLH}	A to B	1	5	11	1	3.5	7	0.6	3	5.5	0.5	2.5	5	ns
	t_{PHL}		1	5	11.5	0.9	3.5	7	0.7	3	5.5	0.5	2.5	4.5	
	t_{PLH}	B to A	1	4	7	0.7	3	5.5	0.7	2.5	5	0.5	2.5	5	
	t_{PHL}		1	4	7	0.7	3	5.5	0.7	2.5	5	0.5	2.5	4.5	
Disable Time	t_{PHZ}	DIR to A	1.5	4	6.5	1.5	4	6.5	1.5	4	6.5	1.5	4	7	ns
	t_{PLZ}		1	3	5.5	1	3	5.5	1	3	5.5	1	3	5.5	
	t_{PHZ}	DIR to B	3.5	12	19.5	2.5	8	12.5	2.5	5	10	2	4	7.5	
	t_{PLZ}		3	9.5	16	2	5.5	9	2	5.5	8.5	1.5	3.5	6	
Enable Time (2)	t_{PZH}	DIR to A		13.5	23		8.5	14.5		8	13.5		6	11	ns
	t_{PZL}			16	26.5		11	18		7.5	15		6.5	12	
	t_{PZH}	DIR to B		8	16.5		6.5	12.5		6	11		5.5	10.5	
	t_{PZL}			9	18		7.5	13.5		7	12		6.5	11.5	

NOTES:

1. Specified by design and characterization, not production tested.

2. The enable time value is calculated. Calculate the enable times for the 74LVC1T45 using the following formulas:

- t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
- t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
- t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
- t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

DYNAMIC CHARACTERISTICS (continued)

(For test circuit see Figure 1. All typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		V_{CCA} = V_{CCB} = 1.8V	V_{CCA} = V_{CCB} = 2.5V	V_{CCA} = V_{CCB} = 3.3V	V_{CCA} = V_{CCB} = 5V	UNITS
				TYP	TYP	TYP	TYP	
Power Dissipation Capacitance (1)	C_{PDA}	C_L = 0pF, f = 10MHz, t_R = t_F = 1ns	A Port Input, B Port Output	3	3	4	5	pF
			B Port Input, A Port Output	19	20	21	22	
	C_{PDB}	C_L = 0pF, f = 10MHz, t_R = t_F = 1ns	A Port Input, B Port Output	19	20	21	22	pF
			B Port Input, A Port Output	3	3	4	5	

NOTE:

1. Power dissipation capacitance per transceiver. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}{}^2 \times f_o)$

   where:

   f_i = input frequency in MHz.

   f_o = output frequency in MHz.

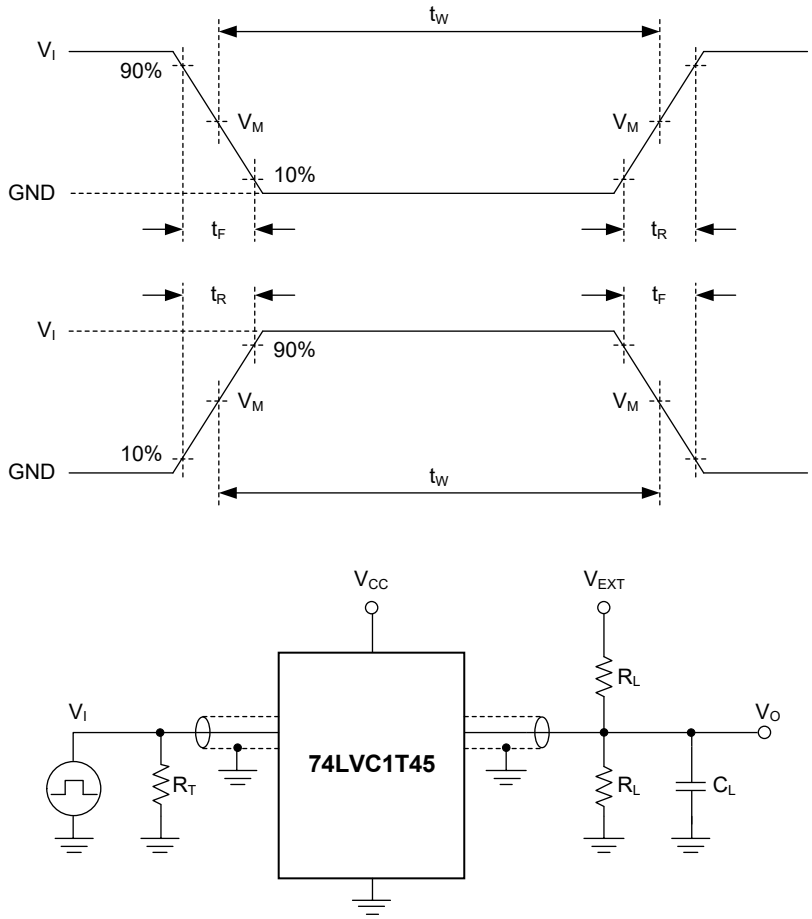
   C_L = output load capacitance in pF.

   V_{CC} = supply voltage in Volts.

   N = number of inputs switching.

   $\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of the outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

V_{EXT}: External voltage used to measure switching time.

Figure 1. Test Circuit for Measuring Switching Times

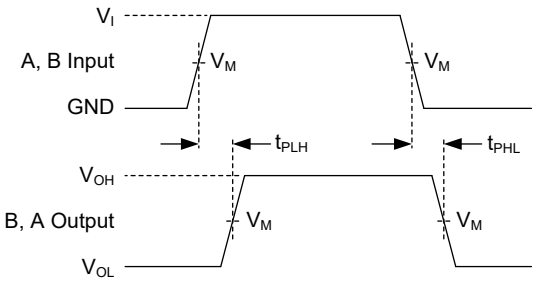
Table 1. Test Conditions

SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}		
V_{CCA}, V_{CCB}	V_I (1)	t_R, t_F	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL} (2)	t_{PLH}, t_{PHL}
1.65V to 5.5V	V_{CCI}	≤ 2.5ns	15pF	2kΩ	GND	2 × V_{CCO}	Open

NOTES:

1. V_{CCI} is the supply voltage related to the data input port.
2. V_{CCO} is the supply voltage related to the data output port.

WAVEFORMS

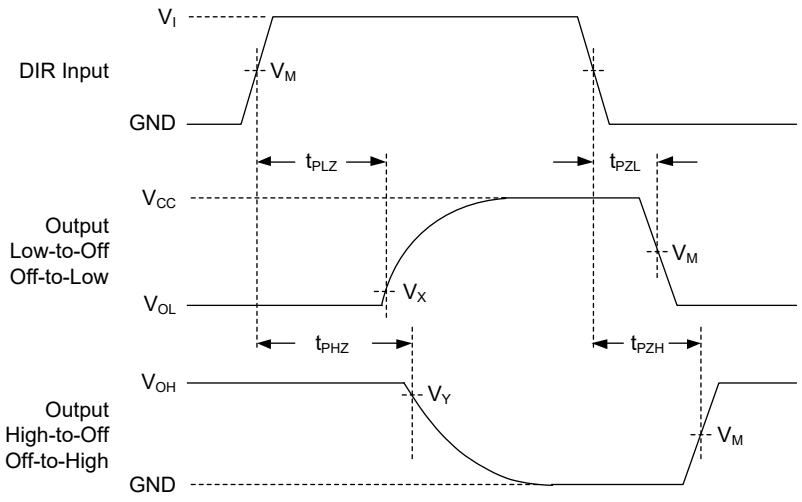


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Input (A, B) to Output (B, A) Propagation Delay Times



Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Enable and Disable Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT (1)		OUTPUT		
V_{CCA}, V_{CCB}	V_I	V_M (2)	V_M (3)	V_X	V_Y
1.65V to 2.7V	V_{CCI}	0.5 × V_{CCI}	0.5 × V_{CCO}	V_{OL} + 0.15V	V_{OH} - 0.15V
3V to 5.5V	V_{CCI}	0.5 × V_{CCI}	0.5 × V_{CCO}	V_{OL} + 0.3V	V_{OH} - 0.3V

NOTES:

1. V_{CCI} is the supply voltage related to the data input port.
2. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 2.5ns.
3. V_{CCO} is the supply voltage related to the data output port.

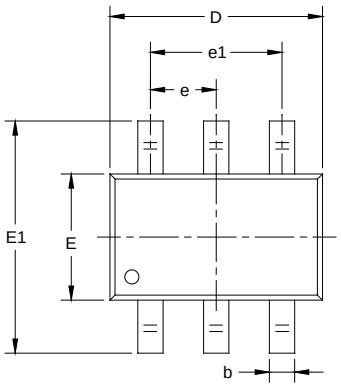
REVISION HISTORY

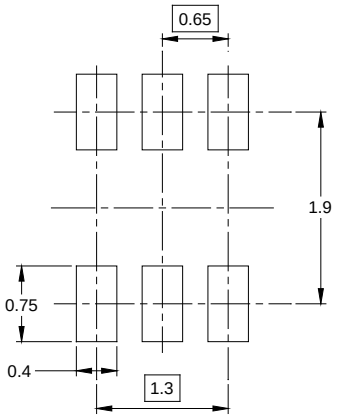
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (DECEMBER 2022) to REV.A	Page
Changed from product preview to production data	All

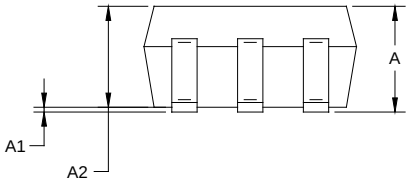
PACKAGE OUTLINE DIMENSIONS

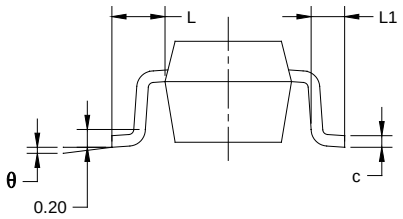
SC70-6





RECOMMENDED LAND PATTERN (Unit: mm)



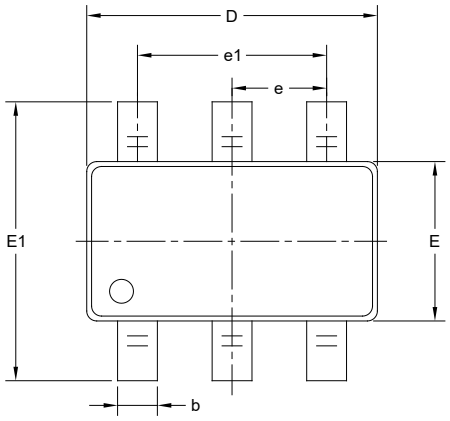


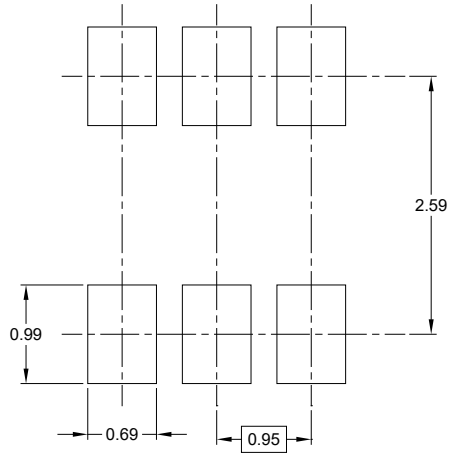
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	1.000	0.031	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.220	0.003	0.009
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.65 TYP		0.026 TYP	
e1	1.300 BSC		0.051 BSC	
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

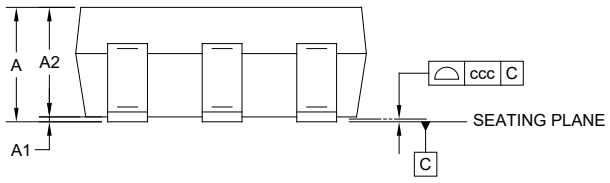
PACKAGE OUTLINE DIMENSIONS

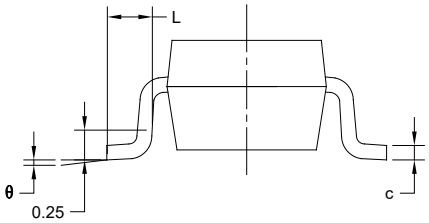
SOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



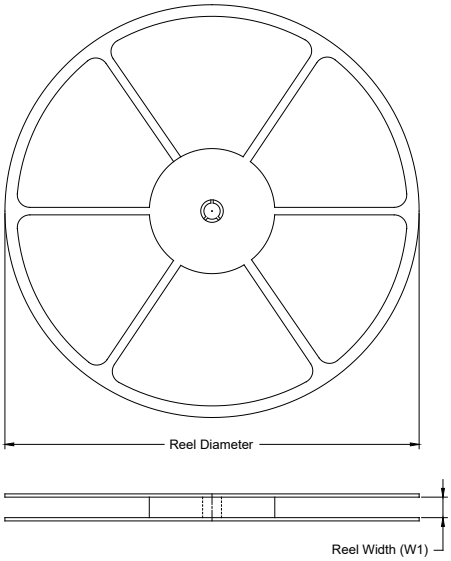


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

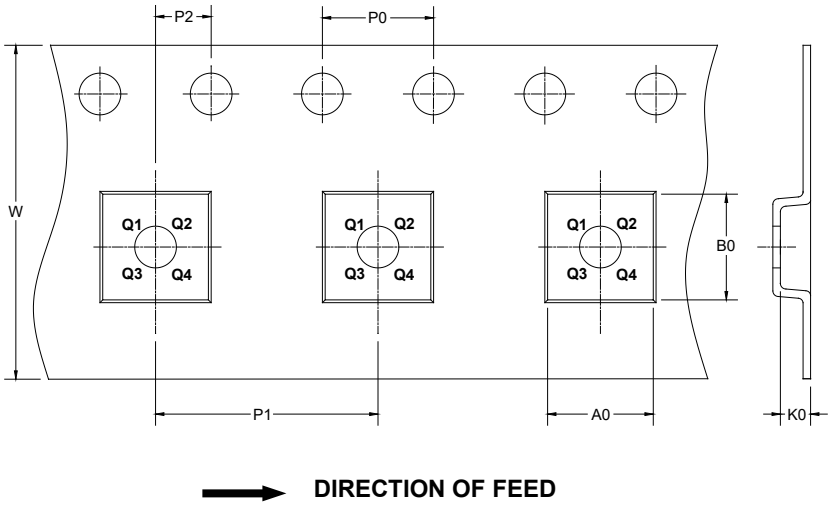
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



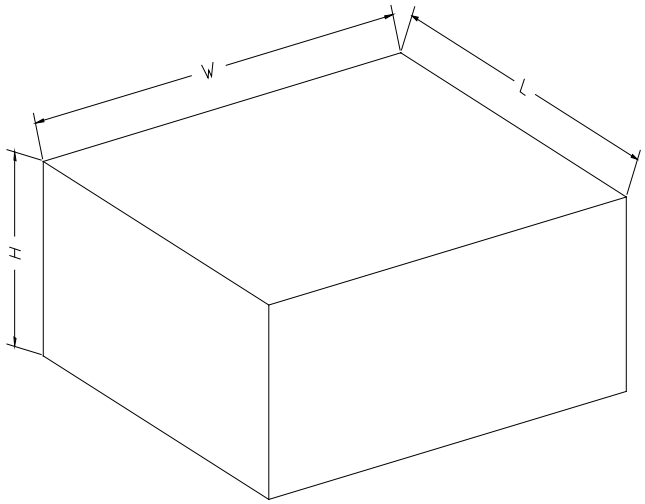
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SC70-6	7″	9.5	2.40	2.50	1.20	4.0	4.0	2.0	8.0	Q3
SOT-23-6	7″	9.5	3.23	3.17	1.37	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002

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SGM8255A-2XMS8G/TR SGM891B-2.5XN5G/TR SGM892B-2.5XUDH4G/TR SGM2036-2.3YUDH4G/TR
SGM2200H-2.8YN3LG/TR SGM2588FYN5G/TR SGM2588KYN5G/TR SGM2205-3.3XS8G/TR
SGM2200H-2.5YC5G/TR SGM890B-2.9XN5G/TR SGM2022-HYN6/TR SGM2205-12XKC3G/TR
SGM706B-RXMS8G/TR SGM2036-2.6YN5G/TR SGM2212-2.8XOA3G/TR SGM2540YUDV8G/TR
SGM41002-4.50YUDS8G/TR SGM892B-2.7LXN3G/TR SGM2020-1.8YN5G/TR SGM836-3.0XN6G/TR
SGM836-3.0XTDI6G/TR SGM897PXTN6G/TR