AUIRF5210STRL-VB Datasheet

P-Channel 100 V (D-S) MOSFET

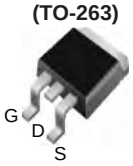
PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 100	0.040 at V_{GS} = - 10 V	- 37	54 nC
	0.050 at V_{GS} = - 4.5 V	- 32	

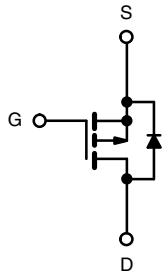
FEATURES

- Trench Power MOSFET

RoHS COMPLIANT
HALOGEN FREE

D²PAK (TO-263)





P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)[b]	T_C = 25 °C	I_D	- 37	A
	T_C = 70 °C		- 29.5	
	T_A = 25 °C		- 10[b, c]	
	T_A = 70 °C		- 8.2[b, c]	
Pulsed Drain Current		I_{DM}	- 150	
Continuous Source Current (Diode Conduction)	T_C = 25 °C	I_S	- 50[a]	
	T_A = 25 °C		- 6.75[b, c]	
Avalanche Current	L = 0.1 mH	I_{AS}	- 35	
Single Pulse Avalanche Energy		E_{AS}	61	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	113.6	W
	T_C = 70 °C		72.7	
	T_A = 25 °C		6.9[b, c]	
	T_A = 70 °C		4.4[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter		**Symbol**	**Limit**	**Unit**
Junction-to-Ambient	PCB Mount (TO-263)[c]	R_{thJA}	40	°C/W
Junction-to-Case (Drain)		R_{thJC}	2.1	

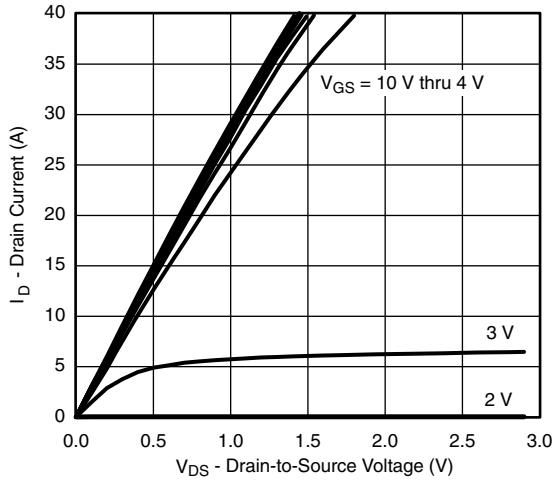
Notes:
a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 100			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 109		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			5.9		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 1		- 3	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 100 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 100 V, V_{GS} = 0 V, T_J = 55 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = - 10 V	- 40			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 9.2 A		0.040		Ω
		V_{GS} = - 4.5 V, I_D = - 7.7 A		0.050		
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 9.2 A		38		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 50 V, V_{GS} = 0 V, f = 1 MHz		3800		pF
Output Capacitance	C_{oss}			185		
Reverse Transfer Capacitance	C_{rss}			135		
Total Gate Charge	Q_g	V_{DS} = - 50 V, V_{GS} = - 10 V, I_D = - 9.2 A		106	160	nC
		V_{DS} = - 50 V, V_{GS} = - 4.5 V, I_D = - 9.2 A		54	81	
Gate-Source Charge	Q_{gs}			14		
Gate-Drain Charge	Q_{gd}			26		
Gate Resistance	R_g	f = 1 MHz		4		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 50 V, R_L = 6.5 Ω $I_D \cong$ - 7.7 A, V_{GEN} = - 10 V, R_g = 1 Ω		15	25	ns
Rise Time	t_r			20	30	
Turn-Off Delay Time	$t_{d(off)}$			110	165	
Fall Time	t_f			100	150	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 50 V, R_L = 6.5 Ω $I_D \cong$ - 7.7 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		42	65	ns
Rise Time	t_r			160	240	
Turn-Off Delay Time	$t_{d(off)}$			100	150	
Fall Time	t_f			100	150	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 50	A
Pulse Diode Forward Current[a]	I_{SM}				- 40	
Body Diode Voltage	V_{SD}	I_S = - 7.7 A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 7.7 A, dI/dt = 100 A/µs, T_J = 25 °C		60	90	ns
Body Diode Reverse Recovery Charge	Q_{rr}			150	225	nC
Reverse Recovery Fall Time	t_a			46		ns
Reverse Recovery Rise Time	t_b			14		

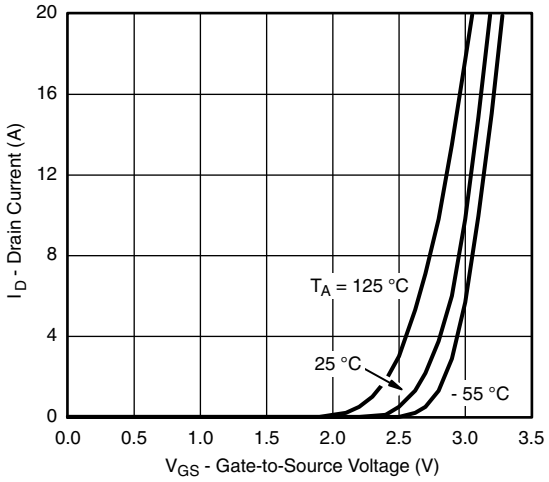
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

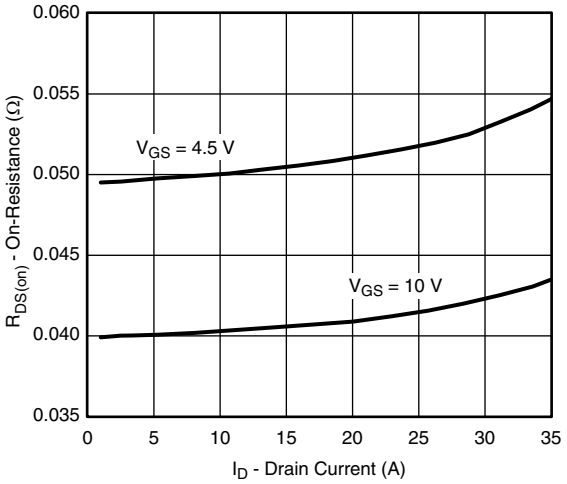
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



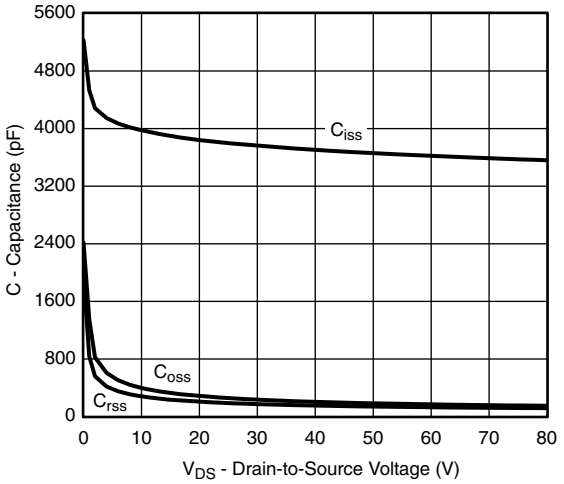
Output Characteristics



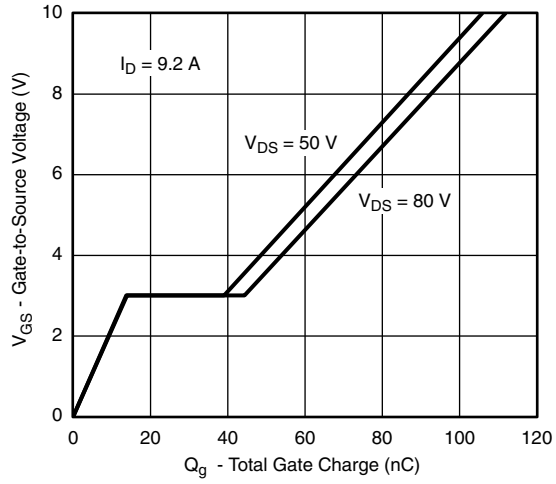
Transfer Characteristics



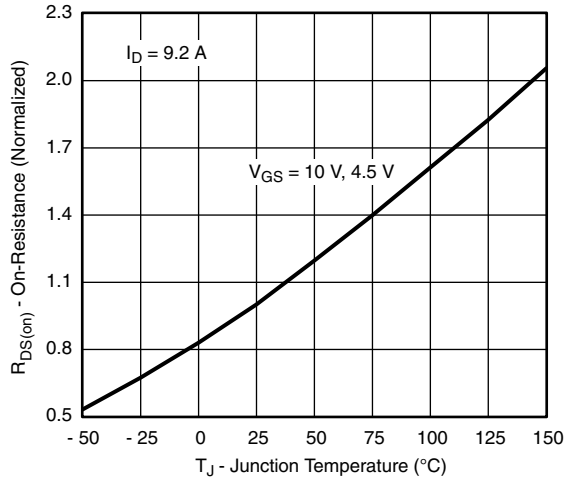
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

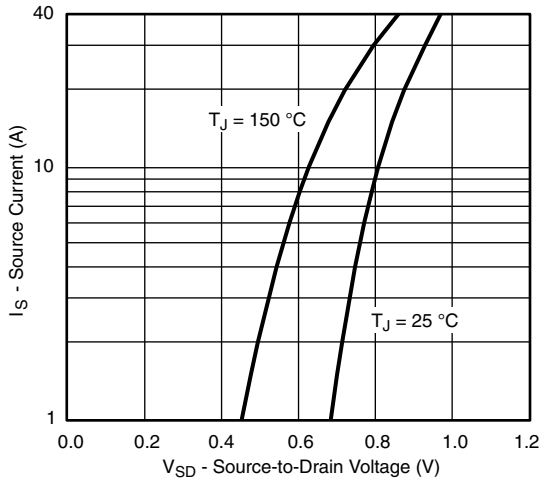


Gate Charge

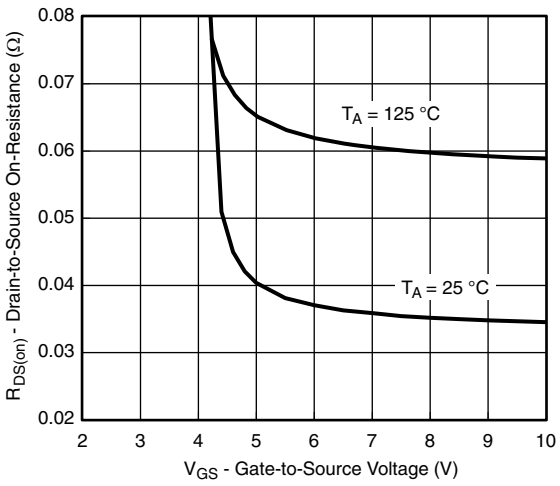


On-Resistance vs. Junction Temperature

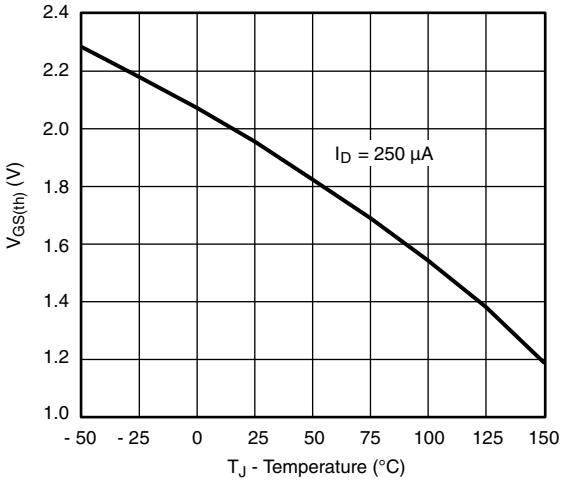
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



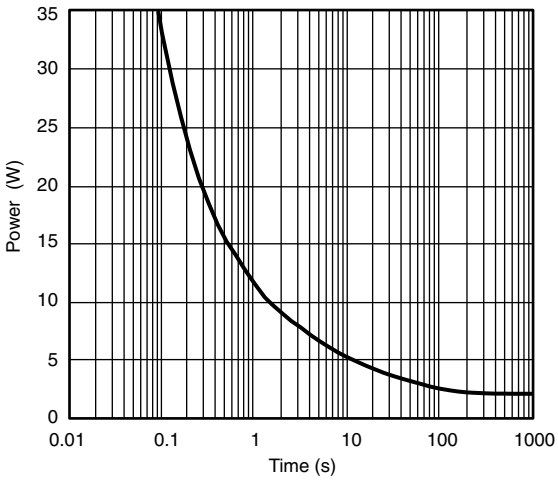
Source-Drain Diode Forward Voltage



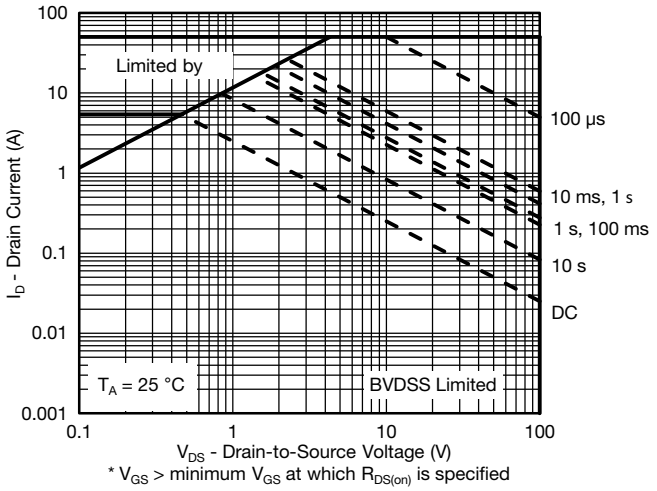
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

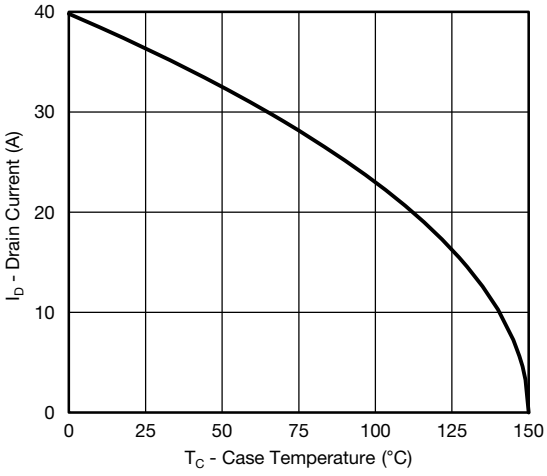


Single Pulse Power, Junction-to-Ambient

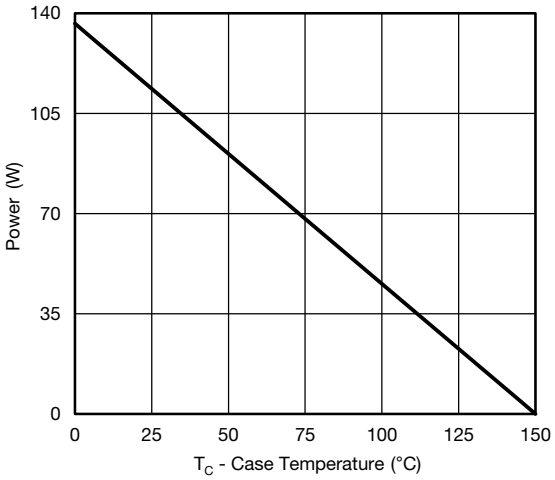


Safe Operating Area, Junction-to-Ambient

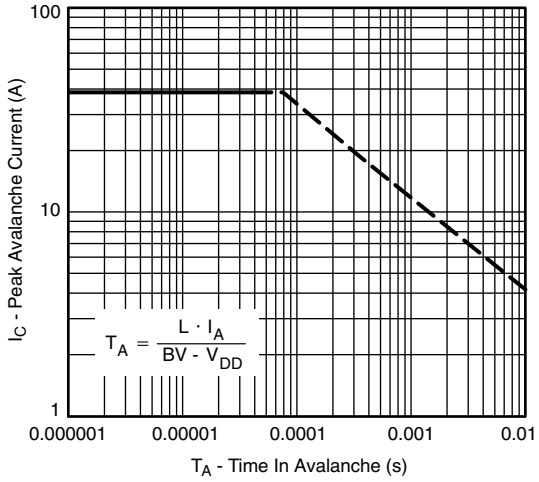
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



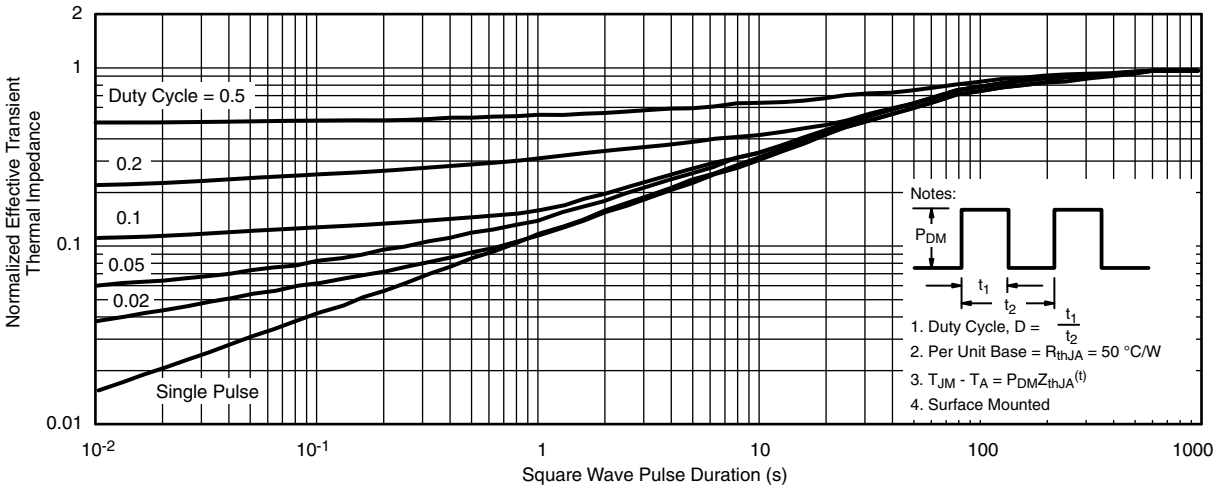
Single Pulse Power, Junction-to-Ambient



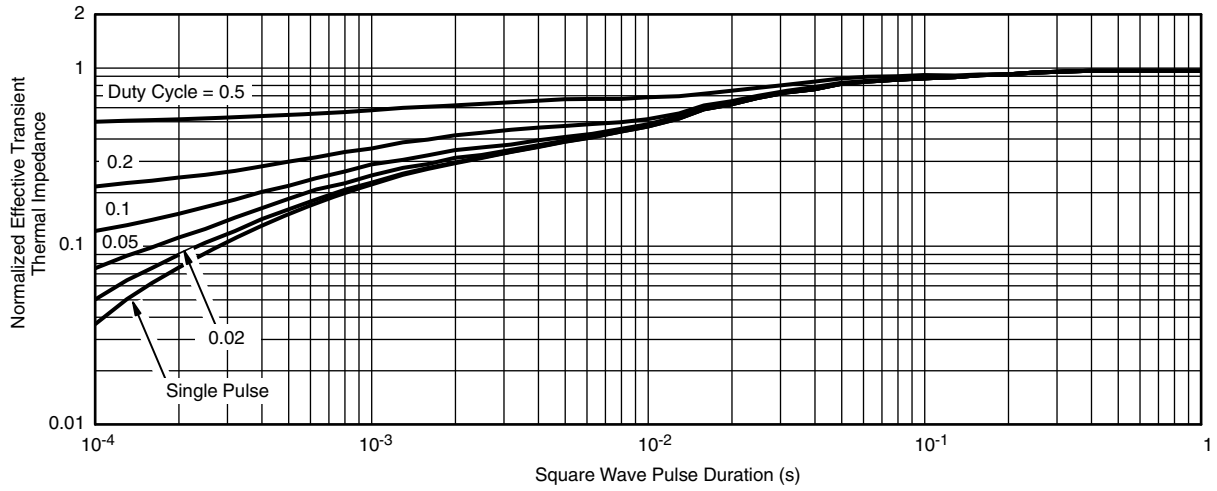
Single Pulse Avalance Capability

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

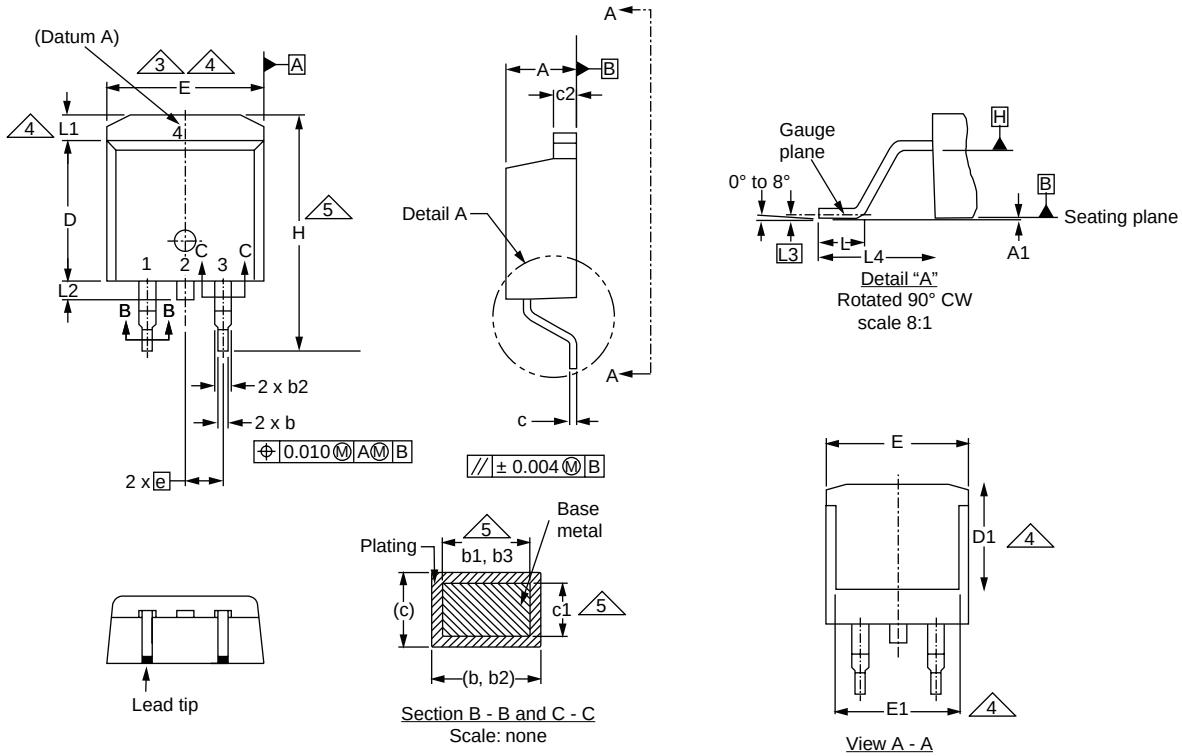


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

TO-263AB (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

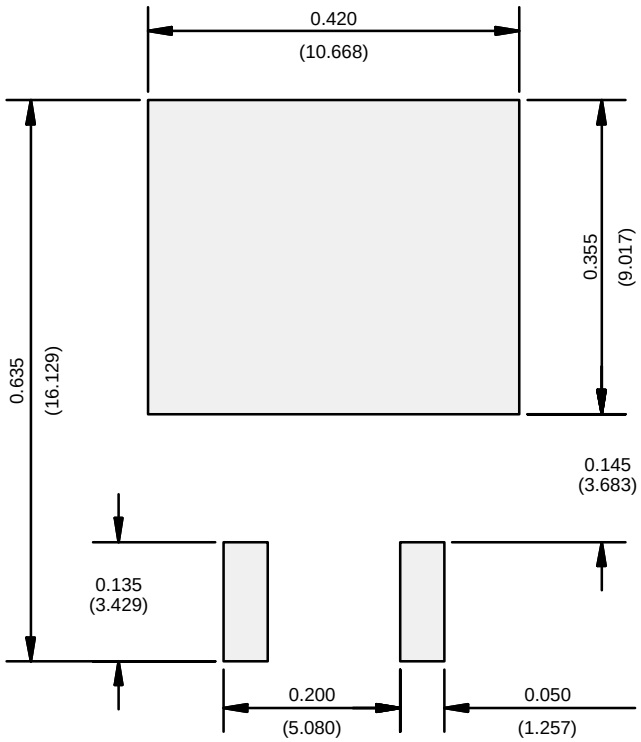
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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