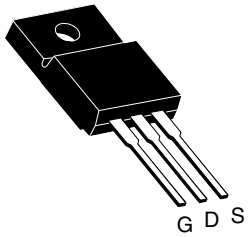
JCS12N60FT-O-F-N-B TK12A-VB Datasheet
N-Channel 650V (D-S) Power MOSFET

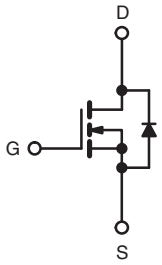
PRODUCT SUMMARY		
V_{DS} (V)	650	
$R_{DS(on)}$ at 25 °C (Ω)	V_{GS} = 10 V	0.17
Q_g max. (nC)	109	
Q_{gs} (nC)	15	
Q_{gd} (nC)	31	
Configuration	Single	

FEATURES
- Low figure-of-merit (FOM) R_{on} x Q_g
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)

RoHS* Available

TO-220 FULLPAK





N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage			V_{DS}	650	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	20	A
		T_C = 100 °C		13	
Pulsed Drain Current [a]			I_{DM}	56	
Linear Derating Factor				1.8	W/°C
Single Pulse Avalanche Energy [b]			E_{AS}	691	mJ
Maximum Power Dissipation			P_D	30	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	T_J = 125 °C		dV/dt	70	V/ns
Reverse Diode dV/dt [d]				26	
Soldering Recommendations (Peak Temperature) [c]	for 10 s			300	°C

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature.
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω, I_{AS} = 7 A.
c. 1.6 mm from case.
d. $I_{SD} \leq I_D$, dI/dt = 100 A/μs, starting T_J = 25 °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.6	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	650	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.74	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	3	-	5	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
		V_{GS} = ± 30 V	-	-	± 1	µA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 520 V, V_{GS} = 0 V, T_J = 125 °C	-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 11 A	-	0.170	-	Ω
Forward Transconductance	g_{fs}	V_{DS} = 8 V, I_D = 5 A	-	6.7	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	2414	-	pF
Output Capacitance	C_{oss}		-	118	-	
Reverse Transfer Capacitance	C_{rss}		-	4	-	
Effective Output Capacitance, Energy Related [a]	$C_{o(er)}$	V_{DS} = 0 V to 520 V, V_{GS} = 0 V	-	89	-	
Effective Output Capacitance, Time Related [b]	$C_{o(tr)}$		-	307	-	
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 11 A, V_{DS} = 520 V	-	73	110	nC
Gate-Source Charge	Q_{gs}		-	15	-	
Gate-Drain Charge	Q_{gd}		-	32	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 520 V, I_D = 11 A, V_{GS} = 10 V, R_g = 9.1 Ω	-	22	45	ns
Rise Time	t_r		-	33	66	
Turn-Off Delay Time	$t_{d(off)}$		-	73	110	
Fall Time	t_f		-	38	76	
Gate Input Resistance	R_g	f = 1 MHz, open drain	-	0.64	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	22	A
Pulsed Diode Forward Current	I_{SM}		-	-	56	
Diode Forward Voltage	V_{SD}	T_J = 25 °C, I_S = 11 A, V_{GS} = 0 V	-	-	1.2	V
Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S = 11 A, dI/dt = 100 A/µs, V_R = 400 V	-	400	-	ns
Reverse Recovery Charge	Q_{rr}		-	5.9	-	µC
Reverse Recovery Current	I_{RRM}		-	20	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

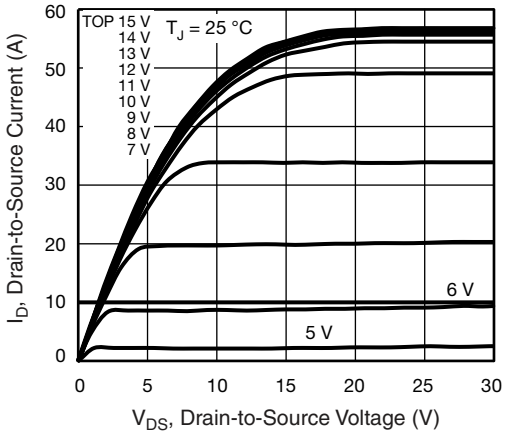


Fig. 1 - Typical Output Characteristics

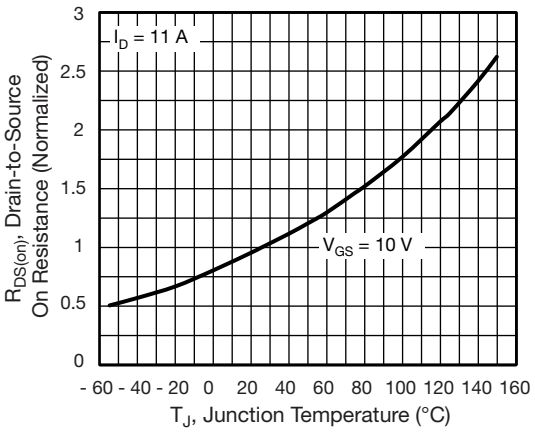


Fig. 4 - Normalized On-Resistance vs. Temperature

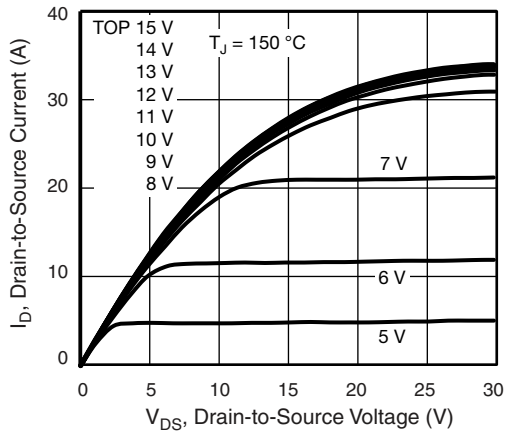


Fig. 2 - Typical Output Characteristics

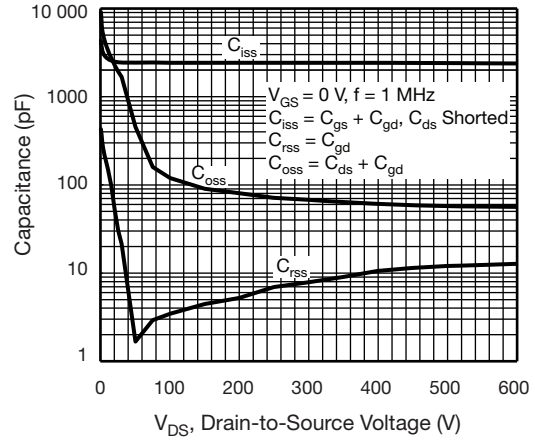


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

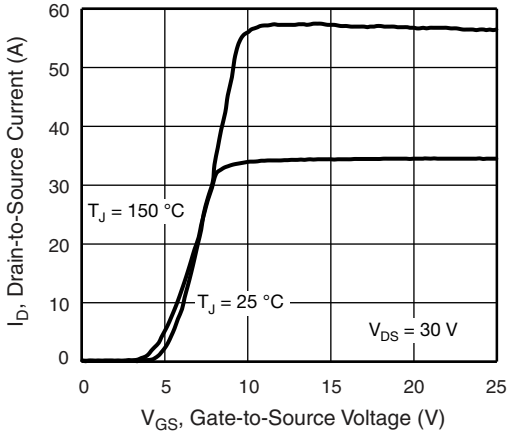


Fig. 3 - Typical Transfer Characteristics

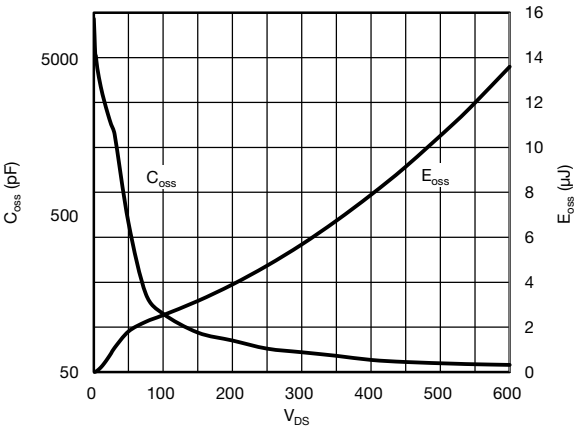


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

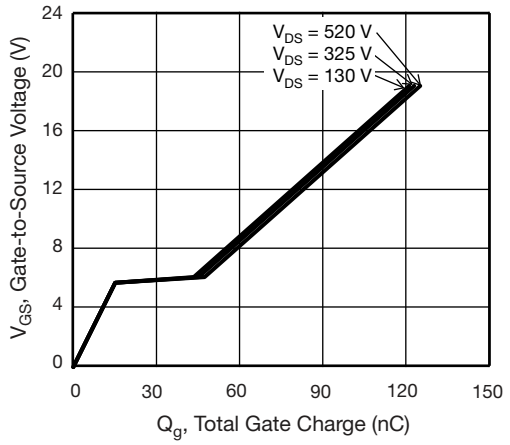


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

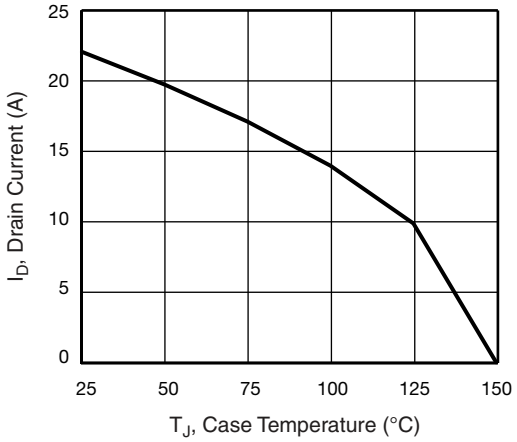


Fig. 10 - Maximum Drain Current vs. Case Temperature

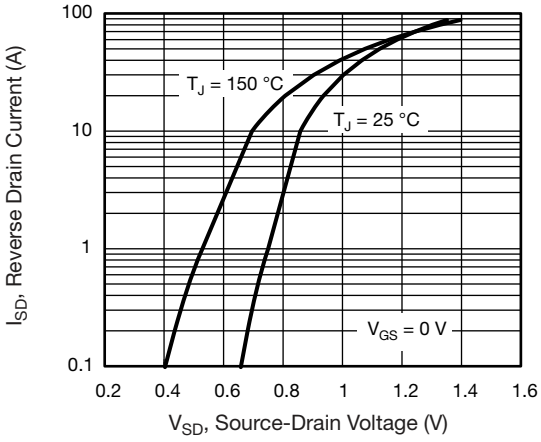


Fig. 8 - Typical Source-Drain Diode Forward Voltage

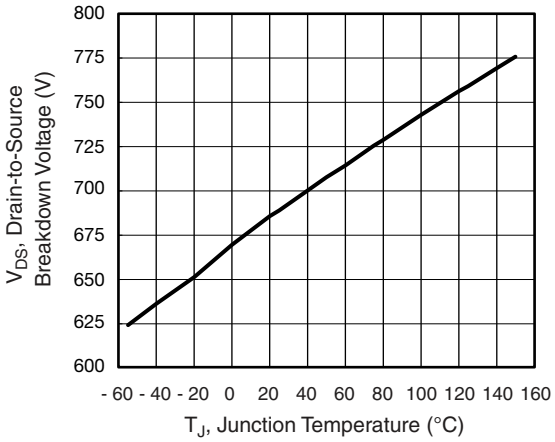


Fig. 11 - Temperature vs. Drain-to-Source Voltage

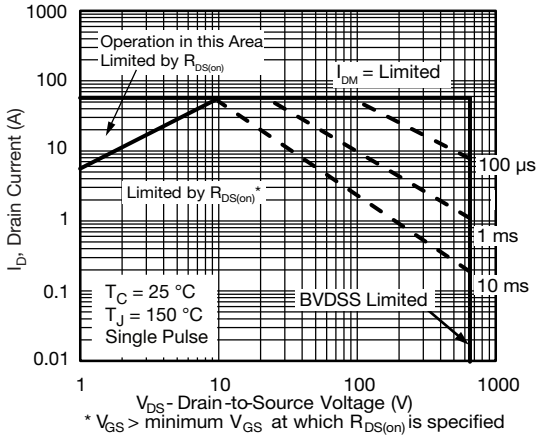


Fig. 9 - Maximum Safe Operating Area

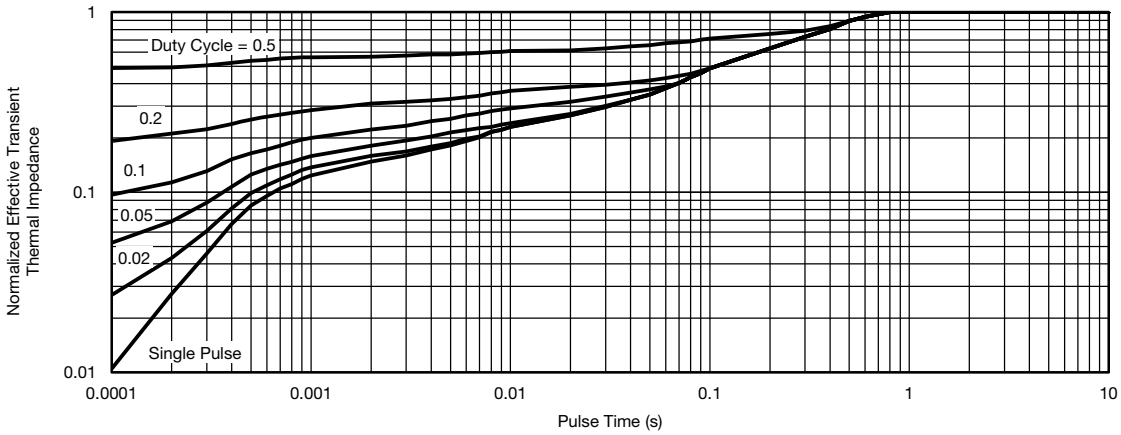


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

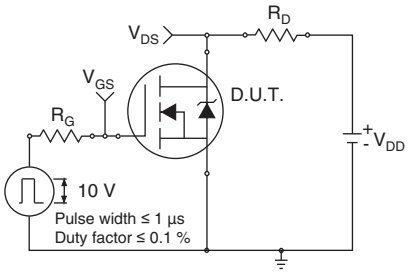


Fig. 13 - Switching Time Test Circuit

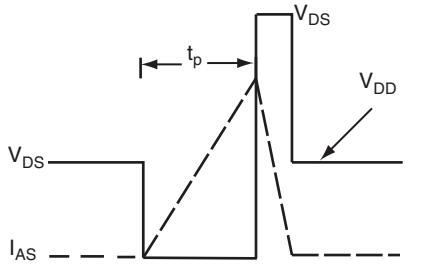


Fig. 16 - Unclamped Inductive Waveforms

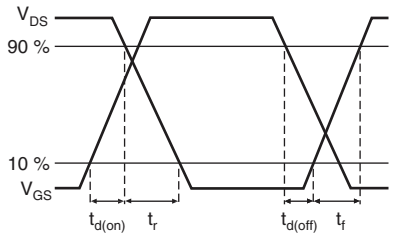


Fig. 14 - Switching Time Waveforms

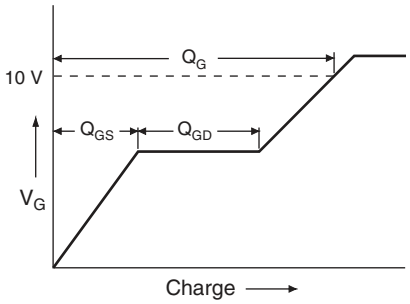


Fig. 17 - Basic Gate Charge Waveform

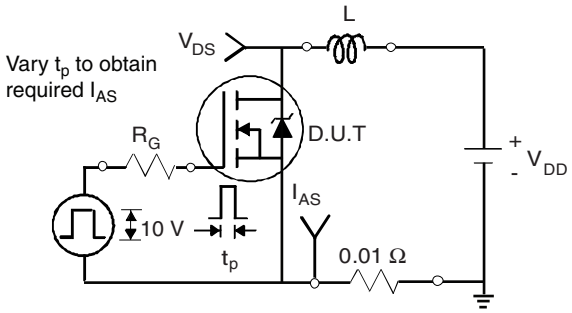


Fig. 15 - Unclamped Inductive Test Circuit

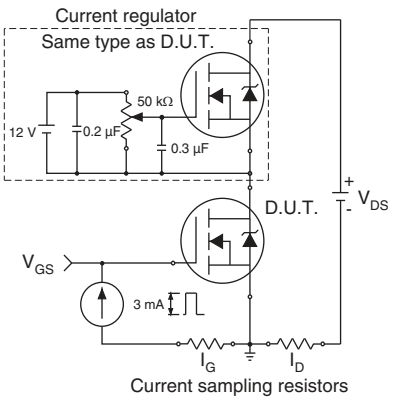
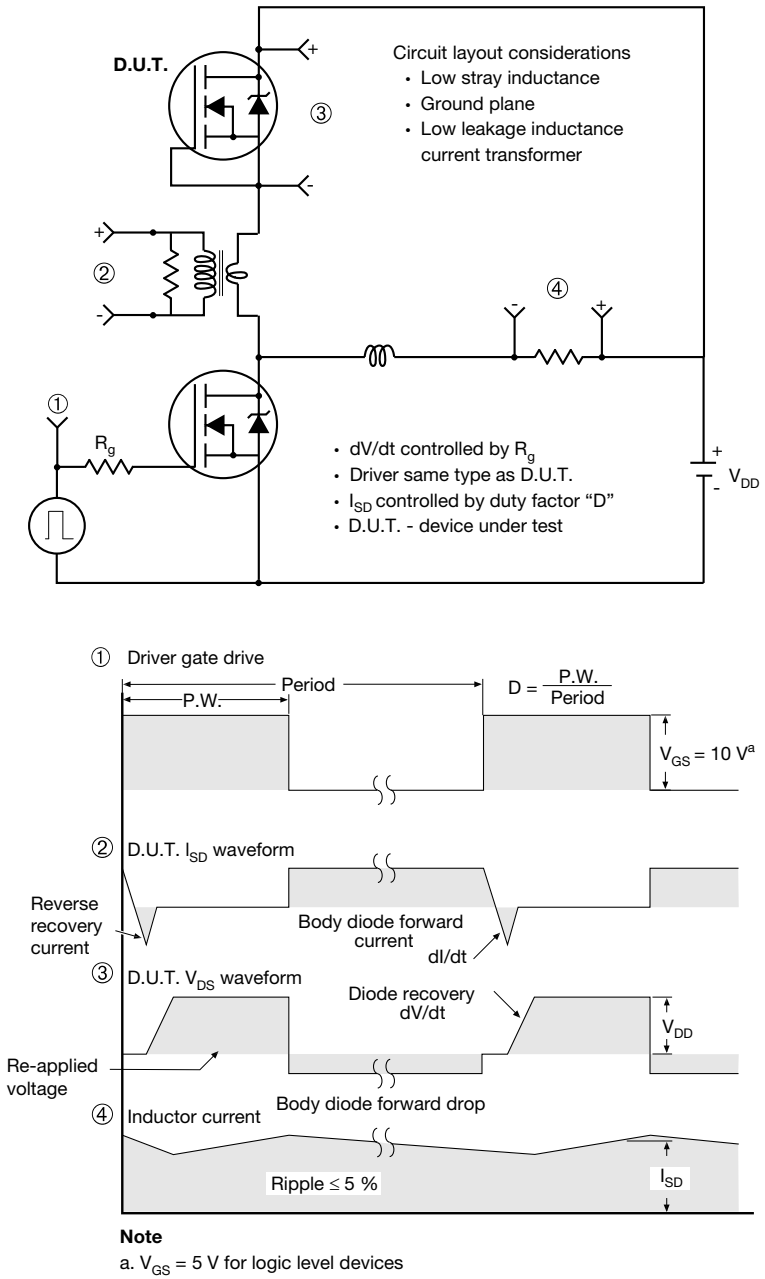


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

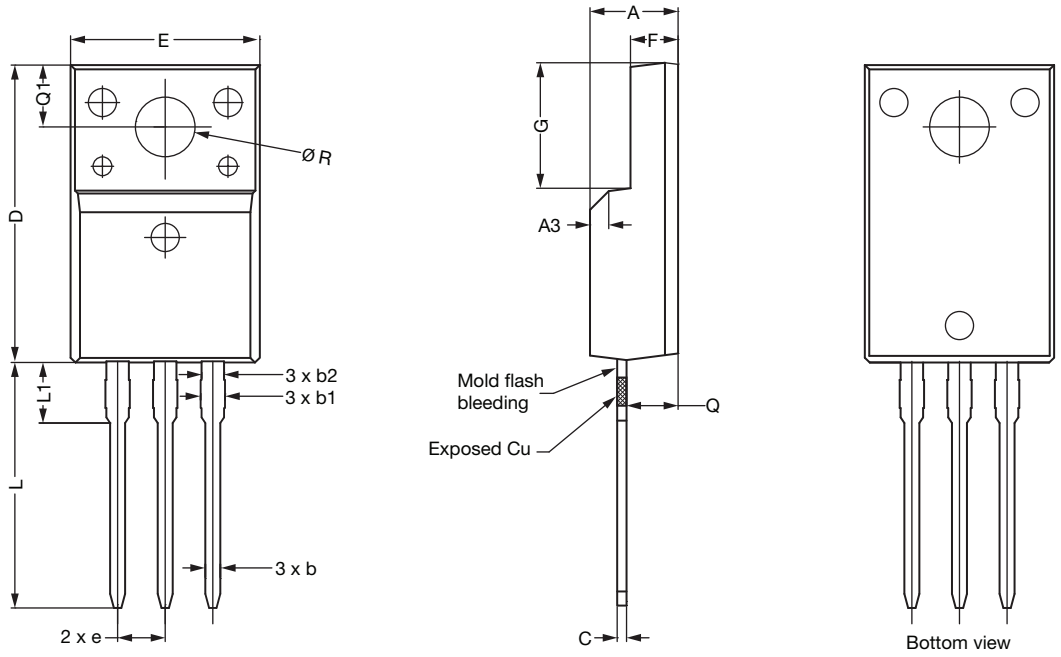


Note

a. V_{GS} = 5 V for logic level devices

Fig. 19 - For N-Channel

TO-220 FULLPAK

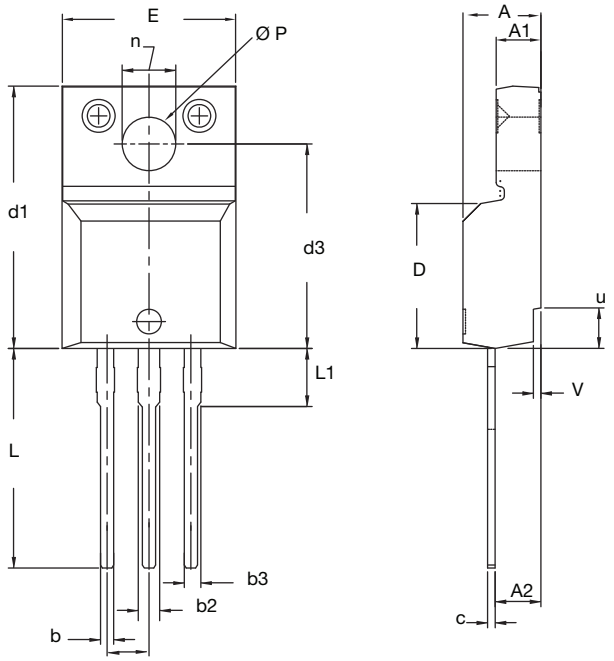


	MILLIMETERS		
DIM.	**MIN.**	**NOM.**	**MAX.**
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e		2.54 BSC	
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
Ø R	3.08	3.18	3.28

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking

FACILITY



	MILLIMETERS		INCHES	
DIM.	**MIN.**	**MAX.**	**MIN.**	**MAX.**
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020
ECN: E19-0180-Rev. D, 08-Apr-2019 DWG: 5972				

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking

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