VDR10N095LSA

N-SGT Enhancement Mode MOSFET

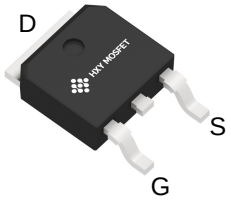
General Description

The VDR10N095LSA use advanced SGT MOSFET

technology to provide low RDS(ON), low gate charge,

fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness.

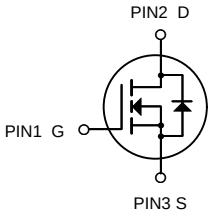


TO-252-2L

General Features

V_{DS} = 100V I_D = 70A

$R_{DS(ON)}$ < 10.5mΩ @ V_{GS}=10 V



N-SGT MOSFET

Applications

DC-DC Converters

Power management functions

Synchronous-rectification applications

Ordering Information

Product ID	Pack	Brand	Qty(PCS)
VDR10N095LSA	TO-252-2L	HXY MOSFET	2500

Absolute Maximum Ratings at T_j=25°C unless otherwise noted

Symbol	Parameter	Value	Unit
V_{DS}	Drain source voltage	100	V
V_{GS}	Gate source voltage	±20	V
I_D	Continuous drain current, T_C=25°C	70	A
P_D	Power dissipation, T_C=25°C	100	W
EAS	Single pulsed avalanche energy	110	mJ
Tstg.T_j	Operation and storage temperature	-55 to 150	°C
$R_{\theta JC}$	Thermal resistance, junction-case	1.25	°C/W
$R_{\theta JA}$	Thermal resistance, junction-ambient	64	°C/W

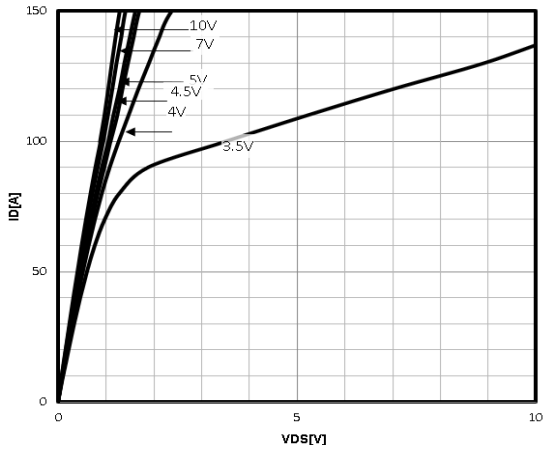
Electrical Characteristics at T_j=25°C unless otherwise specified

Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=100V, V_{GS}=0V	--	--	1	μA
I_{GSS}(F)	Gate to Source Forward Leakage	V_{GS}=+20V, V_{DS}=0V	--	--	100	nA
I_{GSS}(R)	Gate to Source Reverse Leakage	V_{GS}=-20V, V_{DS}=0V	--	--	-100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=VGS, I_D=250μA	1.3	1.8	2.3	V
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V, I_D=20A	--	8.5	10.5	mΩ
		V_{GS}=4.5V, I_D=15A		9.5	15	mΩ
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} = 50V f = 1.0MHz	--	1368	--	pF
C_{oss}	Output Capacitance		--	451	--	
C_{rss}	Reverse Transfer Capacitance		--	12.9	--	
R_g	Gate resistance	V_{GS}=0V,V_{DS} Open	--	0.48	--	Ω
$t_{d(ON)}$	Turn-on Delay Time	I_D =10A V_{DS} = 50V V_{GS} = 10V R_G = 4Ω	--	16	--	ns
t_r	Rise Time		--	10	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	40	--	
t_f	Fall Time		--	6	--	
Q_g	Total Gate Charge	V_{GS} =10V V_{DS} = 50V I_D =10A	--	31.3	--	nC
Q_{gs}	Gate Source Charge		--	3.49	--	
Q_{gd}	Gate Drain Charge		--	7.63	--	
I_S	Diode Forward Current	T_C =25 °C	--	--	70	A
V_{SD}	Diode Forward Voltage	I_S=10A, V_{GS}=0V	--	--	1.2	V
t_{rr}	Reverse Recovery time	I_S=10A, V_{DD}=50V dI/dt=100A/μs	--	103	--	ns
Q_{rr}	Reverse Recovery Charge		--	187	--	nC

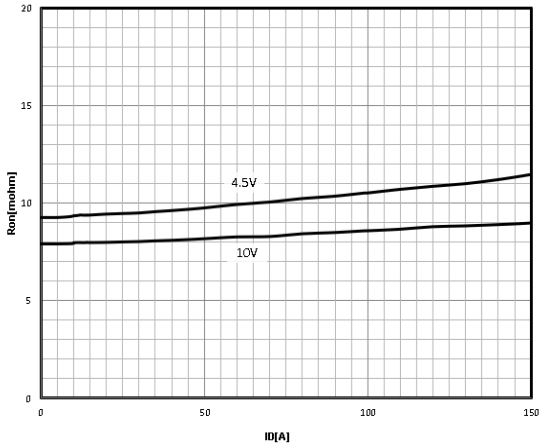
a1: Repetitive rating; pulse width limited by maximum junction temperature
a2: VDD=50V, L=0.3mH, Rg=25Ω, Starting TJ=25°C.

Typical Characteristics

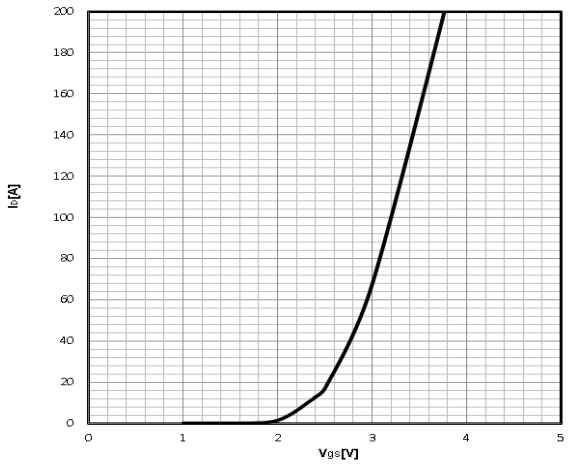
Typ. output characteristics
$I_D=f(V_{DS})$



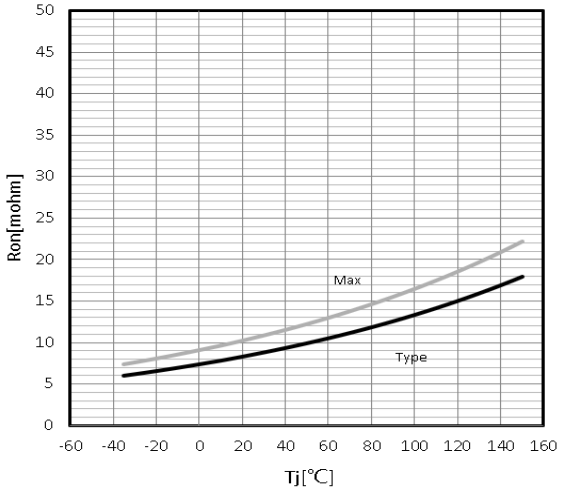
Typ. drain-source on resistance
$R_{DS(on)}=f(I_D)$



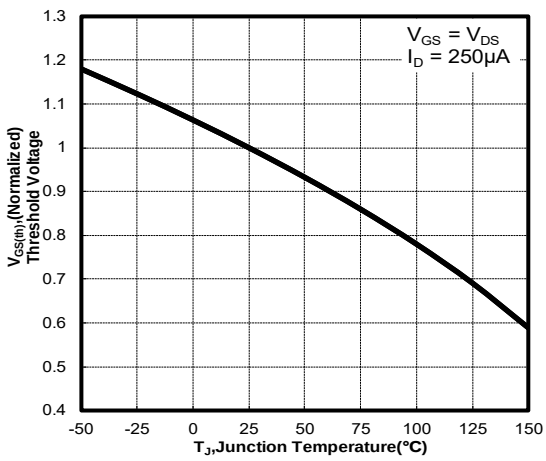
Typ. transfer characteristics
$I_D=f(V_{GS})$



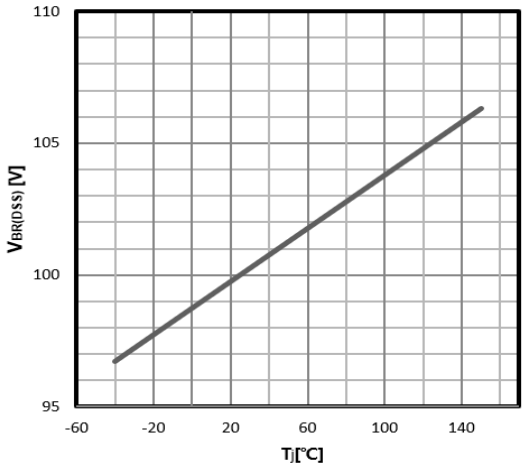
Drain-source on-state resistance
$R_{DS(on)}=f(T_j)$;I_D=20A; V_{GS}=10V



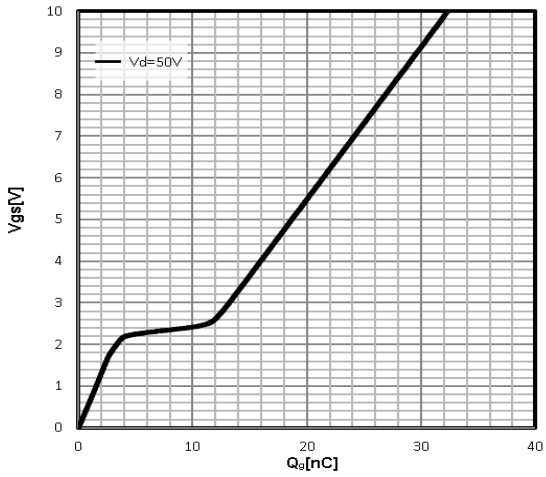
Gate Threshold Voltage
$V_{TH}=f(T_j)$; I_D=250uA



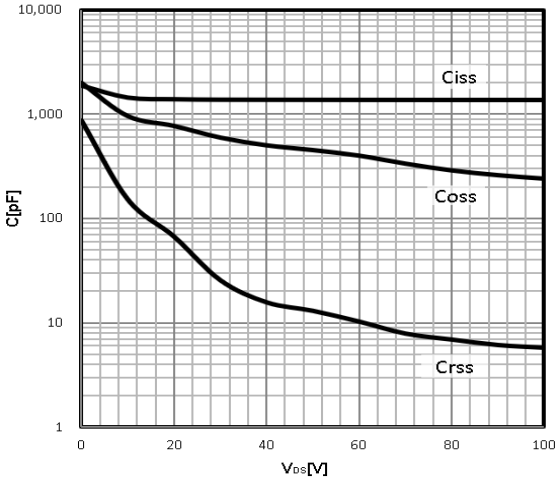
Drain-source breakdown voltage
$V_{BR(DSS)}=f(T_j)$; I_D=250uA



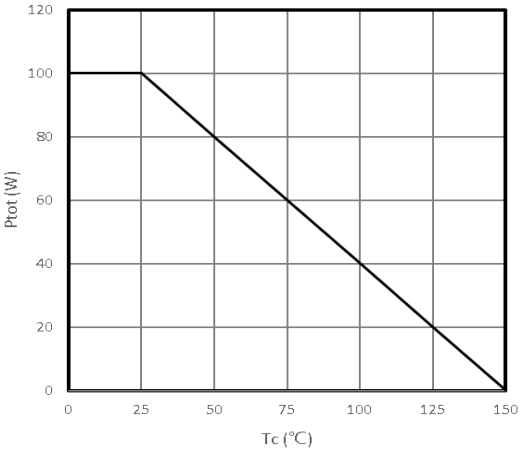
Typ. gate charge
$V_{GS}=f(Q_g)$; $I_D=10A$



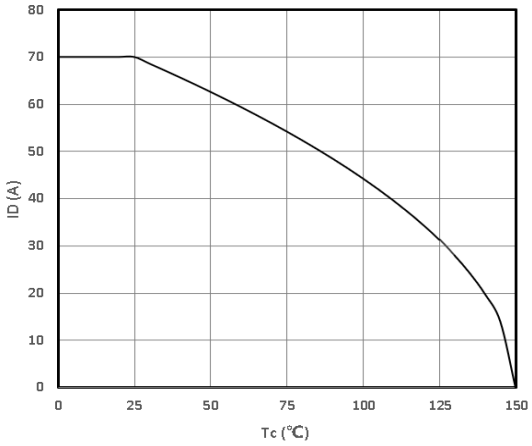
Typ. capacitances
C =f(V_{DS}); V_{GS}=0V; f =1MHz



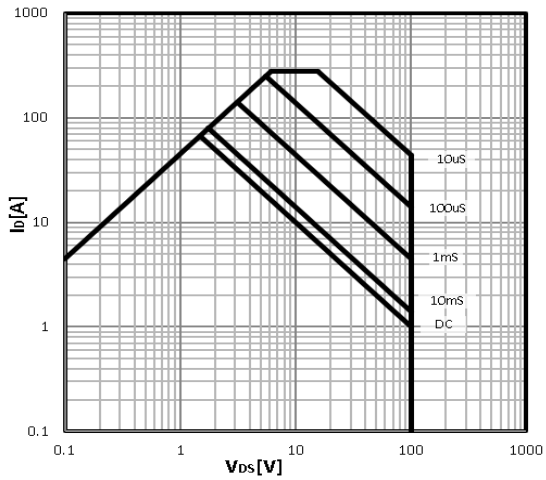
Power Dissipation
$P_{tot}=f(T_C)$



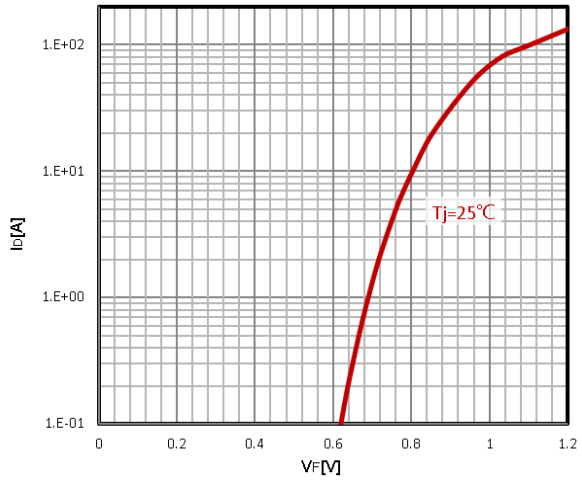
Maximum Drain Current
$I_D=f(T_C)$



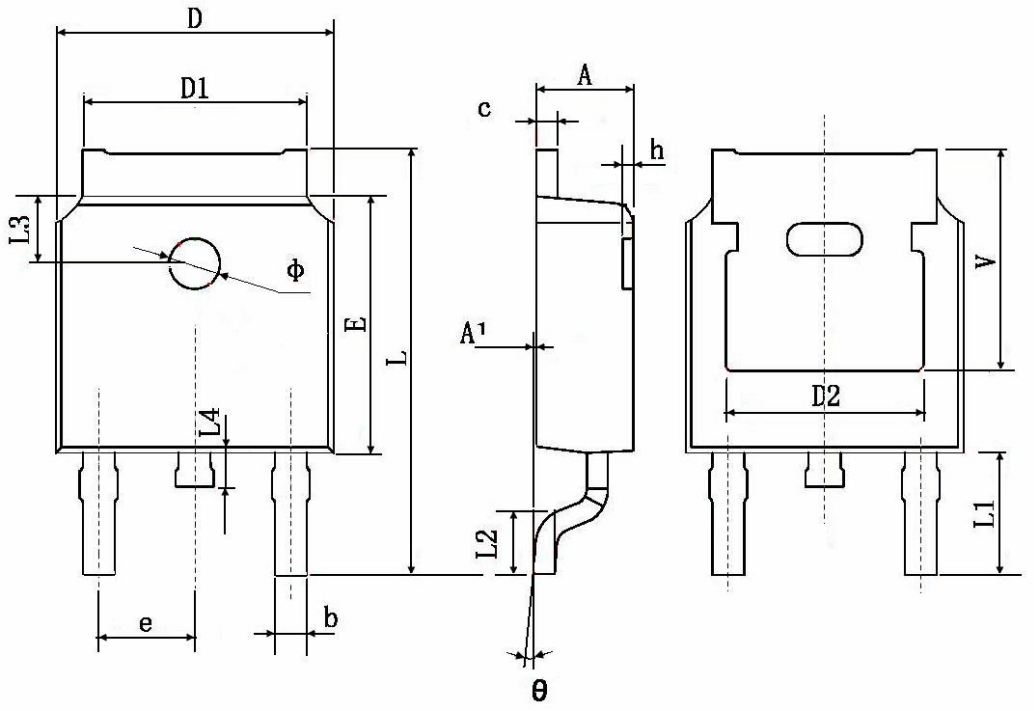
Safe operating area
$I_D=f(V_{DS})$



Body Diode Forward Voltage Variation
$I_F=f(V_{GS})$



TO-252-2L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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